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Research Article

Keywords: Quantum confinement, drain current, transconductance, DMDG-JLFENT, TCAD

Posted Date: June 2nd, 2021

DOI: <https://doi.org/10.21203/rs.3.rs-525148/v1>

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Version of Record: A version of this preprint was published at Silicon on July 27th, 2021. See the published version at <https://doi.org/10.1007/s12633-021-01282-2>.

An approach for drain current modeling including quantum mechanical effects for a DMDG Junctionless Field Effect Nanowire Transistor

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Abstract: This paper presents the effects of quantum confinements on the surface potential, threshold voltage, drain current, transconductance, and drain conductance of a Dual Material Double Gate Junctionless Field Effect Nanowire Transistor (DMDG-JLFET). The carrier energy quantization on the threshold voltage of a DMDG-JLFET is modeled, and subsequently, other parameters like drain current were analytically presented. The QME considered here is obtained under the quantum confinement condition for an ultra-thin channel, i.e., below 10 nm of Si thickness. The threshold voltage shift due to QME can be used as a quantum correction term for compact modeling of junctionless transistors. The analytical model proposed for surface potential, threshold voltage, drain current, transconductance, and drain conductance were verified by TCAD 3-D quantum simulation results which makes it suitable for SPICE compact modeling.

Keywords: Quantum confinement; drain current; transconductance; DMDG-JLFET; TCAD.

1. Introduction

As the IC industry moves toward very low dimensions of the order of 10 nm and below the need for alternate device structure are highly desirable. To overcome the fabrication difficulty to maintain very steep junctions at low dimensions, recently, an alternate MOS structure named Junctionless transistor was proposed [1]. Several analytical models were developed for double gate junctionless transistor with symmetric gate, asymmetric gates [2–6]. The quantum confinements models are also available in literature for these structures [7–9]. Even though this structure has many advantages the leakage current in the sub-threshold regime of Double Gate Junctionless Field Effect Transistors (DG JLFET) is considerably high. It flows through the center of the channel i.e., volume conduction occurs due to the low concentration of the depletion charge carriers [10][11]. The necessity for materials with high work function (~5.6 eV) arises from turning the device properly OFF and lowering the subthreshold leakage current [12], which is technologically challenging. To overcome this problem, the use of dual material (DM) in the gate [1, 4] was suggested, enhancing the electrostatic performance of the device by incorporating a step in the surface potential profile.

In 2014, Agarwal *et al.* [12] proposed a pseudo-2-D surface potential model for dual material double gate junctionless field-effect transistor (DMDG-JLFET). Baruah *et al.* [13] presented a study on analog circuit performance of a DMDG-JLFET with a high k-spacer. Recently, Kumari *et al.* [10] proposed a theoretical investigation of DMDG-JLFET for analog and digital performance. Gupta *et al.* [14], showed that a continuous increase in the threshold voltage was observed as we move down towards sub 10nm regime of the silicon film thickness. The growth is less prominent above 10nm silicon thickness which occurs due to QMEs [15]. Because of the high substrate doping and ultra-thin silicon thickness, severe band bending on the substrate occurs. The narrowing of potential well in the interface is sufficient for energy quantization of the carrier [16]. As a result, the inversion charge density will get reduced at the same gate bias compared to the classical mechanically computed results. The inclusion of quantum mechanical analysis becomes necessary when the device dimensions are scaled down to 10nm as the QME governs the device performances at such a small dimension.

This paper has included the QME on DMDG JLFENT by incorporating the shift in threshold voltage and charge quantization effects. The analytical model results were verified with that obtained from the 3-D GENIUS Visual TCAD quantum simulation, which shows the high accuracy of our model.

2. Analytical model

The 3-D Poisson's equation in the channel region for the DMDG JLFENT device shown in Fig. 1(a), can be written as

$$\frac{d^2\psi(x, y, z)}{dx^2} + \frac{d^2\psi(x, y, z)}{dy^2} + \frac{d^2\psi(x, y, z)}{dz^2} = \frac{qN_{si}}{\epsilon_{si}} [e^{(\psi(x, y, z) - V)/V_T} - 1], \quad (1)$$

where,

$\psi(x, y, z)$ = Potential at any point in the channel,

N_{si} = Channel doping concentration, ϵ_{si} = Dielectric constant of silicon,

V = Quasi-Fermi potential, V_T = Thermal voltage,

As the variation along the width (z) is very less so we consider a parabolic potential profile as

$$\psi(x, y) = \psi_s(x) + \alpha(x)y + \beta(x)y^2, \quad (2)$$

where $\psi_s(x)$ is the surface potential, $\alpha(x), \beta(x)$ are arbitrary coefficients that are functions of 'x'. The total channel length is $L=20$ nm and $L_{M1}=10$ nm, $L_{M2}=10$ nm is the portion of the channel under the metal M_1 and M_2 , respectively.

Fig. 1: (a) Schematic cross-section (b) TCAD simulation device structure of DMDG JLFENT.

1.2.1. Surface potential model

In DMDG JLFENT we have two different gate materials with different work functions so the flat-band voltages can be given as

$$V_{FB1} = \phi_{M1} - \phi_{si} \quad \text{and} \quad V_{FB2} = \phi_{M2} - \phi_{si}, \quad (3)$$

here ϕ_{M1}, ϕ_{M2} are work functions of metal M_1, M_2 and ϕ_{si} is that of the silicon region, respectively.

Now, the potential under the gate (M_1) can be written as,

$$\psi_1(x, y) = \psi_{s1}(x) + \alpha_{11}(x)y + \beta_{12}(x)y^2. \quad (4)$$

Similarly, the potential under the gate (M_2) can be written as,

$$\psi_2(x, y) = \psi_{s2}(x) + \alpha_{21}(x)y + \beta_{22}(x)y^2. \quad (5)$$

The Poisson's equation (1) under two gates can be solved using the boundary conditions:

1. The electric flux at the front gate-oxide interface is continuous,

$$\frac{\epsilon_{si}}{C_{ox}} \frac{\partial \psi_1(x, y=0)}{\partial y} = (V_{GS1} - V_{FB1} - \psi_{s1}(x)) , \quad \text{for } M_1 \quad (6)$$

$$\frac{\epsilon_{si}}{C_{ox}} \frac{\partial \psi_2(x, y=0)}{\partial y} = (V_{GS2} - V_{FB2} - \psi_{s2}(x)) , \quad \text{for } M_2 \quad (7)$$

here, the gate oxide capacitance is $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$, where ϵ_{ox} is the dielectric constant of the oxide layer and t_{ox} is oxide layer thickness.

2. The surface potential at the interface of two different materials is continuous,

$$\psi_{s1}(L_1) = \psi_{s2}(L_1). \quad (8)$$

3. The electric field at the interface of two different materials is continuous,

$$\left. \frac{d\psi_{s1}}{dx} \right|_{L1} = \left. \frac{d\psi_{s2}}{dx} \right|_{L1}. \quad (9)$$

Considering the extra depletion ' d_s ' into the source region, we have the potential at the source end to be,

$$\psi_{Source} = V - \frac{qN_{si}d_s^2}{2\epsilon_{si}}. \quad (10)$$

The potential at the drain end similarly can be given as,

$$\psi_{Sdrain} = V + V_{DS} - \frac{qN_{si}d_D^2}{2\epsilon_{si}}. \quad (11)$$

In junctionless transistor's high current flows before the flat band condition, we would consider full and partial depletion modes of operations that are enough for most practical applications. Poisson's equation neglecting mobile charge in depletion mode ($V_{GS} < V_{Th}$) can thus be written as,

$$\frac{\partial^2 \psi(x, y)}{\partial x^2} + \frac{\partial^2 \psi(x, y)}{\partial y^2} = -\frac{qN_{si}}{\epsilon_{si}}, \quad (12)$$

due to symmetry, the electric field at the center is zero thus

$$\frac{\partial \psi(x, y = -t_{si}/2)}{\partial x^2} = 0. \quad (13)$$

The coefficients $\alpha_{j1}(x), \beta_{j2}(x)$ can be obtained from the (6), (7), and (13) where $j=1, 2$. Using the values of coefficients in (4) and (5) and then substituting the potentials in (12) we have,

$$\frac{\partial^2 \psi_{s_j}}{\partial x^2} - a\psi_{s_j} = b_j,$$

$$a = \frac{C_{ox}}{t_{si}\epsilon_{si}}, \quad (14)$$

$$b_j = -\left[\frac{qN_d}{\epsilon_{si}} + A(V_{GS} - \psi_{M_j} + \psi_{S_j}) \right]. \quad (15)$$

When $V_{Th} < V_{GS} < V_{FB}$, the transistor operates in partial depletion mode during which a neutral region starts to develop in the middle of the device. Taking the origin to be at the center of the device, the electric field and depletion thickness ' y_d ' can be calculated as [12],

$$E_0 = \frac{\partial \psi(x, y = y_0)}{\partial y} = \frac{-8V_T y_d}{t_{si}^2}, \quad (16)$$

$$y_d = \frac{-m + \sqrt{m^2 - 4nl}}{2l}; \quad (17)$$

where,

$$l = \frac{qN_{si}}{2\epsilon_{si}} + \frac{8V_T}{t_{si}^2}, \quad m = \frac{qN_{si}}{C_{ox}} + \frac{8\epsilon_{si}V_T}{C_{ox}t_{si}^2}, \quad n = V_{GS} - V_{FB2} - V + V_T.$$

The potential in the neutral region follows a simple parabolic potential approximation [17], where the potential at the center (V_C) of the device can be approximated as,

$$\psi(x, y = -t_{si}/2) = V_C. \quad (18)$$

The coefficients $\alpha_{j1}(x), \beta_{j2}(x)$ are deduced from the boundary conditions (8), (9), and (18). Substituting their corresponding values in (4) and (5) and then from (12), we obtain,

$$\frac{\partial^2 \psi_{S_j}}{\partial x^2} - a\psi_{S_j} = b_j, \quad (19)$$

where,

$$a = \frac{C_{ox}}{y_d \epsilon_{si}}, \quad \text{and} \quad b_j = -\left[\frac{qN_d}{\epsilon_{si}} + A(V_{GS} - \psi_{M_j} + \psi_{S_j}) \right]; \quad j=1, 2.$$

1.2.2. Combination of operating modes

As the gate work functions are different ($\phi_{M1} > \phi_{M2}$), thus the threshold and the flatband voltages for the gate under metal M_1 (G_{M1}) are higher than that of the gate under metal M_2 (G_{M2}). When we apply gate voltage, the corresponding channel region may be in different modes of operations. The first useful combination is the full depletion under G_{M1} and partial depletion under G_{M2} . Under this condition, the surface potentials are,

$$\psi_{s1}(x) = C_1 e^{\kappa_1 x} + D_1 e^{-\kappa_1 x} - \frac{b_1}{a}, \quad \text{for } 0 \leq x \leq L_1 \quad (20)$$

$$\psi_{s2}(x) = C_2 e^{\kappa_2(x-L_1)} + D_2 e^{-\kappa_2(x-L_2)} - \frac{b_2}{a}, \quad \text{for } 0 \leq x \leq L_2 \quad (21)$$

where the coefficients are deduced using the boundary conditions equations (6-9).

Similarly, the surface potential for the second possible combination, i.e., channel region under both the gates G_{M1} and G_{M2} , is in partial depletion. It happens when gate voltage crosses the threshold voltage of G_{M1} .

1.2.3. Threshold voltage model

Substituting $y_d = -t_{si}/2$ in equation (17) and solving for the gate voltage, we get the threshold voltage as,

$$V_{Th} = V_{FB1} - \frac{qN_{si}}{8\epsilon_{si}}t_{si}^2 - \frac{qN_{si}}{2\epsilon_{ox}}t_{si}t_{ox} + V_C - 3V_T - \frac{4C_{si}}{C_{ox}}V_T. \quad (22)$$

1.2.4. Inclusion of Quantum mechanical effect

In the subthreshold region of junctionless transistors, the channel is fully depleted, the channel potential is bent, and electrons are preferentially confined at the center of the channel. The Schrödinger's equation can be decoupled from the Poisson's equation by neglecting the mobile charge term in the Poisson's equation, when t_{si} is large the discrete subband energy is mostly confined between the bent portion of the conduction band boundaries. In this case, the system is similar to a quantum harmonic oscillator (QHO) with an energy potential given as [16],

$$V_{QM} = \frac{q^2 N_{si} x^2}{2\epsilon_{si}}. \quad (23)$$

Using the effective-mass approximation, the discrete sub-band energy levels can be expressed as

$$E_{k,n} = \left(n + \frac{1}{2}\right) \frac{h}{2\pi} \sqrt{\frac{q^2 N_{si}}{m_{c,k}^* \epsilon_{si}}}, \quad (24)$$

where n is a quantum number ($n=0, 1, 2, 3, \dots$), and h is the Planck's constant. When the t_{si} is small, the discrete sub-band energy levels for this case are expressed by [16]

$$E_{k,n} = \frac{h^2 n^2}{8m_{c,k}^* t_{si}^2} + \frac{q^2 N_{si} t_{si}^2}{24\epsilon_{si}} \left(1 - \frac{6}{\pi^2 n^2}\right), \quad (25)$$

where, $k=1$ and 2 ; $n=1, 2, 3, \dots$

The quantum shift in threshold voltage is incorporated by the energy quantization of the carriers in a channel. In a silicon crystal with $\langle 100 \rangle$ orientation, six valleys in the conduction band clustered into two separate groups with degeneracy factors $g_1=2$ and $g_2=4$, respectively [18].

Quantum Shift in threshold voltage can then be expressed as [18],

$$\Delta V_{Th}^{QM} = \left[\frac{dV_{GS}}{d\psi_{si}} \Delta \psi_{si}^{QM} \right] = m \Delta \psi_{si}^{QM}, \quad (26)$$

where,

$$\Delta \psi_{si}^{QM} \approx \frac{kT}{q} \ln \left[\frac{h^2 N_c}{4\xi_s \pi q \left(2m_{d,1}^* \sum_{n=1}^{\infty} e^{-\left(\frac{E_{1,n}}{kT}\right)} + 4m_{d,2}^* \sum_{n=1}^{\infty} e^{-\left(\frac{E_{2,n}}{kT}\right)} \right)} \right],$$

ξ_s = Electric field at the surface.

W_{dm}^0 = Maximum depletion width.

The threshold voltage including the quantum shift now can be expressed as

$$V_{Th}^{CL+QM} = V_{Th}^{CL} + \Delta V_{Th}^{QM}. \quad (27)$$

Thus surface potential becomes

$$\psi'_{s_j}(x) = C_j e^{\kappa_j(x-L_1)} + D_j e^{-\kappa_j(x-L_1)} - \frac{b'_j}{a}; \quad j=1,2 \quad (28)$$

where,

$$b'_j = - \left[\frac{qN_{si}}{\epsilon_{si}} + a(V_{GS} - V_{Th}^{CL+QM}) \right].$$

The equation (28) gives the surface potential with QME. However, it can be noted that while carrying out investigations, the QME is assumed to be uniform throughout the channel.

1.2.5. Drain current and transconductance model

The drain current equation for DMDG JLFENT, including the quantum effect, can be obtained by using (27) for threshold voltage in linear and saturation regions of operations as

$$I_{D_lin} = \kappa[(V_{GS} - V_{Th}^{CL+QM})V_{DS} - \frac{V_{DS}^2}{2}], \quad (29)$$

$$I_{D_sat} = \kappa(V_{GS} - V_{Th}^{CL+QM})^2, \quad (30)$$

where, $\kappa = \mu_n C_{ox}(W/L)$.

The gate transconductance equation is obtained from (30) as

$$g_m = \frac{dI_D}{dV_{GS}} = \kappa(V_{GS} - V_{Th}^{CL+QM}). \quad (31)$$

The drain conductance equation is obtained from (29) as

$$g_{ds} = \frac{dI_D}{dV_{DS}} = \frac{\kappa}{2}(V_{GS} - V_{Th}^{CL+QM})^2. \quad (32)$$

3. Results and Discussion

To validate the semi-analytical model for threshold voltage, drain current, and transconductance, the results were compared with that obtained from GENIUS 3-D TCAD software [19]. Fig. 1(b) shows the 3D device structure with mesh distribution used for simulation. To include the dependence on the impurity concentrations and the transverse and longitudinal electric field values Lombardi mobility model is employed. Carrier trapping, the DIBL, the Shockley-Read-Hall recombination model, and Fermi-Dirac carrier statistics with impact ionization is utilized in the simulations. The quantum mechanical effect can be modeled using the density gradient technique [20]. The QME model is based on the Wigner Function Equations of motion moments, which consists of quantum correction to the carrier current equations. The corrected carrier current equations and their derivatives are pretty sensitive to low carrier concentrations. The doping concentration of the entire Silicon region is $5 \times 10^{19} \text{ cm}^{-3}$ and the work function of the gate metals M_1 and M_2 are considered as 5.4 eV and 4.7 eV, respectively. Throughout the paper the oxide thickness is considered to be 2 nm unless mentioned. The GENIUS

VTCAD 3D quantum simulation results are shown as symbols, and the thick lines represent the results obtained from our analytical model for all results illustrated in this paper.

Fig. 2-3, shows the surface potential variations with V_{GS} for two different values of silicon thickness of 10nm and 6nm, respectively. In both the figures, we can observe a step increase in the surface potential due to the use of two dissimilar metals having different work functions. As the work function increases, the surface potential decreases; thus the surface potential under the gate G_{M1} is lower than that of the gate G_{M2} . Figure 2, where silicon thickness is 10nm, shows the surface potential bent is more prominent under the gate G_{M1} due to higher work function difference, thereby controlling the threshold voltage, therefore the name control gate. When V_{GS} is 0V, the bent is highest and the region under G_{M1} is fully depleted and under G_{M2} is partially depleted. As the V_{GS} increases the bent decreases and at 0.6V the region under G_{M1} is partially depleted and under G_{M2} is near flat band. In figure 3, the silicon thickness is considered 6nm; the bent is more prominent than that of 10 nm at any given V_{GS} , which can be explained based on higher QME or confinement effect with a decrease in silicon thickness. The quantum effect is more prominent since the electron concentration peaks below the silicon-oxide interface and goes nearly zero at the interface, which is entirely in contrast to the classical model. Classically, the electron concentration peaks at the surface. The bending that occurred in the curve at the end portion is due to the inclusion of d_s (depletion towards source region) and d_D (depletion towards drain region) in our analytical model. In both cases the model shows excellent agreement with that of the quantum simulation results of 3-D VTCAD software.

Figure 4, shows the surface potential variations along the channel for different values of silicon thickness from 4nm to 10nm, while V_{DS} kept at 0.5V and V_{GS} kept at 0.4V, respectively. Here we can observe that as the silicon thickness decreases from 10nm down towards 4nm, the bent in the surface potential contours also increases and this happens because of a higher control of gate over the channel, and the charge carriers become more and more confined due to higher QME.

The transfer characteristics of the DMDG JLFENT were plotted in Fig 5-7. The variation of the drain current to the gate voltage is shown in Fig. 5. While V_{DS} was kept constant, the silicon thickness was varied from 10nm down to 4nm. Here we can observe that, as silicon thickness decreases, the drain current reduces for the same value of V_{GS} . Moreover, we can observe that at 4nm, the curve is not smooth because of distortion that occurred due to the high confinement effect or QME. Fig 6, shows the same plot on a semi-logarithmic scale, reflecting the low leakage current in smaller silicon body thickness due to better control of the gate over the channel. Fig 7, shows the variation of the drain current regarding V_{DS} where V_{GS} was kept constant at 0.5V and silicon thicknesses are being varied. Here we can note that as silicon thickness decreases, the drain current reduces, which is evident for reduced charged carriers and confinement effects. In all the cases Fig. 5-7, the model is in good agreement with quantum simulation results of 3-D VTCAD software.

The transconductance for varying silicon thickness model was plotted in Fig. 8; we can observe that the plot for T_{si} of 4nm is low up to the threshold voltage and increases just after crossing it. This may be because of the very high confinement effect as compared to others. Fig. 9, shows the drain conductance model for various silicon thicknesses where we can observe that the conductance was low for lower dimensions owing to lower corresponding drain currents. In both cases, the model shows excellent agreement with that of the quantum 3D TCAD simulation results.

Fig. 2: Surface Potential along the channel with thickness of 10nm

Fig. 3: Surface Potential along the channel with a thickness of 6nm

Fig. 4: Surface Potential along the channel with varying thicknesses

Fig. 5: I_{DS} - V_{GS} characteristics with t_{si} of the proposed model for DMDG JLFENT

Fig. 6: Log (I_{DS})- V_{GS} with t_{si} of the proposed model.

Fig. 7: I_{DS} - V_{DS} characteristics with different t_{si} of the proposed model.

Fig. 8: Transconductance variations with V_{GS} for different t_{si} of DMDG JLFENT

Fig. 9: Drain conductance variations with V_{DS} for different t_{si} of DMDG JLFENT.

4. Summary

This paper investigated the effects of quantum confinements on the several key parameters of a DMDG-JLFENT. The carrier energy quantization on the threshold voltage of a DMDG-JLFENT is analytically modeled. The QME considered here is obtained under the quantum confinement condition for an ultra-thin channel, i.e., below 10 nm of Si thickness. Based on the shifts in threshold voltage, the change in drain current, transconductance, and drain conductance with quantum effects were modeled. The analytical model proposed for surface potential, threshold voltage, drain current, transconductance, and drain conductance were verified by GENIUS Cogenda VTCAD 3-D quantum simulation results. The model is thereby suitable for compact modelling.

Acknowledgments The author is highly thankful to the Department of Electronics and Communication Engineering, NEHU Shillong for providing the software support in carrying out this work.

Declarations

Funding

The authors did not receive support from any organization for the submitted work.

- No funding was received to assist with the preparation of this manuscript.
- No funding was received for conducting this study.
- No funds, grants, or other support was received.

Conflicts of interest/Competing interests

Conflict of Interest

- The authors have no relevant financial or non-financial interests to disclose.
- The authors have no conflicts of interest to declare that are relevant to the content of this article.
- All authors certify that they have no affiliations with or involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript.
- The authors have no financial or proprietary interests in any material discussed in this article.

The authors followed all accepted principles of ethical and professional conduct.

Consent to Participate The research involved no human participants and animals.

Consent for Publication The research involved no such materials which requires consent for publication

Availability of data and material There are no linked data or material to this submission

Authors' contributions All work carried out by the author N. Bora.

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Figures

Figure 1

(a) Schematic cross-section (b) TCAD simulation device structure of DMDG JLFENT.

Figure 2

Surface Potential along the channel with thickness of 10nm

Figure 3

Surface Potential along the channel with a thickness of 6nm

Figure 4

Surface Potential along the channel with varying thicknesses

Figure 5

IDS-VGS characteristics with t_{Si} of the proposed model for DMDG JLFENT

Figure 6

Log (IDS)-VGS with tSi of the proposed model.

Figure 7

IDS-VDS characteristics with different t_{Si} of the proposed model.

Figure 8

Transconductance variations with VGS for different t_{Si} of DMDG JLFENT

Figure 9

Drain conductance variations with VDS for different t_{Si} of DMDG JLFENT.