Analog/RF Performance of Triple Material Gate Stack-Graded Channel Double Gate-Junctionless Strained-Silicon MOSFET with Fixed Charges

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Analog/RF performance of Triple Material Gate Stack-Graded Channel Double Gate-Junctionless strained-silicon MOSFET with fixed charges

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Abstract In this paper, analog/radio frequency (RF) electrical characteristics of triple material gate stack-graded channel double gate-Junctionless (TMGS-GCDG-JL) strained-Si (s-Si) MOSFET with fixed charge density is analyzed with the help of Sentaurus TCAD. By varying the various device parameters, the analog/RF performance of the proposed TMGS-GCDG-JL s-Si MOSFET is evaluated in terms of transconductance-generation-factor (TGF), early voltage, voltage gain, unity-power-gain frequency (f_{max}), unity-current-gain frequency (f_t), and gain-transconductance frequency product (GTFP). The results confirm that the proposed TMGS-GCDG-JL s-Si MOSFET has superior analog/RF performance compared to gate stack-graded channel double gate-junctionless (GS-GCDG-JL) s-Si device. However, the proposed MOSFET has less transconductance and less output conductance when compared with the GS-GCDG-JL s-Si device in above threshold region, and reverse trend follows in sub-threshold region.

Keywords Fixed charges · Early voltage · Strained-silicon · Short channel effects · Transconductance.

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1 Introduction

Nano scaled strained-silicon (s-Si) MOSFETs are promising candidates for upcoming high-speed devices on account of high field velocity, enhanced mobility, and higher driving current [1]-[6]. With the aid of layer transfer process [7], the strain is developed in the silicon material. In this method, the biaxial-tensile strain is introduced in silicon material by growing the silicon material on the relaxed $Si_{(1-X)}Ge_{(X)}$ material, which is developed on the Silicon-on-insulator (SOI) layer. When device operates in nano-scaled regime, fixed charges are created at Oxide/s-Si (SiO_2/s-Si) interface due to the lateral electric field in s-Si MOSFETs [8]-[9]. Thereby, the performance of MOSFET deteriorates in terms of threshold voltage and channel potential.

A few authors have presented the impact of fixed charges on the electrical characteristics of double gate (DG) junctionless device [10]-[12]. Also, they have confirmed that the fixed charges at the SiO_2/s-Si interface of MOSFET can cause change in the channel potential and threshold voltage. To suppress the hot carrier effects (HCEs), the triple metal gate (TMG) engineering is introduced in DG MOSFET [13]-[14]. In TMG structure, screen and control gates are used with three distinct work functions. Therefore, a step equivalent profile in s-Si channel potential and increase in average electric-field of s-Si channel are obtained. Hence, the performance of DG device is improved by employing the TMG structure. To further suppress HCEs, gate stack (GS) structure is also incorporated in DG MOSFET to achieve better device performance in terms of gate leakage current and drive current [15]-[16]. Furthermore, graded channel (GC) engineering is employed in DG junctionless device, thus resulting in improved analog/RF characteristics owing to diminished HCEs

[17]-[18]. Therefore, better performance of the DG junctionless MOSFET is obtained by employing the GS with gate and channel engineering.

The analog/RF electrical characteristics of junctionless MOSFETs for low power applications was demonstrated in [19]. Moreover, enhancement in early voltage and intrinsic voltage gain are attained due to low electric field at drain end of oxide interface. In [20], the effect of laterally graded channel doping in double gate junctionless MOSFETs for analog/RF applications was presented. Besides, high cutoff frequency and high intrinsic voltage gain are obtained. In [21], the comparative analysis of DG junction less and GS DG junction less MOSFETs was presented. Also, the effect of doping on obtaining the optimum performance of the device was studied. In [22], the analytical modeling of leakage currents in dual material halo doped cylindrical gate junctionless MOSFET was illustrated. Till now, in literature, the analog/RF characteristics of triple material gate stack-graded channel DG-junctionless (TMGS-GCDG-JL) s-Si device with the fixed charges has not been presented. By employing the GC and GS structure with gate engineering, better analog/RF performance of junctionless s-Si DG device is achieved.

This paper demonstrates the analysis of analog/RF characteristics of TMGS-GCDG-JL s-Si device with fixed charges. The analog/RF characteristics of TMGS-GCDG-JL s-Si device is exhaustively analyzed by varying the strain (m), fixed charge density (N_f), and the thickness of high-k material (t_{ox2}). Moreover, the analog figure of merits of the proposed MOSFET are evaluated in terms of transconductance generation factor $\left(TGF = \left(\frac{g_m}{I_{ds}}\right)\right)$, early voltage $\left(\frac{I_{ds}}{g_{ds}}\right)$, and intrinsic voltage gain $\left(\frac{g_m}{g_d}\right)$. Besides, the RF figure of merits of the proposed device, unity current gain frequency (f_t), unity power gain frequency (f_{max}) and gain transconductance frequency product $\left(GTFP = \left(\frac{g_m}{g_d}\right)\left(\frac{g_m}{I_d}\right) f_t\right)$, are evaluated exhaustively. The analog/RF characteristics of the proposed junctionless s-Si device are improved by increasing in the t_{ox2}, m, and positive N_f in the below threshold region, and vice-versa in above threshold voltage region. Also, better analog/RF electrical characteristics of the proposed TMGS-GCDG-JL s-Si MOSFET are obtained when compared to GS graded channel DG junctionless (GS-GCDG-JL) s-Si MOSFET.

2 Proposed MOSFET structure and TCAD setup

The simulated cross sectional view of TMGS-GCDG-JL s-Si device with fixed charges is demonstrated in Fig. 1(a). The strained-silicon graded channel region is doped with three different uniform phosphorous doping concentrations (i.e., N_{d1}, N_{d2}, and N_{d3}). Screen and control gates are used together to form bottom and top gates of TMGS-GCDG-JL s-Si device. The bottom and top gates of the GS-GCDG-JL s-Si MOSFET has a single gate layer whose work function is an average of ϕ_{m1}, ϕ_{m2} and ϕ_{m3}. Because of HCEs in nano scaled proposed s-Si junctionless MOSFET, interface charges are created at s-Si/SiO_2 interface and are represented as damaged region of length L_d, as demonstrated in Fig. 1(a). The drain current of s-Si MOSFET is calibrated with the transfer characteristics of the strained-silicon MOSFET using TCAD [23], as shown in Fig. 1(b). It is obvious from Fig. 1(b) that the TCAD simulation results of strained-silicon MOSFET are in good accordance with the experimental results shown in [23]. The various parameters and dimensions of the proposed TMGS-GCDG-JL s-Si MOSFET are used in the simulation are listed in Table 1.

Since the strain is developed into silicon channel, the energy-band diagram of the silicon material is affected because of the biaxial-tension. Thereby, energy band gap of silicon and effective mass of the carriers decrease, whereas electron affinity (χ_{Si}) increases. The changes in energy band gap, electron affinity, and effective masses of carrier in s-Si material are formulated as shown below [24,25]

$$(\Delta E_c)_{s-Si} = 0.57X, \qquad (\Delta E_g)_{s-Si} = 0.4X$$

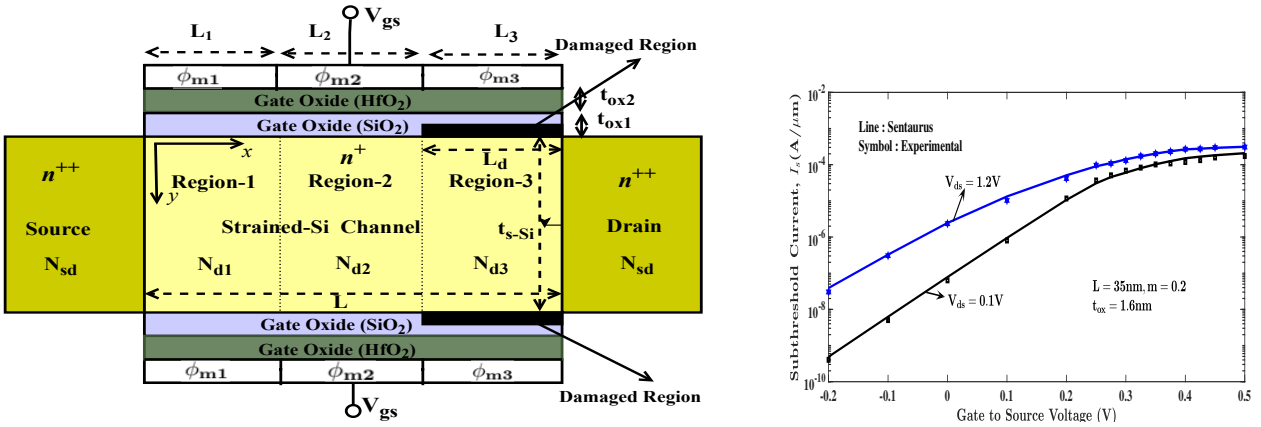
$$V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) = V_T \ln\left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}}\right)^{\frac{3}{2}} \approx 0.075X$$

where V_T denotes the thermal voltage, $N_{V,Si}$ and $N_{V,s-Si}$ represent density of states in the valence band, $m^*_{h,Si}$ and $m^*_{h,s-Si}$ denote the effective masses of hole in silicon and strained-silicon, respectively. Also, both flat band voltage and barrier potential of the source (drain) to channel decrease simultaneously [26].

$$\Delta V_{fb} = -\frac{E_c}{q} + \frac{E_g}{q} - V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$$
$$\Delta V_{bi} = V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) - \frac{E_g}{q}$$

where ΔV_{fb} and ΔV_{bi} are the changes in flat band voltage and built-in potential, respectively.

The proposed device with the fixed charges is simulated using the TCAD [27]. In the device simulation, to evaluate the analog/RF characteristics of the TMGS-GCDG-JL s-Si deice with fixed charges, the following physical models are considered. The charge transport mechanism is estimated with the help of the drift diffusion model and the recombination of carriers are determined by using Auger and SRH recombination models. And also, mobility of carriers is estimated by us-



(a) (b)

Fig. 1: Symmetrical TMGS-GCDG-JL s-Si MOSFET fixed charges a. Proposed junctionless MOSFET structure b. Comparison of strained-silicon MOSFET with experimental results of the [23].

Table 1: Parameters are employed in the simulation of TMGS-GCDG-JL s-Si MOSFET

S. No.	Variable	Symbol	Values
1	strained-silicon channel length	L	15 nm
2	strained-silicon channel doping	N_{d1}, N_{d2}, N_{d3}	10^{18}, 5×10^{17}, 10^{17} cm^{-3}
3	Source (Drain) doping	N_{sd}	10^{20} cm^{-3}
4	strained-silicon thickness	t_{s-Si}	6 nm
5	Oxide thicknesses	t_{ox1}, t_{ox2}	0.6, 1 nm
6	Work function of the control gate and screen gate	$\phi_{m1}, \phi_{m2}, \phi_{m3}$	4.8, 4.6, 4.4 eV
7	Gate to source voltage	V_{gs}	0 - 1 V
8	Drain to source voltage	V_{ds}	0 - 1 V
9	Ge mole fraction	m	0.1 - 0.3
10	Fixed charges	N_f	-4×10^{12} - 4×10^{12} cm^{-2}
11	Operating frequency	f_0	0.1 - 1000 GHz

ing Enormal mobility model and high field saturation model. Moreover, the energy band gap narrowing effects are considered by the OldSlotboom model and strained-silicon characteristics are assessed by MoleFraction model. Furthermore, the effect of fixed charges at SiO_2/s-Si interface of the device are included with the help of Traps model and quantum mechanical effects are also assessed with the help of density gradient model [28].

3 Result analysis

This section demonstrates the analog and radio frequency performance of the TMGS-GCDG-JL s-Si MOSFET with fixed charges using the simulation results obtained from TCAD. Fig. 2 depicts the effects of m on the g_m and transfer characteristics of TMGS-GCDG-JL s-Si device. It is noticed from the Fig. 2 that the GS-GCDG-JL s-Si device has enhanced transport characteristics and g_m compared to proposed TMGS-GCDG-JL s-Si device because of the lower threshold voltage of GS-GCDG-JL s-Si device. Moreover, increment in both ON current and g_m of the TMGS-GCDG-JL s-Si device are observed in subthreshold region by increasing the m because of decrease in the threshold voltage.

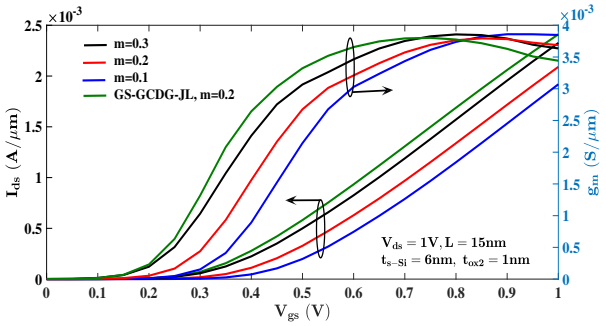


Fig. 2: Effect of strain in silicon channel on the transfer characteristics and g_m of the TMGS-GCDG-JL s-Si device.

The variation of t_{ox2} on g_m and transfer characteristics of TMGS-GCDG-JL s-Si MOSFET is shown in Fig. 3. When t_{ox2} decreases, increment in both g_m and transfer characteristics of MOSFET are observed in the above threshold region because of the greater gate control over the s-Si channel than drain and reverse trend follows in weak inversion region. Besides, the gate stack that consists of HfO_2 in the TMGS-GCDG-JL s-Si MOSFET has better g_m and transfer characteristics

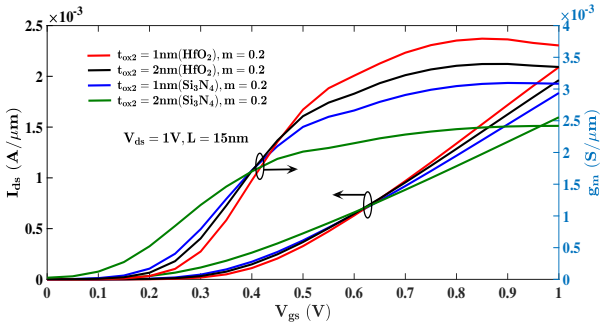


Fig. 3: Variation of t_{ox2} on the g_m and transfer characteristics of the TMGS-GCDG-JL s-Si MOSFET.

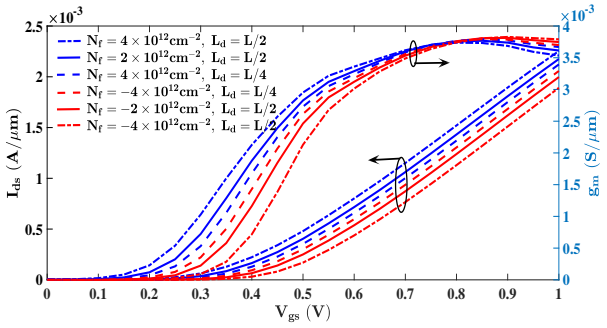


Fig. 4: Variation of N_f on the transfer characteristics and g_m of TMGS-GCDG-JL s-Si device.

than the gate stack that consists of Si_3N_4 in the above threshold region and inversely in subthreshold region.

The variation of N_f with L_d on the transfer characteristics and g_m of the proposed TMGS-GCDG-JL s-Si MOSFET is depicted in Fig. 4. The enhanced transfer characteristics of the TMGS-GCDG-JL s-Si device are attained by increasing positive N_f since the threshold voltage of device decreases, and reverse trend follows for the negative N_f. Moreover, as positive/negative fixed charge density increases, the transconductance of TMGS-GCDG-JL s-Si MOSFET increases in sub-threshold region and reverse trend follows in strong inversion region. Hence, the analog/RF characteristics of the proposed TMGS-GCDG-JL s-Si MOSFET are affected with respect to the fixed charges at SiO_2/s-Si interface.

Fig. 5 depicts the variation of m on the output characteristics and g_d of TMGS-GCDG-JL s-Si MOSFET. As strain increases, better drain characteristics and high g_d of the TMGS-GCDG-JL s-Si MOSFET are attained because of decrease in the threshold voltage of proposed MOSFET. It is evident from Fig. 5 that the GS-GCDG-JL s-Si device has enhanced drain characteristics and higher g_d compared to the proposed TMGS-GCDG-JL s-Si MOSFET. Therefore, the proposed TMGS-GCDG-JL s-Si MOSFET has lower effect of drain to source voltage on the channel compared to the GS-GCDG-JL s-Si MOSFET.

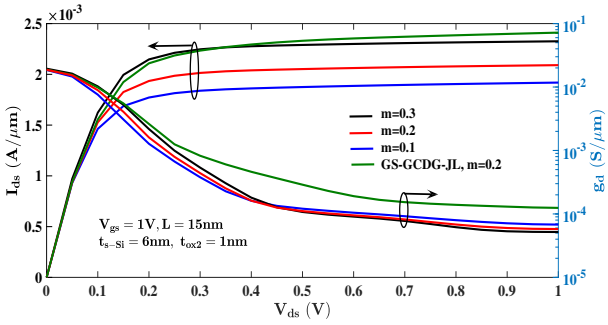


Fig. 5: Effect of m on the drain characteristics and output conductance of TMGS-GCDG-JL s-Si device.

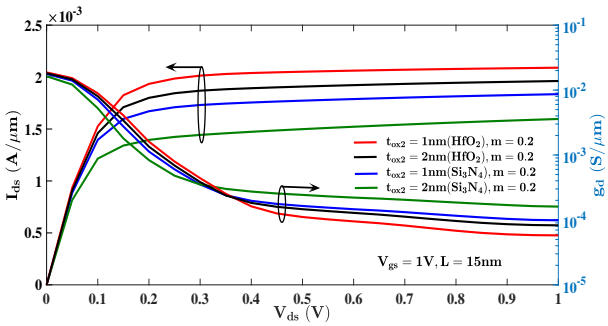


Fig. 6: Variation of t_{ox2} on the drain characteristics and g_d of TMGS-GCDG-JL s-Si device.

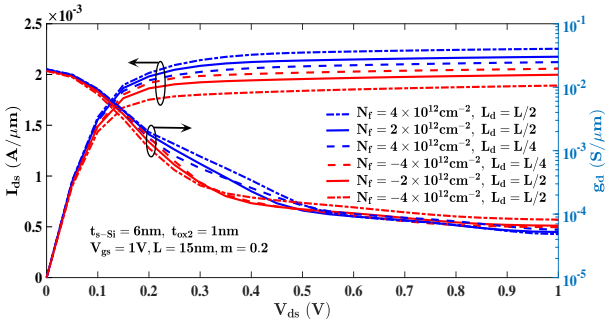


Fig. 7: Variation of N_f with L_d on output characteristics and g_d of TMGS-GCDG-JL s-Si MOSFET.

The variation of t_{ox2} on output characteristics and g_d of the TMGS-GCDG-JL s-Si MOSFET is illustrated in Fig. 6. As t_{ox2} decreases, g_d decreases and the proposed MOSFET achieves better drain characteristics. Besides, the gate stack that consists of HfO_2 in the TMGS-GCDG-JL s-Si MOSFET has improved drive current and less g_d than the gate stack that consists of Si_3N_4. Therefore, HfO_2/SiO_2 gate stack of proposed TMGS-GCDG-JL s-Si has better electrical characteristics and less impact of V_{ds} on the channel when compared to the Si_3N_4/SiO_2 gate stack, as shown in Fig. 6.

Fig. 7 illustrates the effect of N_f with L_d on output characteristics and g_d of the TMGS-GCDG-JL s-

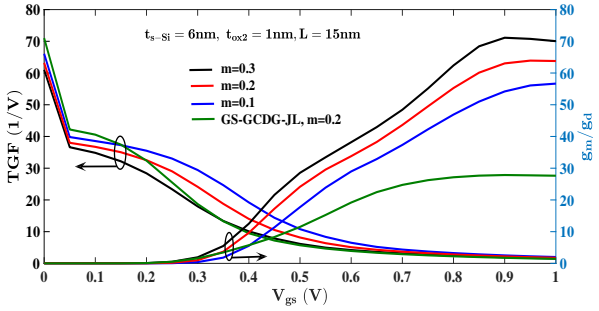


Fig. 8: Effect of m on the intrinsic voltage gain and TGF of TMGS-GCDG-JL s-Si device.

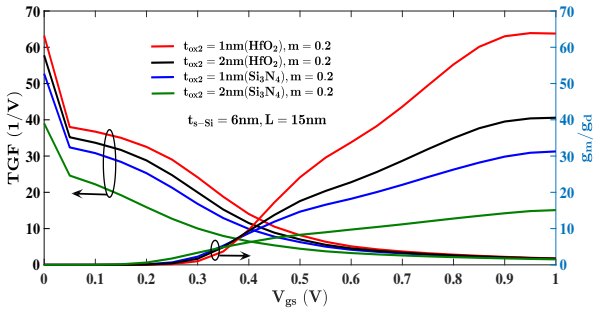


Fig. 9: Variation of t_{ox2} on the intrinsic voltage gain and TGF of TMGS-GCDG-JL s-Si device.

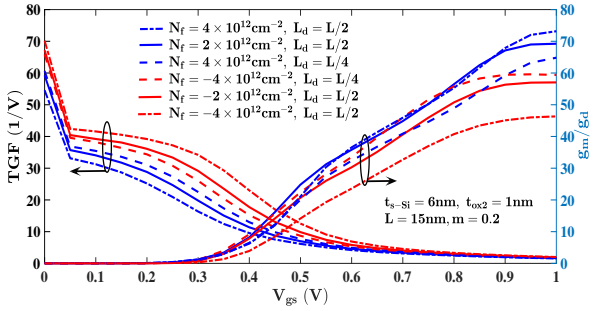


Fig. 10: Variation of N_f on the intrinsic voltage gain and TGF of the TMGS-GCDG-JL s-Si device.

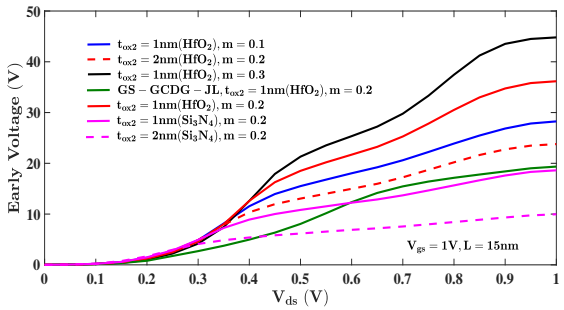


Fig. 11: Variations of t_{ox2} and m on the early voltage of TMGS-GCDG-JL s-Si device

Si MOSFET. Increase in output characteristics is observed by increasing the positive N_f owing to reduced threshold voltage of device, and vice-versa when N_f is negative. Moreover, as positive N_f increases, g_d of proposed device decreases, and vice-versa when N_f is negative. Therefore, the proposed TMGS-GCDG-JL s-Si MOSFET with positive N_f has lower impact of V_{ds} on the channel compared to the GS-GCDG-JL s-Si MOSFET with negative N_f.

The variation of strain on TGF and intrinsic gain of TMGS-GCDG-JL s-Si is depicted in Fig. 8. As strain increases in the TMGS-GCDG-JL s-Si MOSFET, TGF decreases and intrinsic voltage gain increases owing to increasing the values of transconductance and drain current of the proposed device, as depicts in Fig. 2. When compared to GS-GCDG-JL s-Si device, TMGS-GCDG-JL s-Si device has better TGF and higher $\frac{g_m}{g_d}$ due to high g_m and low g_d of the TMGS-GCDG-JL s-Si device, as illustrated in Fig. 2 and Fig. 5. Thereby, the proposed device has higher analog voltage gain and superior power efficiency due to TMG structure when compared to GS-GCDG-JL s-Si device.

Fig. 9 plots the effect of t_{ox2} on the voltage gain and TGF of the TMGS-GCDG-JL s-Si MOSFET. The power conversion efficiency and voltage gain of proposed MOSFET decrease because of the less gate control over the strained-Si channel than drain terminal as t_{ox2} increases. Moreover, gate stack with HfO_2 has better TGF and higher voltage gain than the gate stack with Si_3N_4 of the TMGS-GCDG-JL s-Si MOSFET due to the higher g_m and lower g_d of the TMGS-GCDG-JL s-Si MOSFET, as illustrated in Fig. 3 and Fig. 6. Therefore, the proposed MOSFET with Si_3N_4 has higher analog intrinsic gain and low power consumption are obtained.

The effect of N_f on the intrinsic voltage gain and TGF of the TMGS-GCDG-JL s-Si device is shown in Fig. 10. As positive N_f increases, TGF decreases and intrinsic voltage gain increases owing to the decrease in threshold voltage of TMGS-GCDG-JL s-Si MOSFET, and vice-versa for negative fixed charge density. Hence, the TMGS-GCDG-JL s-Si MOSFET with negative fixed charge density can be operated at lower bias values, and vice-versa for positive N_f. Moreover, the proposed MOSFET with positive N_f has higher analog intrinsic gain is attained.

Fig. 11 shows the variations of m and t_{ox2} on the early voltage of TMGS-GCDG-JL s-Si device. The early voltage of the TMGS-GCDG-JL s-Si MOSFET increases as m increases and t_{ox2} decreases since the g_d of the device decreases, as illustrated in Fig. 5 and Fig. 6 (low early voltage denotes the high channel length modulation effect in the MOSFET). Besides, gate stack with HfO_2 has greater early voltage than the gate stack with

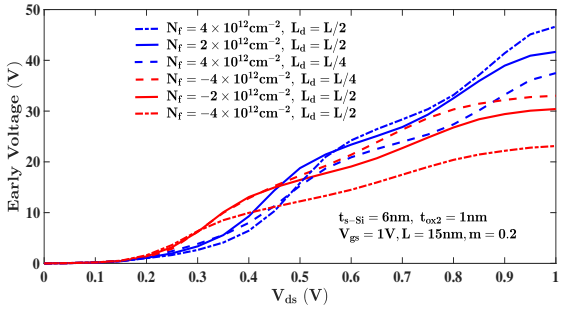


Fig. 12: Variation of the N_f on the early voltage of TMGS-GCDG-JL s-Si device.

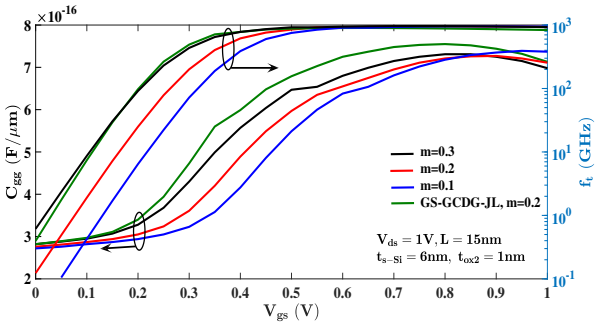


Fig. 13: Effect of the strain on the gate capacitance and f_t of TMGS-GCDG-JL s-Si device.

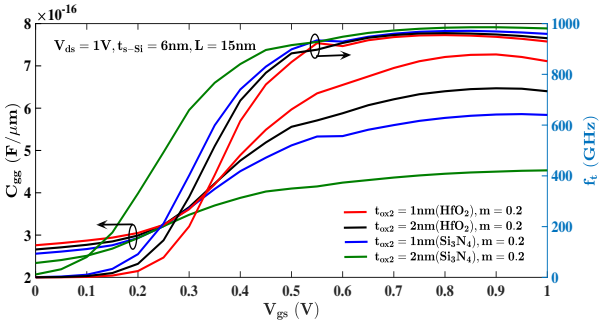


Fig. 14: Variation of t_{ox2} on gate capacitance and f_t of TMGS-GCDG-JL s-Si MOSFET.

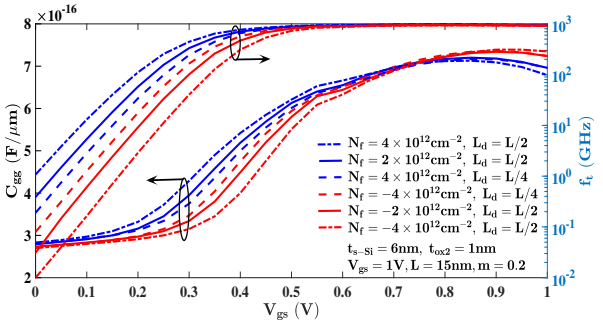


Fig. 15: Variation of N_f on the f_t and gate capacitance of TMGS-GCDG-JL s-Si device.

Si_3N_4 of the TMGS-GCDG-JL s-Si MOSFET since the output conductance for gate stack with HfO_2 is less, as depicts in Fig. 6. Moreover, the proposed TMGS-GCDG-JL s-Si MOSFET has higher early voltage than the GS-GCDG-JL s-Si MOSFET due to the less output conductance of the proposed device, as depicts in Fig. 5. As a result, the effect of channel length modulation in proposed TMGS-GCDG-JL s-Si MOSFET is less compared to the GS-GCDG-JL s-Si MOSFET.

Fig. 12 demonstrates the effect of N_f on early voltage of the TMGS-GCDG-JL s-Si MOSFET. The early voltage of the proposed device decreases/increases by increasing the negative/positive fixed charge density due to a increment/decrement in the output conductance with respect to negative/positive N_f, as demonstrated in Fig. 7. Hence, effect of channel length modulation in the device increases/decreases due to negative/positive fixed N_f at s-Si/oxide interface.

Fig. 13 demonstrates the effect of m on f_t and total gate capacitance of the TMGS-GCDG-JL s-Si MOSFET. As m decreases, the f_t and gate capacitance of the TMGS-GCDG-JL s-Si MOSFET decrease owing to an increment in the flat-band voltage of TMGS-GCDG-JL s-Si device and reduction of inversion carriers in strained-silicon channel. Moreover, when compared to proposed TMGS-GCDG-JL s-Si device, the gate capacitance and f_t of the GS-GCDG-JL s-Si MOSFET are higher due to the higher g_m of the GS-GCDG-JL s-Si device, as shown in Fig. 2.

The variation of t_{ox2} on the f_t and gate capacitance of the TMGS-GCDG-JL s-Si device is depicted in Fig. 14. As t_{ox2} decreases, higher C_{gg} and lower f_t of the TMGS-GCDG-JL s-Si MOSFET are obtained due to the increase in inversion carriers in the channel. Besides, the gate stack with HfO_2 has higher gate capacitance than the gate stack with Si_3N_4 of the TMGS-GCDG-JL s-Si MOSFET due to the higher permittivity of HfO_2. However, the gate stack with HfO_2 has less f_t than the gate stack with Si_3N_4 of the TMGS-GCDG-JL s-Si MOSFET is noticed.

Fig. 15 shows the effect of fixed charged density on the gate capacitance and f_t of the TMGS-GCDG-JL s-Si device. As negative N_f increases, gate capacitance of the TMGS-GCDG-JL s-Si MOSFET decreases due to mitigate of inversion charges in channel of MOSFET, and reverse trend follows for positive N_f. Moreover, as negative/positive N_f increases, f_t of the TMGS-GCDG-JL s-Si device decreases/increases because of the decrement/increment in g_m of TMGS-GCDG-JL s-Si MOSFET with negative/positive N_f, as demonstrated in Fig. 4.

Fig. 16 shows the variation of t_{ox2} on the voltage gain of the TMGS-GCDG-JL s-Si MOSFET with the operating frequency. As seen in Fig. 16, as t_{ox2} de-

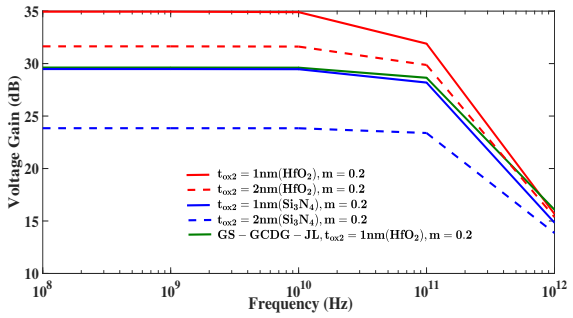


Fig. 16: variation of the t_{ox2} on the voltage gain of the TMGS-GCDG-JL s-Si device along operating frequency.

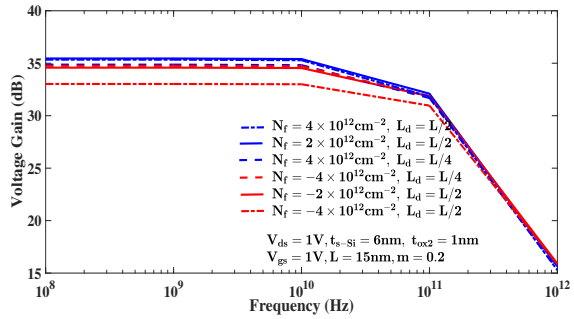


Fig. 17: Variation of N_f on the voltage gain of TMGS-GCDG-JL s-Si device along operating frequency.

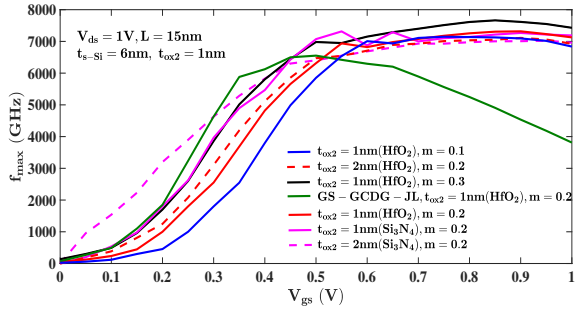


Fig. 18: Variations of strain and t_{ox2} on f_{max} of the TMGS-GCDG-JL s-Si MOSFET.

creases, voltage gain of TMGS-GCDG-JL s-Si device increases because of decrement in g_d and increment in g_m, as shown in Fig. 2 and Fig. 5. Moreover, gate stack with HfO_2 has higher voltage gain than the gate stack with Si_3N_4 of the TMGS-GCDG-JL s-Si MOSFET. However, as operating frequency increases, voltage gain of proposed MOSFET decreases owing to the more parasitic capacitive effects. Also, the proposed TMGS-GCDG-JL s-Si MOSFET has greater voltage gain than GS-GCDG-JL s-Si device because of the TMG structure in the proposed device. Fig. 17 depicts the effect of fixed charge density on the voltage gain of the TMGS-GCDG-JL s-Si MOSFET. As positive/negative

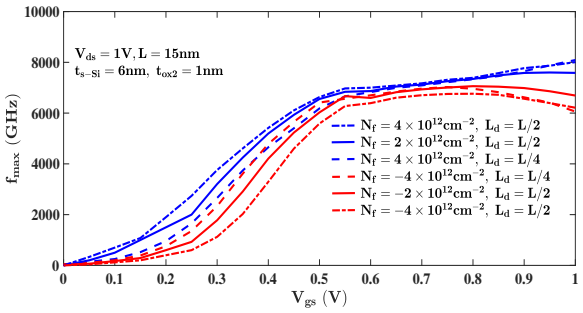


Fig. 19: Variation of N_f on f_{max} of the TMGS-GCDG-JL s-Si MOSFET.

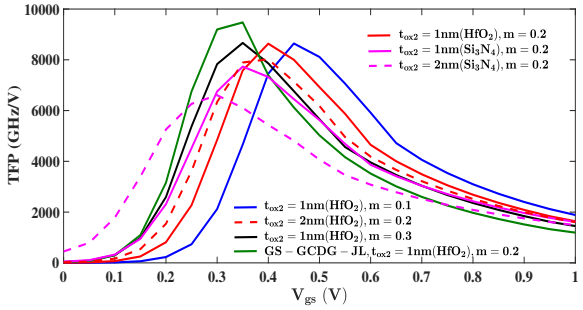


Fig. 20: Variations of the m and t_{ox2} on the TFP of TMGS-GCDG-JL s-Si device.

N_f increases, voltage gain of TMGS-GCDG-JL s-Si device increases/decreases owing to increment in g_m and decrement in g_d, as shown in Fig. 4 and Fig. 7.

The variations of m and t_{ox2} on f_{max} of the TMGS-GCDG-JL s-Si MOSFET are shown in Fig. 18. Since m increases and t_{ox2} decreases, f_{max} of the TMGS-GCDG-JL s-Si MOSFET increases because of higher g_m of proposed MOSFET, as shown in Fig. 2 and Fig.3. Besides, higher f_{max} is attained for the HfO_2/SiO_2 gate stack in comparison with the Si_3N_4/SiO_2 gate stack of the TMGS-GCDG-JL s-Si device since higher g_m of proposed MOSFET, as shown in Fig. 4. Moreover, the TMGS-GCDG-JL s-Si MOSFET has higher f_{max} in comparison with the GS-GCDG-JL s-Si device. The effect of N_f on f_{max} of the TMGS-GCDG-JL s-Si device is illustrated in Fig. 19. It is evident from Fig. 19 that the increment/decrement in f_{max} of the TMGS-GCDG-JL s-Si MOSFET is obtained as positive/negative N_f increases with damaged length since higher/lower g_m of proposed MOSFET with positive/negative N_f at s-Si/oxide interface, as shown in Fig. 4.

The variations of m and t_{ox2} on TFP of s-Si TMGS-GCDG-JL s-Si device are shown in Fig. 20. As seen from Fig. 20, it is evident that the TFP of the proposed MOSFET is improved by decreasing the values of m and t_{ox2} in the above threshold voltage region and reverse trend follows in weak inversion region. Be-

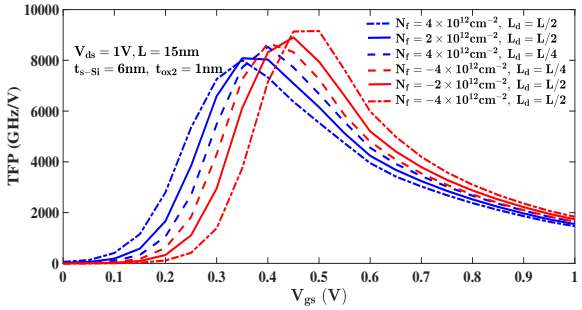


Fig. 21: Variation of the N_f on TFP of TMGS-GCDG-JL s-Si MOSFET.

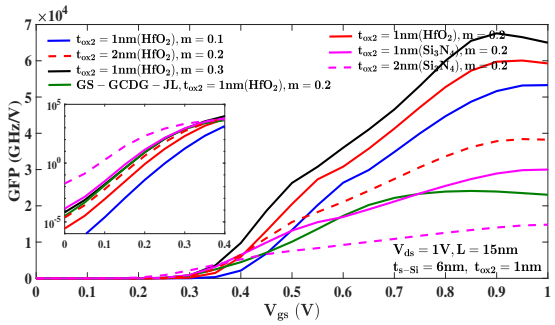


Fig. 22: Variations of m and t_{ox2} on the GFP of the TMGS-GCDG-JL s-Si MOSFET.

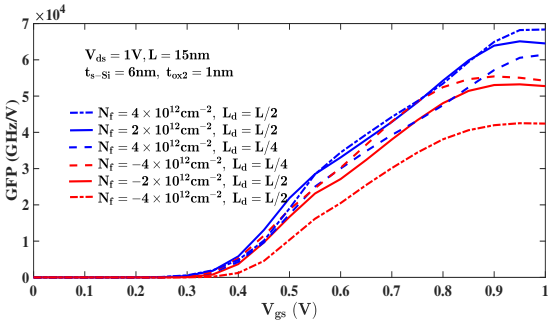


Fig. 23: Variation of the N_f the TFP of TMGS-GCDG-JL s-Si MOSFET.

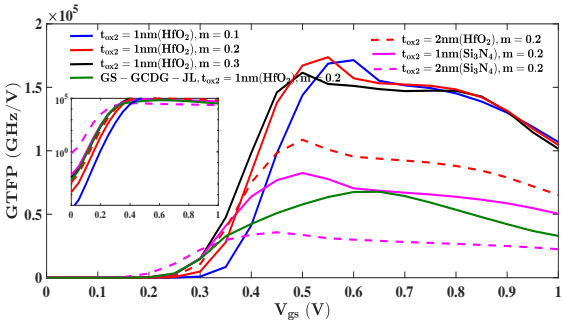


Fig. 24: Variations of m and t_{ox2} on the GTFP of the TMGS-GCDG-JL s-Si MOSFET.

sides, better TFP is obtained for the HfO_2/SiO_2 gate stack in comparison with the Si_3N_4/SiO_2 gate stack of the TMGS-GCDG-JL s-Si MOSFET. Also, TFP of the proposed TMGS-GCDG-JL s-Si MOSFET is more than the GS-GCDG-JL s-Si MOSFET in above sub-threshold region, and reverse trend follows in weak inversion region. The effect of fixed charge density on the TFP of the TMGS-GCDG-JL s-Si MOSFET is shown in Fig. 21. TFP of the TMGS-GCDG-JL s-Si device decreases/increases as positive/negative N_f increases in the strong inversion region, and reverse trend follows in weak inversion region.

Fig. 22 The variations of t_{ox2} and m on the GFP of TMGS-GCDG-JL s-Si device are depicted in Fig. 22. GFP of the TMGS-GCDG-JL s-Si MOSFET decreases as strain and t_{ox2} increase in the above threshold region, and reverse trend follows in weak inversion region. Moreover, enhanced GFP is obtained for the HfO_2/SiO_2 gate stack in comparison with the Si_3N_4/SiO_2 gate stack of the TMGS-GCDG-JL s-Si MOSFET. Besides, the proposed TMGS-GCDG-JL s-Si MOSFET achieves higher GFP than the GS-GCDG-JL s-Si device in the above threshold voltage region, and reverse trend follows in weak inversion region. The variation of fixed charge density on GFP of the TMGS-GCDG-JL s-Si device is depicted in Fig. 23. As negative (positive) interface charge density increases, GFP of the TMGS-GCDG-JL s-Si MOSFET decreases (increases).

The variations of m and t_{ox2} on GTFP of the TMGS-GCDG-JL s-Si MOSFET are depicted in Fig. 24. The GTFP of the TMGS-GCDG-JL s-Si MOSFET is increased by decreasing strain and t_{ox2} in above threshold region, and reverse trend follows in weak inversion region. Besides, HfO_2/SiO_2 gate-stack has greater GTFP when compared to Si_3N_4/SiO_2 gate stack of the TMGS-GCDG-JL s-Si MOSFET. Moreover, it is obvious from Fig. 24 that the proposed device has improved overall figure of merit compared to the the GS-GCDG-JL s-Si device in the above threshold region.

Fig. 25 plots the variation of N_f on GTFP of TMGS-GCDG-JL s-Si device. For a given L_d, when $4 \times 10^{12} \leq N_f \leq -2 \times 10^{12}$, it is observed that GTFP of TMGS-GCDG-JL s-Si MOSFET increases/decreases as positive/negative interface charge density increases in the sub-threshold region and reverse trend follows in above threshold region. Besides, GTFP of the TMGS-GCDG-JL s-Si device reduces because of DIBL effect when $N_f > -2 \times 10^{12}$. Hence, the overall analog/RF performance of the proposed the TMGS-GCDG-JL s-Si MOSFET varies with respect to fixed charges.

The performance analysis of proposed TMGS-GCDG-JL s-Si MOSFET is compared with existing works in the previous works, as demonstrated in Table 2. The

Table 2: The performance analysis of TMGS-GCDG-JL s-Si MOSFET with literature.

Device	$\mathbf{g_m}$**, S/**μ**m**	$\left(\frac{I_d}{g_d}\right)$**, V**	$\left(\frac{g_m}{I_d}\right)$**,** $\mathbf{V^{-1}}$	$\frac{g_m}{g_d}$	$\mathbf{C_{gg}}$**, fF/**μ**m**	$\mathbf{f_t}$**, GHz**	**GTFP, (THz/V)**
GS-GCDG-JL s-Si	3.8	19.35	71.01	27.85	0.755	900.2	67.71
TMGS-GCDG-JL s-Si	3.79	36.17	63.23	63.91	0.727	954.6	173.7
High-k DG-JL [14]	2.1	50.1	40.1	60.1	1.5	250	–
DG-JL [19]	0.26	1.28	26.7	33.88	0.4	139	–
GC DG-JL [20]	2.0	14.3	11.5	43.0	0.6	580	–
s-Si GC-DMDG [29]	3.9	11.2	33.26	22.59	0.924	787	54.13

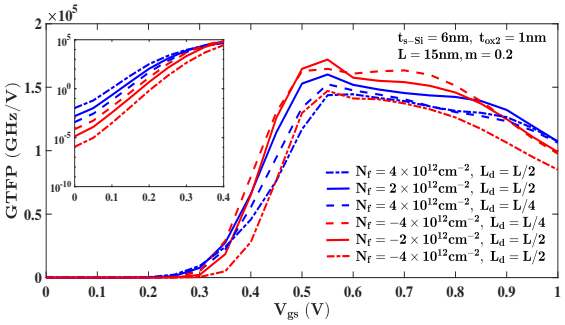


Fig. 25: Variation of N_f on the GTFP of the TMGS-GCDG-JL s-Si device.

voltage gain, f_t, and GTFP of proposed TMGS-GCDG-JL s-Si MOSFET (m=0.2 and t_{ox2}= 1nm) are better than when compared to the GS-GCDG-JL s-Si MOSFET (m=0.2 and t_{ox2}= 1nm), high-k spacer DG junctionless MOSFET [14], DG junctionless MOSFET with channel length 20 nm [19], GC DG junctionless device with channel length 30 nm [20] and strained-Si GC-DMDG MOSFET with channel length 20 nm [29]. However, the proposed TMGS-GCDG-JL s-Si MOSFET has lower early voltage than high-k spacer DG junctionless MOSFET [14]. Moreover, the proposed TMGS-GCDG-JL s-Si MOSFET has lower g_m than strained-Si GC-DMDG MOSFET with channel length 20 nm [29]. Therefore, the proposed MOSFET using the TMG with GC engineering and gate stack techniques achieves improved overall analog/RF performance.

4 Conclusion

The analog/radio-frequency performance of the proposed TMGS-GCDG-JL s-Si MOSFET with fixed charge density at silicon dioxide interface has been estimated using TCAD tool. The proposed TMGS-GCDG-JL s-Si MOSFET has better overall analog/RF figure of merit compared to GS-GCDG-JL s-Si device in the above threshold region. Moreover, the analog/radio frequency figure of merits of TMGS-GCDG-JL s-Si device are improved by employing the TMG structure with the GC engineering and gate stack technique. An exhaustive analysis has been done to investigate the various analog/RF characteristics by varying MOSFET parameters of the TMGS-GCDG-JL s-Si MOSFET. Increments in TFP and GTFP of proposed TMGS-GCDG-JL s-Si MOSFET have been obtained by increasing values of strain, positive fixed charge density, and t_{ox2} in the weak inversion region, and vice-versa in the above threshold voltage region. Therefore, the proposed TMGS-GCDG-JL s-Si MOSFET has better analog/radio-frequency figure of merits in above the threshold voltage region.

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Data availability: The data that support the findings of this study are available from the corresponding author, upon reasonable request.

Compliance with Ethical Standards

Consent for Publication: All the authors declare their consent to transfer the publication rights to the journal in which this manuscript is submitted.

Consent to Participate: Not Applicable

Conflicts of interest: The authors declare that there is no conflict of interests.

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