An Energy Efficient Quantum-dot Cellular Automata Design of 1/2 and 1/3 Convolution Encoder

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An Energy Efficient Quantum-dot Cellular Automata Design of 1/2 and 1/3 Convolution Encoder

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Abstract: Quantum-dot cellular automata (QCA) technology is considered to be the future of nanoelectronic device fabrication technology. The fabrication density of the transistors in a particular area in the current nanoelectronic industry has saturated. Adroit alternate to current CMOS based VLSI technology is being researched upon. QCA technology is considered to be the noblest post-CMOS era fabrication technology. In this paper, novel energy-efficient QCA designs for 1/2 and 1/3 convolution encoders have been presented. Both the presented designs were proven to be efficient than previously designed circuits. The efficiency of the design is calculated for critical design parameters like cell count, cell area, latency (clock phases), complexity and energy dissipation. The proposed 1/2 convolution encoder uses 21 QCA cells consuming an area of $0.012\mu m^2$. The complexity of this design was calculated to be 2. The energy dissipation analysis revealed that the presented circuit dissipated $14.03meV$ of energy. The proposed 1/3 convolution encoder uses 32 QCA cells consuming an area of $0.025\mu m^2$. The energy dissipation analysis revealed that the presented circuit dissipated $16.88meV$ of energy. Both the proposed designs used only a few more extra cells than the previously designed circuits but induced stronger polarizations and were more fault-tolerant. It was found that the circuits proposed are 25% more energy efficient than previously designed circuits. The latency of the proposed designs was of 2 clock phases, thus making it suitable for high-speed operation. Significant improvement of the designs was done to optimize the circuit for secure nano-communication devices.

Keywords: Nanoelectronics, Convolution Encoder, Energy Dissipation, Fault tolerance, Latency, Nano-communication.

1. Introduction

Quantum-dot cellular automata (QCA), the technology considered to be a potent contender for the post-CMOS (Complementary metal oxide semiconductor) era fabrication technology [2]. QCA technology due to its astonishing features like reversibility, ultra-low-power application and high-speed operation, has become a hot topic for research since the saturation of Moore's law in recent years. In QCA technology, the circuits are designed using quantum dots (quantum bits or quantum cells). In these quantum-dot based logic circuits, there is no actual flow of current. Instead, QCA cells inhabit and propagate polarizations based on the position of electrons in the quantum wells. The information is passed on and processed using polarization propagation to the neighbouring cells [3]. Reversibility is one of the focal features of QCA technology. A reversible QCA circuit has the potential to dissipate information processing energy less than the Shannon-Von Neumann-Landauer (SNL) limit of $K_B T \ln(2)$. These circuits can be used for ultra-low-power operation [4 - 6]. Also, the QCA cells are of the size of $18 \times 18 \mu m^2$ therefore, they enable high packaging densities during chip manufacturing.

Extensive research has been done to propose more and more efficient reversible gates, adders, flip flops and memory circuits. Only a trivial amount of research was done on topics

related to communication engineering. Communication error check circuits like parity generators and detectors are some of the few circuits proposed in QCA technology [7, 9]. Channel encoding and decoding is a vital component of digital communication setup. In channel encoding, the information bits being sent upon are encoded to a unique codeword. This helps in securing the communication and provides error-free communication in an inherent noisy channel. During channel encoding, the transmitting bit sequence is converted into an alternate bit sequence called a codeword. Redundancy is introduced during the convolution of the input sequence of bits. Linear block codes and convolution codes are the two types of channel codes. Convolution codes depend both on the present input sequence and the previously transmitted sequence. Thus, a need for memory element in CMOS logic implementation was compulsory. In this paper, a new energy-efficient and fault-tolerant design of the 1/2 and 1/3 convolution encoder is proposed.

In section 2 we have provided a brief introduction to the various building blocks of the QCA technology. In section 3 prior related work was discussed and in section 4 our proposed work was depicted and explained. In section 5 a state of art comparative analysis was drawn between the proposed designs and the previously proposed circuits.

2. QCA Background

Quantum-dot cellular automata is considered to be a potential substitute to the current CMOS based VLSI technology. This technique was first put forward by C. Lent and P.D. Tougaw in 1993 [2]. In quantum-dot cellular automata, the circuits are designed using quantum cells instead of conventional CMOS gate implementation [10]. These cells are square-shaped having four quantum wells separated by quantum barriers. Two of the opposite quantum wells have electrons residing in them. There are two ways in which the electrons can reside in quantum cells. Since only two possible diagonal positions are allowed, they result in two possible polarization (P). These two polarizations are used to depict two states in computation i.e., Logic 1 and Logic 0. The following subsections give an understanding of the basic concepts of QCA technology [11, 12].

2.1. The QCA cell

Quantum-dots are arranged in unique ways to develop QCA designs. These quantum cells propagate the polarization instead of current like in current CMOS technology. The quantum cells work mainly on two fundamental concepts; the bi-stability of cell and the effect of the polarization of neighbouring cells. The electrons reside in the opposite quantum wells to minimize the coulombic interaction. These electrons can only crossover to another set of quantum well only when supplied with enough tunnelling energy [3, 11]. This tunnelling energy is called kink energy. The bistable nature of the quantum cells results in two possible polarizations representing two logic states (0 and 1). Fig. 1 shows the two states of the QCA cell.

Fig. 1 Two possible logic states of a QCA cell

If electrons reside in quantum well 1 and 3, it is considered to be Logic 0 and polarization is said to be $P = -1$. On the other hand, if the electrons reside in quantum well 2 and 4, it is considered to be Logic 1 and the polarization is said to be $P = +1$ [13]. The polarization can be calculated from the following formula;

$$P = \frac{(p_1 + p_3) - (p_2 + p_4)}{p_1 + p_2 + p_3 + p_4} \quad (1)$$

Here, p_i denotes the electronic charge at the i^{th} quantum cell. The area between quantum wells stops the electrons from tunnelling from one quantum well to another and act as barriers. These barriers can only be overcome using sufficient clocking energy [14, 15]. Based on the position of quantum wells in a QCA cell, it can be categorized into two types: 90° cell and 45° cell.

2.1.1. The 90° Cell

In 90° cells the quantum wells are situated at the four corners of the square cell. The electrons at all times reside in the diagonally opposite quantum wells to reduce the coulombic repulsion. It is the most commonly used QCA cell type used in designing logic circuits. Fig. 2 depicts the 90° QCA cell.

Fig. 2 Two possible states of 90° QCA cell

2.1.2. The 45° Cell

In a 45° QCA cell, the quantum wells are located at the midpoints of the four sides of the square cell. This type of cell is also called a rotated QCA cell. In this type of QCA cell, the electrons are located on the opposite quantum wells. Fig. 3 shows a 45° QCA cell.

Fig. 3 Two possible states of 45° QCA cell

2.2. Inter Cellular Interaction

The input at a particular cell is given by fixing the electron positions in two out of four quantum wells. The input cell then polarizes the cells surrounding it. Therefore, the data is propagated by the propagation of polarization. The electron interaction within a cell is given by;

$$E_{i,j} = \frac{Q_i \times Q_j}{4\pi \epsilon_0 \epsilon_r |R_i - R_j|} \quad (2)$$

The influence on a particular cell under the influence of many other cells is given by the summation of the individual polarization influences of the cells surrounding it. It can be mathematically represented as;

$$E = \sum \frac{Q_i \times Q_j}{4\pi \epsilon_0 \epsilon_r R_{ij}}, i \neq j \quad (3)$$

Here, Q_i and Q_j are the charges, ϵ_r is the relative permittivity, R_{ij} is the distance between the charges and ϵ_0 is the vacuum permittivity.

2.3. Clocking in QCA

The flow of information in QCA cell designs is regulated by the clocking. Meta-states in design are avoided using necessary power gain through clocking. Also, synchronization in the data flow can be maintained using clocking schemes. Quantum energy barriers between the quantum cells are managed using the QCA clock. Using the QCA clock the electrons are energized enough to tunnel to other quantum dots [14, 15]. There are four phases to QCA clocking:

1. *Switch Phase*: During this phase, the energy barriers are raised thus the cells attain definite polarization.
2. *Hold Phase*: During the hold phase, the potential barriers are held at a higher value and proscribe electrons from tunnelling. The cells retain the polarization induced during the switch phase.
3. *Release phase*: During the release phase, lowering of the energy barriers starts and the electrons are released from their confinement in quantum wells. The cells lose their polarization during this phase.
4. *Relax Phase*: During the relax phase, the complete lowering of energy barriers takes place and electrons are completely free from confined quantum wells. This phase accounts for the meta-state of the cell.

All these clocking phases have been depicted in Fig. 4.

Fig. 4 Clocking zones in QCA technology

2.4. Basic Building Blocks

There are two basic building blocks in QCA technology that are fundamental in designing the QCA layout for any given logic circuit. QCADesigner [16] simulation software is used to simulate the circuits.

2.4.1. Inverter:

NOT gate is the basic building block in developing any logic design. NOT gate simply inverts the input given to it. Fig. 5 depicts the QCA layout of the NOT gate.

Fig. 5 NOT gate design in QCA

2.4.2. Majority gate:

The output of the majority gate is simply what has more cardinality out of the three inputs. It can be simply modified to perform AND and OR logic function. Fig. 6 depicts the QCA layout of the Majority gate. Majority gate implements the function;

$$F(A,B,C) = AB+BC+CA$$

Fig. 6 Majority gate design in QCA

Here, IN1, IN2 and IN3 are the three inputs and OUT is the output of the majority gate.

3. Prior Work

Quantum-dot cellular automata based 1/2 and 1/3 convolution encoders were previously designed in Ref [17], Ref [18] and Ref [19]. In Ref [17], *Sen et al.* presented a QCA design of 1/2 convolution encoder using 304 QCA cells consuming a cell area of $0.0984\mu m^2$. The total area consumed by the design was $0.497\mu m^2$. The latency incurred in this design was of 3 clock cycles or 12 clock phases. Also, a 1/3 convolution encoder was proposed in this paper which consumed 307 QCA cells. The cell area used by this design was $0.10\mu m^2$ and the total area used was $0.697\mu m^2$. The latency incurred in this design was of 3 clock cycle or 12 clock phases. Both these designs were constructed using 12 majority gates and the complexity was calculated to be 18 for both the designs. No crossovers were used during designing of this circuit.

In Ref [18], *Bahar et al.* proposed efficient QCA designs of 1/2 and 1/3 convolution encoders. 30 cells were used in designing a 1/2 convolution encoder consuming a cell area of $0.021\mu m^2$ and a total area of $0.021\mu m^2$. The latency incurred in this design was 0.5 clock cycle or 2 clock phases. The complexity of this design was calculated to be 2. Similarly, the design for 1/3 convolution encoder was constructed using 44 QCA cells consuming a cell area of $0.027\mu m^2$ and a total area of $0.027\mu m^2$. The complexity of this design was calculated to be 3. No crossovers were used during designing of this circuit.

In Ref [19], *Suhaib et al.* proposed two different designs of 1/2 and 1/3 convolution encoder using two different techniques. For 1/2 convolution encoder, a cell count of 18 and 19 were used in the two different designs respectively. A total cell area consumption of $0.0058\mu m^2$ and $0.0062\mu m^2$ was used to propose two different designs. However, the latency of both the designs was 0.5 clock cycle or 2 clock phases. The two 1/3 convolution encoder designs were constructed using 30 and 40 QCA cells, consuming a cell area of $0.024\mu m^2$ and $0.035\mu m^2$ respectively. The latency incurred in both the designs was 0.5 clock cycle or 2 clock phases.

4. Proposed Work

The designs of the proposed 1/2 and 1/3 encoder with their corresponding simulation results are depicted in the below subsections respectively.

4.1. 1/2 Convolution Encoder

The design for the presented 1/2 convolution encoder is proposed by cascading two 2-input XOR gates. The proposed design can be seen in Fig. 7 and the simulated waveform verifying its working is shown in Fig. 8.

Fig. 7 Proposed design of 1/2 convolution encoder

Fig. 8 Simulated waveform of 1/2 convolution encoder

Here, a0, a1 and a2 are the three inputs and the c0 and c1 are the two convoluted outputs. Using only 21 cells and consuming only $0.018\mu m^2$ cell area this design is proposed. In this design, only 2 majority gates are used. A latency of two clock phases is incurred. There are no crossovers used in this design. The complexity of this design is calculated to be 2. Also, from the simulated waveform it can be concluded that the results obtained are in accordance with the desired outcomes and also within desired specifications.

4.2. 1/3 Convolution Encoder

The design for the presented 1/3 convolution encoder is proposed by cascading three 2-input XOR gates. The corresponding proposed design can be seen in Fig. 9 and the simulated waveform verifying its working is shown in Fig. 10.

Fig. 9 Proposed design of 1/3 convolution encoder

Fig. 10 Simulated waveform of 1/3 convolution encoder

Here, a0, a1, a2 and a3 are the four inputs and the c0, c1 and c2 are the three convoluted outputs. Using only 33 cells and consuming only $0.025\mu m^2$ cell area this design is proposed. In this design, only 3 majority gates are used. A latency of three clock phases is incurred. There are no crossovers used in this design. The complexity of this design is calculated to be 3. Also, from the simulated waveform it can be concluded that the results obtained are in accordance with the desired outcomes and also within desired specifications.

5. Power Dissipation Analysis

Energy and Power dissipation plays a pivotal role in determining the efficiency of any circuitry. The energy and power dissipation analysis in QCA is done using the QCAPro tool [20]. QCAPro tool uses Coherence Vector analysis for accurate time-dependent dynamic simulation. Coherence Vector Engine is based on the density matrix approach. The coherence vector is a vector representation of the cell density matrix [3].

The first model for QCA that was power and energy considerate was developed by Lent. in Ref [21]. The first step in determining the power is to determine the two states of the QCA cell and that is calculated using the Hamiltonian matrix shown below [21, 22];

$$H_i = \begin{bmatrix} -\frac{1}{2}P_j E_{i,j}^k & -\gamma \\ -\gamma & \frac{1}{2}P_j E_{i,j}^k \end{bmatrix} \quad (4)$$

Where, P_j tells us about the polarization of the cell j . $E_{i,j}^k$ is the Kink Energy between cell i and k . γ is the energy required for the electrons to tunnel within quantum cells. Then for each clock cycle, we need to calculate the QCA cell energy using eq. 2 [23];

$$E = \langle H \rangle = \frac{\hbar}{2} \cdot \vec{F} \cdot \vec{\lambda} \quad (5)$$

Where $\vec{F}$ is the energy environment vector of a cell considering its neighbour's effect on it. $\hbar$ is the Planks constant and $\vec{\lambda}$ represents the coherent vector.

$$\vec{F} = \frac{1}{\hbar} \left[-2\gamma, 0, \sum_{j \in s} P_j E_{i,j}^k \right] \quad (6)$$

$$E_{diss} = \frac{\hbar}{2} \int_{-L}^L \vec{F} \cdot \frac{\partial \lambda}{\partial t} dt \quad (7)$$

$$P_{diss} = \frac{E_{diss}}{\tau_{ss}} < \left(\frac{\hbar}{2\tau_{ss}} \vec{F}^+ \right) \times \left(-\vec{\Gamma}_N^+ \tanh\left(\frac{\hbar|\vec{F}^+|}{2k_B T}\right) + \vec{\Gamma}_N^- \tanh\left(\frac{\hbar|\vec{F}^-|}{2k_B T}\right) \right) \quad (8)$$

Only when the changing rate of $\vec{F}$ is maximum, maximum energy dissipation will occur [24]. Using equation 4 and 5 an approximate estimate of the energy and power dissipation can be easily calculated [25].

The energy dissipation maps for the proposed 1/2 and 1/3 convolution encoder are shown in Fig. 11 - 16, for three levels of Kink Energy at a constant temperature, $T = 2K$. A comparative analysis based on the energy dissipation can be seen in table 1.

Fig. 11 Energy dissipation map of 1/2 convolution encoder at $\gamma = 0.5E_k$

Fig. 12 Energy dissipation map of 1/3 convolution encoder at $\gamma = 0.5E_k$

Fig. 13 Energy dissipation map of 1/2 convolution encoder at $\gamma = 1.0E_k$

Fig. 14 Energy dissipation map of 1/3 convolution encoder at $\gamma = 1.0E_k$

Fig. 15 Energy dissipation map of 1/2 convolution encoder at $\gamma = 1.5E_k$

Fig. 16 Energy dissipation map of 1/3 convolution encoder at $\gamma = 1.5E_k$

6. State of Art Comparative Analysis

For a 1/2 convolution encoder, the design proposed by Ref [17] consumed a cell area of $0.0697\mu m^2$. Then in Ref [18] the proposed convolution encoder drastically reduced the cell area to just $0.021\mu m^2$ making an 85% increase in cell area efficiency. The design proposed in Ref [18] was however not fault-tolerant. In the design in Ref [19], the author proposed a fault-tolerant circuit but this resulted in a compromise with energy dissipation.

For a 1/3 convolution encoder, the design proposed by Ref [17] consumed a cell area of $0.0697\mu m^2$. Then in Ref [18] the proposed convolution encoder drastically reduced the cell area to just $0.027\mu m^2$ making an 80% increase in cell area efficiency. The design proposed in Ref [18] was however not fault-tolerant. In the design in Ref [19], the author proposed a fault-tolerant circuit but this resulted in a compromise with energy dissipation.

Table. 1 Comparative Analysis of 1/2 and 1/3 convolution encoder.

Designs	Cell count	Cell Area	Latency	N_M	N_I	N_C	Complexity ($N_M + N_I + N_C$)	Total energy dissipation (meV)		
								$0.5E_k$	$1.0E_k$	$1.5E_k$
1/2 [17]	304	0.697	3	12	6	0	18	305.08	417.38	494.42
1/2 [18]	30	0.021	0.5	2	0	0	2	32.72	48.48	66.17
1/2 [19]	18	0.016	0.5	2	0	0	2	15.02	24.19	29.45
1/2 [19]	19	0.013	0.5	2	0	0	2	15.16	24.85	35.81
Proposed 1/2	21	0.018	0.5	2	0	0	2	14.36	22.71	27.14
1/3 [17]	307	0.697	3	12	6	0	18	319.96	434.97	513.49
1/3 [18]	44	0.027	0.5	3	0	0	3	49.68	73.22	100.04
1/3 [19]	30	0.024	0.5	3	0	0	3	20.84	37.73	56.87
1/3 [19]	40	0.035	0.5	3	0	0	3	63.53	80.58	101.77
Proposed 1/3	32	0.025	3	3	0	0	3	16.88	30.20	51.94

N_M : Number of majority gates. N_I : Number of Inverters. N_C : Number of Crossovers

7. Conclusion

In this paper, the energy-efficient QCA design of the 1/2 and 1/3 convolution encoder is presented. The proposed design of the 1/2 convolution encoder is constructed using 21 quantum cells. The reported cell count of previously designed circuits is in the range of 19 – 304. But, due to various drawbacks like fault tolerance and high energy dissipation, these designs are not practically realizable. The proposed circuit is found to be 25% efficient in energy dissipation analysis. The proposed 1/3 convolution encoder is constructed using 32 quantum cells. The reported cell count of previously designed circuits is in the range of 30 – 307. But, due to various drawbacks like fault tolerance and high energy dissipation, these designs are not practically realizable. The proposed circuit is found to be 30% efficient in energy dissipation analysis. Therefore, it can now be concluded that the proposed design while using only a few more cells is far more efficient on critical design metric like energy dissipation.

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- **Availability of data and material:** Sources of information have been indicated as per their corresponding reference numbers.

- **Author Contribution:** Mr. Neeraj Tripathi played a pivotal role in refining the design. Mr. Rahil Jahangir contributed by collecting information. Mr. Mohammad Mudakir Fazili helped write the research paper.
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References

- [1] IEEE: International symposium on circuit and systems, 2004. QCA: a promising research area for CAS society.
- [2] Lent, Craig S., et al. "Quantum cellular automata." *Nanotechnology* 4.1 (1993): 49.
- [3] Sasamal, Trailokya Nath, Ashutosh Kumar Singh, and Anand Mohan. *Quantum-dot cellular automata based digital logic circuits: a design perspective*. Springer, 2020.
- [4] Bennett, Charles H. "Logical reversibility of computation." *IBM journal of Research and Development* 17.6 (1973): 525-532.
- [5] Landauer, Rolf. "Irreversibility and heat generation in the computing process." *IBM journal of research and development* 5.3 (1961): 183-191.
- [6] Feynman, Richard P. "Quantum mechanical computers." *Optics news* 11.2 (1985): 11-20.
- [7] Das, Jadav Chandra, and Debashis De. "Quantum-dot cellular automata based reversible low power parity generator and parity checker design for nanocommunication." *Frontiers of Information Technology & Electronic Engineering* 17.3 (2016): 224-236.
- [8] Ahmad, Firdous, Peer Zahoor Ahmad, and G. Mohiud din Bhat. "Design and analysis of odd-and even-parity generators and checkers using Quantum-dot Cellular Automata (QCA)." *2015 2nd International Conference on Computing for Sustainable Global Development (INDIACom)*. IEEE, 2015.
- [9] Santra, Santanu, and Utpal Roy. "Design and optimization of parity generator and parity checker based on quantum-dot cellular automata." *International Journal of Nuclear and Quantum Engineering* 8.3 (2014): 491-497.
- [10] Thapliyal, Himanshu, Nagarajan Ranganathan, and Saurabh Kotiyal. "Design of testable reversible sequential circuits." *IEEE transactions on very large scale integration (vlsi) systems* 21.7 (2012): 1201-1209.
- [11] Tahoori, Mehdi B., et al. "Testing of quantum cellular automata." *IEEE Transactions on Nanotechnology* 3.4 (2004): 432-442.
- [12] Toth, Geza, and Craig S. Lent. "Quasiadiabatic switching for metal-island quantum-dot cellular automata." *Journal of Applied Physics* 85.5 (1999): 2977-2984.
- [13] Lent, Craig S., P. Douglas Tougaw, and Wolfgang Porod. "Bistable saturation in coupled quantum dots for quantum cellular automata." *Applied Physics Letters* 62.7 (1993): 714-716.
- [14] Liu, Mo, and Craig S. Lent. "Bennett and Landauer clocking in quantum-dot cellular automata." *10th International Workshop on Computational Electronics*. 2004.
- [15] Lent, Craig S., and Beth Isaksen. "Clocked molecular quantum-dot cellular automata." *IEEE Transactions on Electron Devices* 50.9 (2003): 1890-1896.
- [16] Walus, Konrad, et al. "QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata." *IEEE transactions on nanotechnology* 3.1 (2004): 26-31.
- [17] Sen, Riya, and Sandip Das. "A novel approach to design convolution encoder using quantum-dot cellular automata." *2016 International Conference on Microelectronics, Computing and Communications (MicroCom)*. IEEE, 2016.
- [18] Bahar, Ali Newaz, et al. "Ultra-efficient convolution encoder design in quantum-dot cellular automata with power dissipation analysis." *Alexandria engineering journal* 57.4

(2018): 3881-3888.

- [19] Ahmed, Suhaib, and Syed Farah Naz. "Design of quantum dot cellular automata based fault tolerant convolution encoders for secure nanocomputing." *International Journal of Quantum Information* 18.06 (2020): 2050032.
- [20] Srivastava, Saket, et al. "QCAPro-an error-power estimation tool for QCA circuit design." *2011 IEEE international symposium of circuits and systems (ISCAS)*. IEEE, 2011.
- [21] Timler, John, and Craig S. Lent. "Power gain and dissipation in quantum-dot cellular automata." *journal of applied physics* 91.2 (2002): 823-831.
- [22] Tougaw, P. Douglas, and Craig S. Lent. "Dynamic behavior of quantum cellular automata." *Journal of Applied Physics* 80.8 (1996): 4722-4736.
- [23] Liu, Weiqiang, et al. "Are QCA cryptographic circuits resistant to power analysis attack?." *IEEE transactions on nanotechnology* 11.6 (2012): 1239-1251.
- [24] Srivastava, Saket, Sudeep Sarkar, and Sanjukta Bhanja. "Estimation of upper bound of power dissipation in QCA circuits." *IEEE transactions on nanotechnology* 8.1 (2008): 116-127.
- [25] Ma, Xiaojun, Jing Huang, and Fabrizio Lombardi. "A model for computing and energy dissipation of molecular QCA devices and circuits." *ACM Journal on Emerging Technologies*

Figures

Figure 1

Two possible logic states of a QCA cell

Figure 2

Two possible states of 900 QCA cell

Figure 3

Two possible states of 450 QCA cell

Figure 4

Clocking zones in QCA technology

Figure 5

NOT gate design in QCA

Figure 6

Majority gate design in QCA

Figure 7

Proposed design of 1/2 convolution encoder

Simulation Results

Figure 8

Simulated waveform of 1/2 convolution encoder

Figure 9

Proposed design of 1/3 convolution encoder

Simulation Results

Figure 10

Simulated waveform of 1/3 convolution encoder

Figure 11

Energy dissipation map of 1/2 convolution encoder at $\gamma=0.5E_k$

Figure 12

Energy dissipation map of 1/3 convolution encoder at $\gamma=0.5E_k$

Figure 13

Energy dissipation map of 1/2 convolution encoder at $\gamma=1.0E_k$

Figure 14

Energy dissipation map of 1/3 convolution encoder at $\gamma = 1.0E_k$

Figure 15

Energy dissipation map of 1/2 convolution encoder at $\gamma=1.5E_k$

Figure 16

Energy dissipation map of 1/3 convolution encoder at $\gamma=1.5E_k$