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Drain Current Model for a Single Gate Tunnel Field Effect Transistor with Hetero-Dielectric Gate (HDG)

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Abstract

Purpose: A TFET (Tunnel Field Effect Transistor) is a potential candidate to replace CMOS in deep-submicron region due to its lower SS (subthreshold swing, <60 mV/decade) at room temperature. However, the conventional TFET suffers from low tunneling current and high ambipolar current. To overcome these two drawbacks a new structure, known as Hetero-dielectric gate TFET (HDG TFET), has been proposed in the literature.

Method: To analyze the electrical characteristics of this structure, a closed form of analytical expression of current is required. This paper presents the closed form of compact analytical current model for HDG TFET structure without using any iterative method.

Result: The developed compact analytical models show a good agreement with 2-D TCAD simulator results. The model is used to study in depth about the electrical behavior of the device under various physical variation as well as bias variation.

Conclusion: The proposed model can be incorporated into SPICE to describe the behavior of HDG TFET faster.

Key words: 2-D Poisson Equation. Parabolic approximation, TFET, Hetero dielectric gate TFET, Ambipolar current, Tunnel Current, Tunnel Width, Kane Model,

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1. Introduction

In recent years, tunnel field effect transistor (TFET) has received attention of the researchers due to its lower subthreshold swing (<60 mV/decade) at room temperature [1-6] which makes TFET as an ideal choice to replace CMOS in design of power efficient nanoscale circuit. N-TFET devices employ

band-to-band tunneling (BTBT) process to inject the carriers from valence band of source to conduction band of channel [7-8]. However, TFET suffers from two major drawbacks of lower on-current than the conventional MOSFET and larger ambipolar current [9-10]. To overcome these drawbacks, a number of alternative design techniques as well as non-planar structures have been proposed in the literature. Among these, band gap engineering [11-12], gate oxide engineering [13-14], source/drain material engineering [15-16], multi gate technique [17-20] have been proposed to enhance the on current in the TFET. Gate-drain overlap structure [21-22] was suggested in the literature to suppress the ambipolar current. Each technique has its own advantage and disadvantage. Dual metal gate TFET has been proposed to enhance the on-current and suppress the ambipolar current [23-25]. However, main concern for this technique is that one has to choose appropriate work function for auxiliary gate to overcome both drawbacks at the same time. Chandan Kumar Pandey et al [26] has proposed dielectric pocket in TFET to suppress the ambipolar conduction. In this technique, they have replaced the upper portion of drain region with high κ-DP (dielectric pocket) at the channel-drain interface which increases the minimum tunneling width and hence suppresses the ambipolar current on the cost of on-current. Junsu Yu et al [27] has reduced the ambipolar current in TFET using a stacked gate in L-shaped. The main drawback of this method is an extra processing steps.

A hetero-dielectric gate (HDG) TFET has been proposed by researchers to increase the on-current and suppress the ambipolar current in the device [28-32]. In this proposed structure, high-κ oxide is placed near the source to induce a local minima of conduction band edge of the tunneling junction and low-κ oxide is placed near drain to suppress the ambipolar current. The electrical characteristics of these HDG TFET devices are mostly predicted with the help of TCAD simulator [33-34]. Far fast circuit simulation and to provide in depth understanding of the working principle of the HDG TFET, it is required to develop an analytical compact models. In the literature, various analytical models were proposed [35-40] but these models are either based on iterative methods or many assumptions. However, no compact closed form of drain current analytical expression of single gate HDG TFET structure is available in the literature.

In this paper, we have developed a compact close form of analytical expression for drain current of HDG TFET structure without using any iterative method. The expression is developed using 2-D Poisson equation and parabolic approximation. For the simplification of analysis, we have ignored the source/drain depletion width due to heavy doping and quantum confinement effect due to silicon film thickness larger than 3 nm. The model's results show a good agreement with 2-D TCAD simulator results which confirms the validity of the proposed models. The proposed current model, can be incorporated into Spice for fast simulation and better understanding of the electrical behavior of single gate HDG TFET. This paper is organized as: Section 2 describes the device structure. Section 3 explains the derivation of the analytical models from the solution of 2-D Poisson equation whereas section 4 elaborates on the results. At the end, we conclude the paper in section 5.

2. Device Structure

The 2-D structure and coordinate system of the proposed N-type hetero-dielectric gate TFET (HDG TFET) is shown in Figure 1. The whole channel of length L is divided into two regions, namely, Region I of high-κ-oxide near source with length L1 and Region II of low-κ-oxide near drain of length L2. The high κ-material near the source-channel interface is placed to increase the tunneling current whereas low-κ-material near drain to suppress the ambipolar current. The channel is practically undoped ($\approx 10^{15}/cm^3$), the p^+ source and n^+ drain is heavily doped ($\sim 10^{20}/cm^3$ and $5x10^{18}/cm^3$ respectively). Initially, the high-κ oxide thickness t_{ox1} and the low-κ oxide thickness t_{ox2} are equally set as 3 nm. The gate metal work function for two regions is taken as 4.25 eV unless and until specified. In the present analysis, we have ignored the source/drain depletion region due to heavy doping and the quantum mechanical effect due to silicon film thickness of 5 nm.

To validate the developed analytical models, we used 2-D TCAD simulator results, under the assumptions of the non-local band-to-band tunneling (BTBT), the band gap narrowing, Fermi-Dirac statistics, Shockley-Read-Hall (SRH) recombination and doping dependent mobility for comparison.

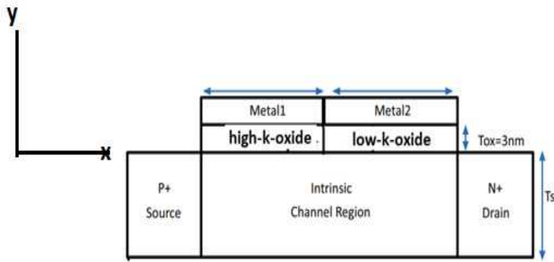

Figure 1: 2-D cross-sectional view of HDG TFET

3. Analytical Models

The 2-D Poisson's equation can be used to describe the potential behavior of the proposed TFET structure across the two regions. After neglecting the fixed carrier oxide charges, 2-D Poisson's equation, governing the potential distribution $\psi_j(x,y)$ in the respective region, is given as;

$$\frac{d^2\psi_j(x,y)}{d^2x} + \frac{d^2\psi_j(x,y)}{d^2y} = -\frac{qN_a}{\varepsilon_{si}}$$
(1)

Where, N_a is the channel doping concentration, j=1, 2 represents the region I and region II, ε_{si} is the silicon permittivity, $\psi_j(x,y)$ is the 2-D electrostatic potential in the region I and II measured with respect to Fermi potential.

Solution of this differential equation (1) can be obtained by assuming parabolic profile along the film thickness t_{si} as [40];

$$\psi_j(x,y) = a_0 + a_{j1}y + a_{j2}y^2$$
(2)

Where, a_0, a_{j1}, a_{j2} are constants and function of x- only. The value of these unknowns can be obtained by using appropriate Boundary Conditions (BCs) [40].

(a)Surface and Channel Potential

Following the same procedure, as mentioned in our earlier paper [40], differential equation (1) can be reduced to 2-D scaling equation,

$$\frac{d^2\psi_{sj}(x)}{dx^2} - \frac{1}{\lambda_j^2}\psi_{js}(x) = -\frac{\sigma_j}{\lambda_j^2}$$
(3)

where

$\lambda_j = \sqrt{\dfrac{\varepsilon_{si} t_{si}}{2\varepsilon_{ox_j}}}$ is known as characteristic or scaling length, $\sigma_j = \dfrac{-qN_{aj}}{\varepsilon_{si}} \lambda_j^2 - V'_{GSF}$ is long channel surface potentials, $V'_{GSF} = v_{gs} - v_{fb}$

Equation (3) describes the surface potential in the respective region. The general solution of equation (3) is given as

$$\psi_{js}(x) = A_j e^{\frac{x-L_j}{\lambda_j}} + B_j e^{-\frac{x-L_j}{\lambda_j}} + \sigma_j$$
(4)

where A_j and B_j are constant and determined using following Boundary Conditions (BCs):

At source channel interface $(x=0)$,

$$\psi_{si}(x=0) = \upsilon_{bi1}$$
5(a)

At boundary of two regions $(x = L_1)$,

$$\psi_{si}(x = L_1) = \psi_{s_2}(x = L_1)$$
5(b)

At boundary of two regions $(x = L_1)$, electric flux is continuous at the junction

$$\frac{d\psi_{s1}(x = L_1)}{dx} = \frac{d\psi_{s_2}(x = L_1)}{dx}$$
5(c)

At drain-channel interface,

$$\psi_{s_2}(x = 2) = \upsilon_{bi2} + \upsilon_{ds}$$
5(d)

where υ_{bij} is the built-in-potential at the respective interface and given as

$$\upsilon_{bi1} = \frac{KT}{q} \ln\left(\frac{N_s N_a}{n_i^2}\right)$$

$$\upsilon_{bi2} = \frac{KT}{q} \ln\left(\frac{N_d N_a}{n_i^2}\right)$$

Where N_s and N_d are the doping concentration of the source and drain regions, n_i is the intrinsic carrier concentration.

Using BCs 5(a) to 5(d) and after mathematical simplification, the value of the constants is,

$$A_1 = \gamma_{11} + B_2 \quad , \quad B_1 = -z_{12} B_2 + z_{11} \quad , \quad A_2 = \frac{\beta_{13} - \beta_{12} B_2}{\beta_{11}}$$

where

$$\gamma_{11} = \frac{\alpha_{11}}{\beta_{11}} \beta_{15} \quad , \quad \alpha_{11} = \frac{\left(1 + \frac{\lambda_1}{\lambda_2}\right)}{2} e^t \quad , \quad t = \frac{L_1 - L_2}{\lambda_2} \quad , \quad \beta_{11} = \alpha_{11}\left(1 - 2e^{-\frac{L_1}{\lambda_1}}\right) - e^t$$

$$\beta_{13} = \frac{N}{2}\left(1 - e^{\frac{-2L_1}{\lambda_1}}\right) - \left(\upsilon_{bc_1} - \sigma_1\right) e^{-\frac{L_1}{\lambda_1}} \quad , \quad N = \sigma_2 - \sigma_1 \quad , \quad \beta_{14} = \beta_{13} e^{t_1} - \beta_{11} N_2 \quad , \quad t_1 = \frac{L - L_2}{\lambda_2}$$

$$N_2 = \upsilon_{bi2} + \upsilon_{ds} \quad , \quad \beta_{15} = \beta_{12} e^{t_1} - \beta_{11} e^{-t} \quad , \quad \beta_{12} = \alpha_{12}\left(1 - e^{-\frac{L_1}{\lambda_1}}\right) - e^{-t} \quad , \quad \alpha_{12} = \left(\frac{1 - \frac{\lambda_1}{\lambda_2}}{2}\right) e^{-t}$$

$$z_{11} = \left(\upsilon_{bi1} - \sigma_1\right) e^{-\frac{L_1}{\lambda_1}} - \gamma_{11} e^{-\frac{2L_1}{\lambda_1}} \quad , \quad z_{12} = \gamma_{12} e^{-\frac{2L_1}{\lambda_1}} B_2 \quad , \quad \gamma_{12} = \alpha_{12} - \gamma_{11} e^{-\frac{2L_1}{\lambda_1}}$$

Substituting the value of these constants in equation (4), the analytical expression of the surface potential in the respective region can be obtained. After determining the surface potential, the channel potential is given as,

$$\psi_j(x, y) = \psi_{sj}(x)\left[\delta_{1j} + \delta_{4j} y^2\right] + \left[\delta_{2j} + \delta_{3j} y^2\right]$$
(6)

where

$$\delta_{1j} = \frac{c_{ox_j}}{\varepsilon_{si}} \cdot \frac{t_{si}}{4} + 1 \quad , \quad \delta_{2j} = \frac{c_{ox_j}}{\varepsilon_{si}} \cdot \frac{t_{si}}{4} V'_{GSF}$$

$$\delta_{3j} = \frac{-c_{ox_j}}{\varepsilon_{si}\ t_{si}} V'_{GSF} \quad , \quad \delta_{4j} = \frac{-c_{ox_j}}{\varepsilon_{si}\ t_{si}}$$

The transverse and the lateral electric field in the proposed TFET can be determined using equation (6) and relations,

$$E_{jy} = \frac{-d\psi_j(x, y)}{dy} \text{ and } E_{xj} = \frac{-d\psi_j(x, y)}{dx}$$

And thus the total electric field is

$$E = \sqrt{E_{jx}^2 + E_{jy}^2}$$

(b) Tunneling Width

Tunneling width is an important parameter to determine the tunneling current from source-to-channel as well as ambipolar current from drain-channel in the TFET device. This parameter exhibits transition from strong dependence to weak dependence on the gate voltage. The tunneling path is defined as the lateral distance between two tunneling points x_1 and x_2 where x_1 is the initial tunneling point and x_2 is the final tunneling point. The initial tunneling point is defined as the value of x for which surface potential changes by an amount $\left(\frac{E_g}{q}\right)$ with respect to source-channel interface [41]. In the present paper, the initial tunneling point is assumed to confined in region 1.

Using $\psi_{s_1}(x = x_1) - \psi_{s_1}(x = 0) = \frac{E_g}{q}$ and substituting the value of surface potential of region 1, the analytical expression for the initial tunneling point (after mathematical simplification) is given as;

$$x_1 = \frac{\lambda_1}{2} \ln \frac{W_{12}}{2}\left[1 \pm \sqrt{1 + \frac{W_{11}}{W_{12}^2}}\right]$$

(7)

where

$$W_{11} = \frac{B_1}{A_1} e^{\frac{2L_1}{\lambda_1}} \quad \text{and} \quad W_{12} = \frac{A_1 + B_1 e^{\frac{2L_1}{\lambda_1}}}{A_1} - \frac{E_g}{q}$$

The initial tunneling point plays an important and decisive role to determine the tunneling current. The shorten x_1 increases the probability of tunneling of carriers and hence results in larger tunneling current. The final tunneling point x_2 is defined as the lateral distance between $x = 0$ to a point where surface potential reaches to the value of the channel potential [41]. Using this definition and after mathematical simplification, we get

$$x_2 = \frac{\lambda_1}{2} \ln \frac{W_{14}}{2}\left(1 \pm \sqrt{1 - \frac{4W_{15}}{W_{14}}}\right)$$

(8)

where

$$W_{15} = \left(\frac{B_1}{A_1}\right) e^{\frac{2L_1}{\lambda_1}} \quad ,$$

$$W_{14} = \left(\frac{\phi_{ch} + \frac{E_g}{q} - \sigma_1}{A_1}\right) e^{\frac{L_1}{\lambda_1}}$$

ϕ_{ch} is the channel potential. The final tunneling point is also confined in region I due to high dielectric material in the source channel region. A similar approach can be used to determine the tunneling points in region II derive analytical expression for the ambipolar current.

(c) Tunneling current

In non-local BTBT, tunneling of charges start only when conduction band edge (CB) of source gets in line with the valence band edge (VB) of the channel region [41]. The tunneling current can be obtained by integrating Kane's band-to-band tunneling (BTBT) generation rate over the entire tunneling volume in both radial and lateral directions as [41];

$$I_{BTBT(S-C)} = q \iiint G_{BTBT}\, dxdydz$$

9(a)

Where G_{BTBT} is the generation rate of the carriers and given as

$$G_{BTBT} = A_k E_{av}^{D} \exp\left(-\frac{B_k}{E}\right)$$

9(b)

A_k and B_k are Kane's parameters dependent upon the effective tunneling mass, charge, the effective bandgap at the tunneling junction and Planck constant. Their values are; A_k=1.4 × 1020 $eV^{1/2}$ //cm.s.V^2 and B_k=

8.6×10^6 V/cm.eV$^{3/2}$, respectively. E_{av} is average electric field, E is the resultant field, and D is fitting parameter (its value is either 2 or 2.5 depending upon the nature of semiconductor material).

In the present paper, we have derived the analytical expression for the tunneling current in the radial direction of the channel from initial tunneling point $x_1$to final tunneling point x_2. It is assumed that the tunneling current is uniform across the channel width W_{ch} and effective channel thickness t_{si}. Therefore, equation 9(a) reduces to

$$I_{BTBT(S-C)} = q * W_{ch} * t_{si} \int_{x_1}^{x_2} G_{BTBT}\, dx$$
9(c)

Using $E_{av} = E * \frac{(\frac{E_g}{q})^{D-1}}{x^{D-1}}$ in expression 9(c), we get

$$I_{BTBT(S-C)} = q * W_{ch} * t_{si} * A_k * (\frac{E_g}{q})^{D-1} \int_{x_1}^{x_2} \frac{E}{x^{D-1}} \exp\left(-\frac{q*B_k}{E_g} x\right) dx$$
9(d)

Using $\psi_1(x,y) = a_0 + a_{11}y + a_{12}y^2$ and $E_y = -\frac{d\psi_1(x,y)}{dy}$, we get the electric field along y-direction;

$$E_y = -[a_{11} + 2ya_{12}]$$
10(a)

After squaring on both sides of equation 10(a) and substituting a_{11}=0 (because for the proposed structure we have a_{11}=0), we get

$$E_y^2 = 4 * a_{12}^2(x) * y^2$$
10(b)

The resultant electric field in the proposed structure is given as (since, t_{si} <<1 and neglecting y^2 term in equation 10(b) so that $E_y \rightarrow 0$)

$$E = \sqrt{E_x^2 + E_y^2} = E_x$$
10(c)

Substituting the value of resultant field from equation 10(c) in equation 9(d) we get

$$I_{BTBT(S-C)} = (q * W_{ch}) * (\frac{1}{\lambda_1}) * t_{si} * A_k * (\frac{E_g}{q})^{D-1} \int_{x_1}^{x_2} [A_1 * e^{\left(\frac{x-L_1}{\lambda_1}\right)} - B_1 * e^{-\left(\frac{x-L_1}{\lambda_1}\right)}] \exp\left(-\frac{q*B_k}{E_g} x\right) * (x^{1-D})\, dx$$
10(d)

Let $\frac{1}{\lambda_1} - \frac{q*B_k}{E_g} = \lambda_{11}$ and $\frac{1}{\lambda_1} + \frac{q*B_k}{E_g} = \lambda_{12}$. Substituting λ_{11} *and* λ_{12} in equation 10(d) and taking D=2 for simplification, we get

$$I_{BTBT(S-C)} = (q * W_{ch}) * (\frac{1}{\lambda_1}) * t_{si} * A_k * (\frac{E_g}{q})^1 \{A_1 * e^{-\frac{L_1}{\lambda_1}} * \int_{x_1}^{x_2} [e^{(\lambda_{11}*x)} * \left(\frac{1}{x}\right)] dx - B_1 * e^{\frac{L_1}{\lambda_1}} * \int_{x_1}^{x_2} [e^{(\lambda_{12}*x)} * \left(\frac{1}{x}\right)] dx\}$$
11(a)

Using, the expansion e^x=1+x+higher orders and neglecting higher order terms due to short channel device, equation 11(a) reduces to;

$$I_{BTBT(S-C)} = (q * W_{ch}) * (\frac{1}{\lambda_1}) * t_{si} * A_k * (\frac{E_g}{q})^1 \{A_1 * e^{-\frac{L_1}{\lambda_1}} * \int_{x_1}^{x_2} [\frac{1+\lambda_{11}x}{x}] dx - B_1 * e^{\frac{L_1}{\lambda_1}} * \int_{x_1}^{x_2} [\frac{1+\lambda_{12}}{x}] dx$$

After performing the integration and simplification, the closed form of the tunnel current from source to channel is given as;

$$I_{BTBT(S-C)} = (q * W_{ch}) * (\frac{1}{\lambda_1}) * t_{si} * A_k * (\frac{E_g}{q})^1 \{(A_1 * e^{-\frac{L_1}{\lambda_1}} - B_1 * e^{\frac{L_1}{\lambda_1}}) \ln\frac{x_2}{x_1} + (\lambda_{11} +$$

$\lambda_{12})(x_2 - x_1)\}$
11(b)

This expression is derived without any iteration and much approximations.

4. Results and Discussion

We have analyzed the developed analytical models in detail to understand the electrical characteristics of the proposed device in terms of surface potential, electric field and drain current. The study is also helpful to get in-depth understanding of the gate engineered structure. The values of various parameters used in the model are; L=30 nm, L1=15-20 nm, t_{si}=5 nm and t_{ox}=3 nm unless and until specified. The source region and drain region are heavily doped with dopant concentration of $10^{20}/cm^3$ and $5x10^{18}/cm^3$ respectively whereas channel region is lightly doped with $5x10^{15}/cm^3$ dopant concentration. To validate the developed analytical models, results were compared with 2-D TCAD simulator.

Figure 2(a) shows the variation of surface potential along the channel of the proposed structure. The surface potential first reduces along the channel for x ≤ 25 nm and then increases sharply. The sharp rise in surface potential near drain restricts the tunnel of carriers from drain to channel and hence suppresses the ambipolar current. The change in surface potential due to increased gate-source voltage greatly narrows the tunneling width for charge carriers near source and hence results in larger tunneling probability. The model results show a good agreement with the 2-D simulator results.

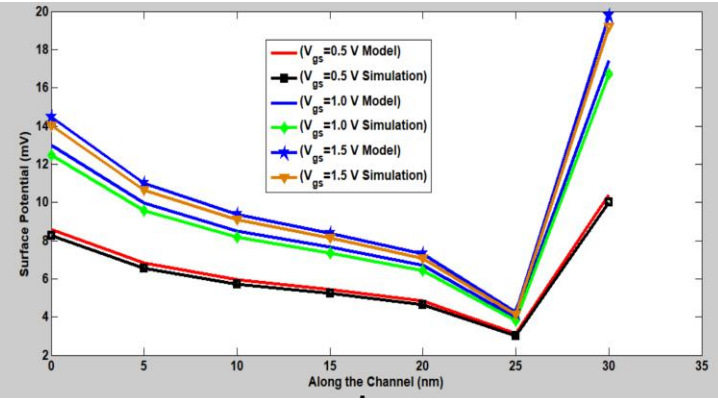

Figure 2(a): Surface potential variation along channel: comparison with 2-D ATLAS Simulator

Figure 2(b) shows the variation of surface potential along the channel for different V_{ds} values. One interesting result is that the surface potential does not show any significant change with drain voltage in region I. This finding reflects that the drain induced barrier lowering (DIBL) effect in TFET can be controlled by placing high κ-oxide over the source-channel region. A significant variation in surface potential occurs near drain region where it takes larger value for the lower drain-source voltage.

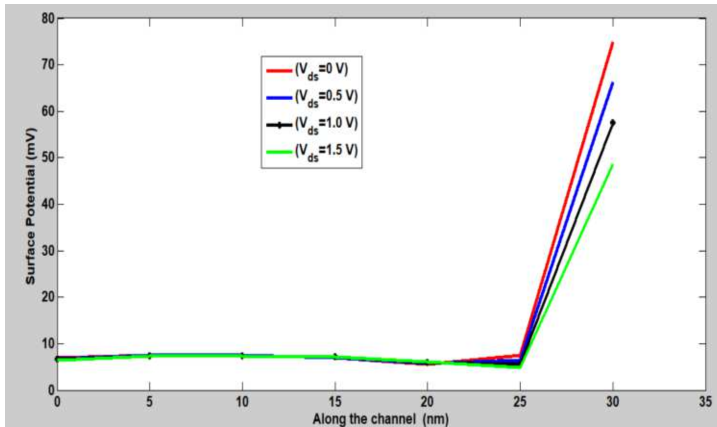

Figure 2(b): Variation of Surface potential along channel for different V_{DS} value

We have analyzed the effect of length L1 on the surface potential of the proposed structure. As LI decreases, conduction band

becomes shallower which results in lower tunneling of carriers whereas the increase in L1 results in wider conduction band as seen from Figure 2(c). This result suggests that an optimized value of L1=15 nm is a good choice to control the tunneling and ambipolar currents in the device.

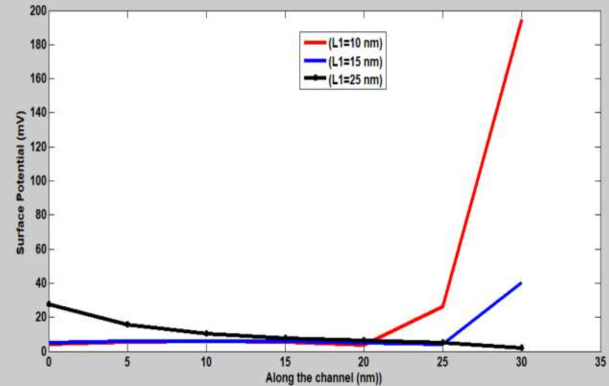

Figure 2(c): Surface potential variation along channel for different length of high-κ oxide

Figure 2(d) shows that thinner EOT (equivalent of thickness) means stronger gate control over the tunneling channel which results in considerable bending of the energy band diagram at the drain-channel junction. This results in sharp increase in surface potential. As a result, we have narrow tunnel width and larger tunnel current. This finding reflects that the scaling of EOT can produce larger tunnel current in the proposed device.

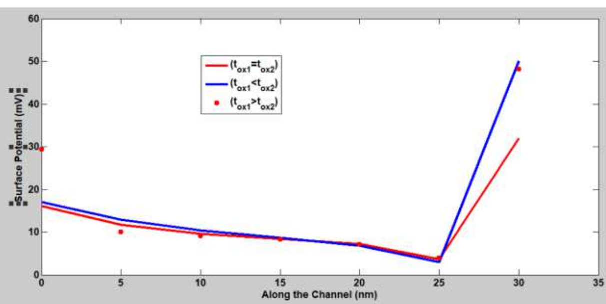

Figure 2(d): Surface potential along the channel for different combination of oxide thickness

Figure 3(a) shows the variation of tunneling width against gate-source voltage (V_{gs}) for a single dielectric gate TFET and hetero-dielectric gate TFET. It is observed that hetero-dielectric gate TFET results in narrow tunneling width compare to a single dielectric gate TFET irrespective of the gate source voltage. Tunneling width shows a sharp decrease with Vgs for hetero dielectric gate TFET, which results in larger tunnel current compare to a single dielectric gate TFET. The model results show a good agreement with simulator results. A slight difference is due to negligence of source depletion width in the proposed model.

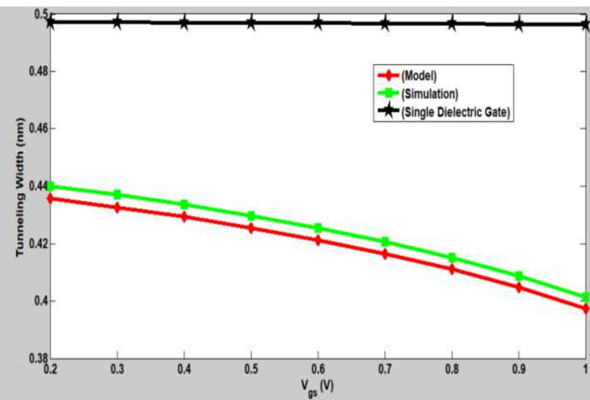

Figure 3(a): Tunneling width versus V_{gs} for single dielectric gate and Hetero-dielectric gate

Figure 3(b) shows that the tunneling width of the proposed structure decreases as the dielectric constant κ- of region I increases due to stronger gate control over the channel. This tells us that the purpose of introducing high κ-dielectric near source-channel junction is to shorten the on-state tunnel path.

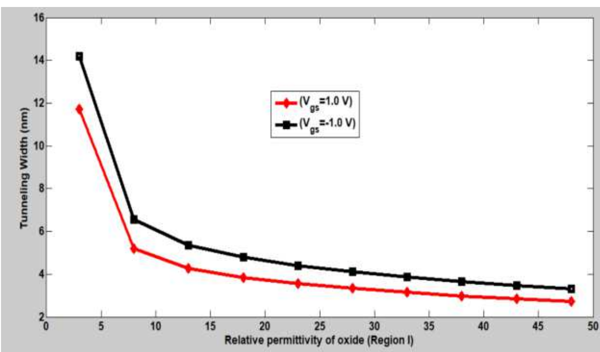

Figure 3(b): Tunneling width versus relative permittivity of oxide in region I for two different values of V_{gs}

We have analyzed the lateral as well as transverse electric field of region II as shown in Figure 4(a). Both the fields increase as the dielectric constant κ-increases. From analytical results, it is observed that for $\kappa \leq 4$, fields take negative value. The negative field in drain-channel region deaccelerates the carriers and hence suppresses the ambipolar current. From this result, it is clear that SiO_2 dielectric material near drain-channel region, is the natural choice to control the ambipolar current.

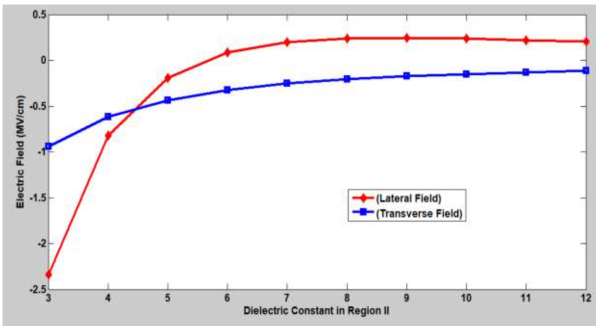

Figure 4(a): Electric field versus dielectric constant in region II

Figure 4(b) shows the variation of lateral electric field in region I along the channel for single dielectric gate TFET and hetero dielectric gate TFET for κ=25 and κ=50. It is observed that field takes larger value near source-channel junction for κ=50 due to better control of gate over the channel. The peak of the lateral electric field near the source-channel interface is responsible for the larger tunneling probability.

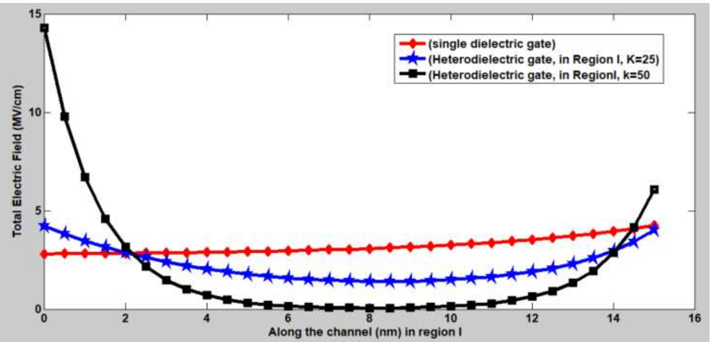

Figure 4(b): Total electric field along region I for single dielectric gate and Hetero-dielectric gate

Figure 5(a) shows the variation of drain current per unit channel width with gate source voltage. For negative gate bias voltage, ambipolar current decreases and reaches to its minimum value at V_{gs}=-0.4 V. The on-current starts only when gate-source voltage is equal or larger than threshold voltage which is more than 500 mV in this structure. The analytical results show an excellent matching with the simulator results.

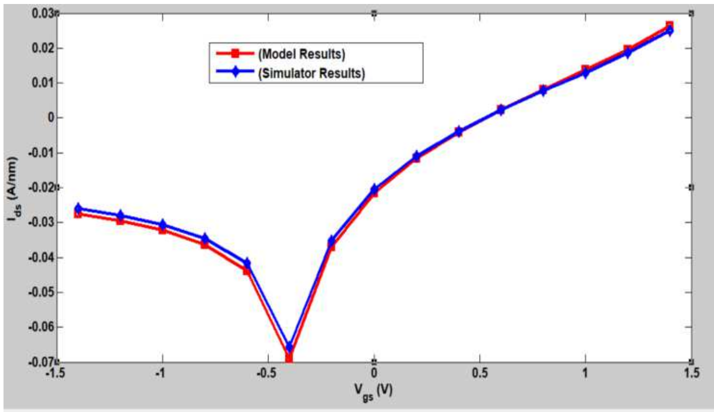

Figure 5(a): Comparison of drain current with 2-D ATLAS simulator result

We have studied the transfer characteristics of single dielectric gate TFET and hetero

dielectric gate TFET as shown in Figure 5(b). Single dielectric gate TFET is studied under two cases; case 1 when gate is occupied by SiO_2. Case 2 when gate is occupied by HfO_2-dielectric material. In case 2, we have larger on-current compared to case 1 but hetero dielectric gate TFET provides lower ambipolar current and larger ON current compare to the single dielectric TFET.

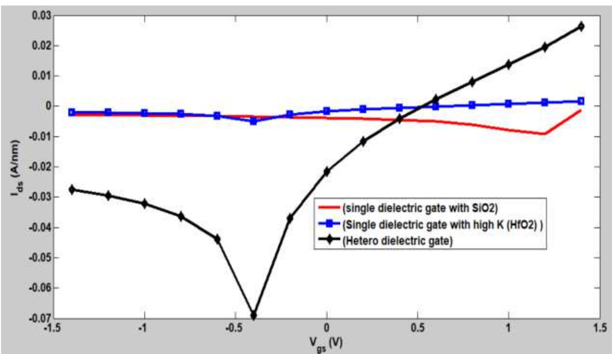

Figure 5(b): Transfer characteristics for single dielectric gate and Hetero-dielectric gate

To further investigate the effect of dielectric material on the drain current of the proposed structure, we have plotted the graph as shown in Figure 5(c). The analytical results show that larger on-current and lower ambipolar current is obtained when region I is occupied by larger dielectric material of strength κ=50 and region II is occupied by SiO_2. The result concludes that an improved on-current and decreased SS can be obtained using gate engineering.

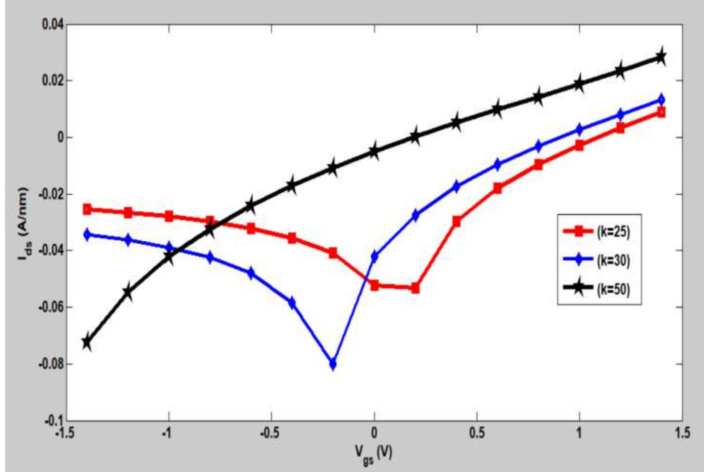

Figure 5(c): Transfer characteristics for different –κ oxide values

To see the effect of work function on the drain current of the hetero dielectric gate TFET, we have studied the current for single metal TFET and two other cases namely; dual metal gate with tunnel gate having higher work function and dual metal gate with auxiliary gate having larger work function. The result is shown in Figure 5(d). Due to reduction of the tunnel gate work function compare to auxiliary gate, the band width overlap increases which results in narrow tunneling width and hence ultimately increase in on-current on the cost of increased ambipolar current. This result also suggests that the work function difference results in change in surface potential which improves the gate control over tunneling process. A narrow tunneling width gives larger tunneling probability of carriers. Therefore, we can conclude that gate dielectric engineering along with choice of metal can be employed in HDG TFEET design to enhance the tunnel current and reduce the ambipolar current.

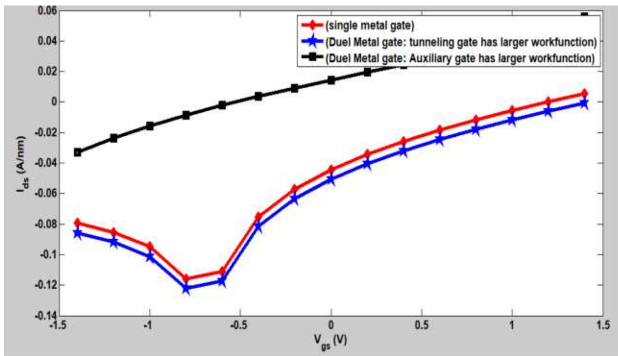

Figure 5(d): Transfer characteristics for single metal gate and dual metal gate with Hetero-dielectric

Since, the length of region I (L1) determines the tunneling barrier width in the source region, it is observed that as L1 increases the tunneling current enhances on the cost of increased ambipolar current as seen in Figure 5(e). The lower ambipolar current and acceptable on-current in the proposed structure is obtained when L1=15 nm for L=30 nm. Therefore, for the better electrical performance of the device, we have chosen the optimized value of L1=15 nm instead of L1=20 nm on the cost of slight decrease in on-current. This result also confirms the finding that as L1 decreases, BTBT becomes difficult due to shallower conduction band well whereas an increase in L1 results in less abrupt transition between on- and off-state due to wider conduction band.

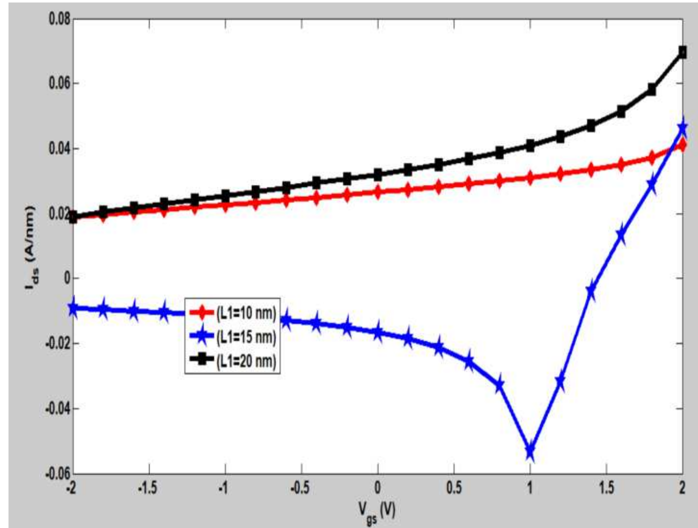

Figure 5(e): Transfer characteristics of HDG TFET for different length of region I

The silicon film thickness t_{si} is the critical parameter for better gate control over the channel. The lower tunneling width is achieved for lower t_{si} which results in higher tunneling probability and hence larger tunneling current (on current) as seen from Figure 6(a). The lower silicon film thickness also reduces the ambipolar current. Figure 6(a) shows that on-current decreases with increase in film thickness. For better on-current and lower off-current in the device, the optimized value of the t_{si}=6 nm.

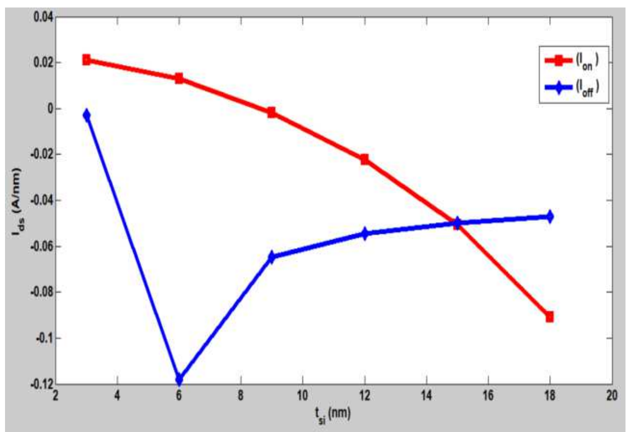

Figure 6(a): ON and Off current versus silicon film thickness

From our proposed analytical results, it was observed that higher gate dielectric material in source-channel region provides larger tunneling current as long as t_{si}<12 nm (Figure 6(b)). This study only reflects that using gate engineering and lower film thickness, one can enhance the tunneling current and suppress the ambipolar current in TFET device. The improved on-current can result in decreased SS as well as controlled SCEs. From this observation, it is concluded that careful choice of the gate dielectric material near source and film thickness can improve the on-current and reduce SS of HDG TFET.

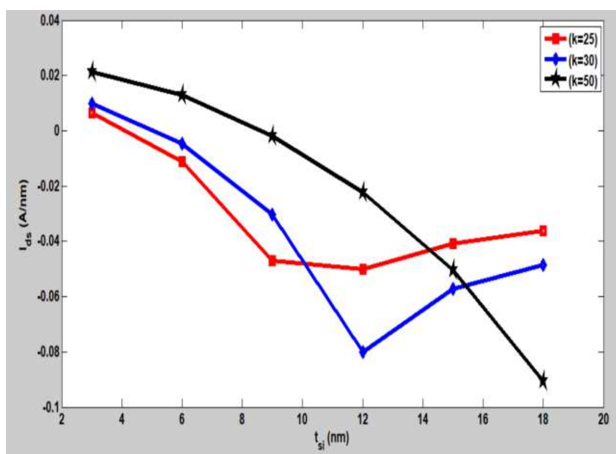

Figure 6(b): Drain current versus t_{si} for different high-κ values

As seen from Figure 7(a), the heavily doped source region results in higher tunneling current because increase in source doping concentration causes increase in band narrowing which results in narrower tunneling width. The narrow width, increases the tunneling probability of carriers from source valence band to channel conduction band and hence increase in tunnel current.

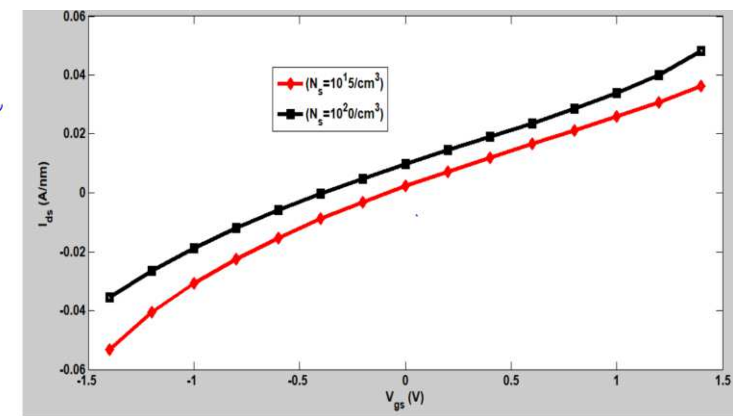

Figure 7(a): Transfer characteristics for different source doping concentration

The ambipolar current in the proposed structure reduces when drain region is doped with concentration of $10^{18}/cm^3$instead of $10^{20}/cm^3$as seen from Figure 7(b).

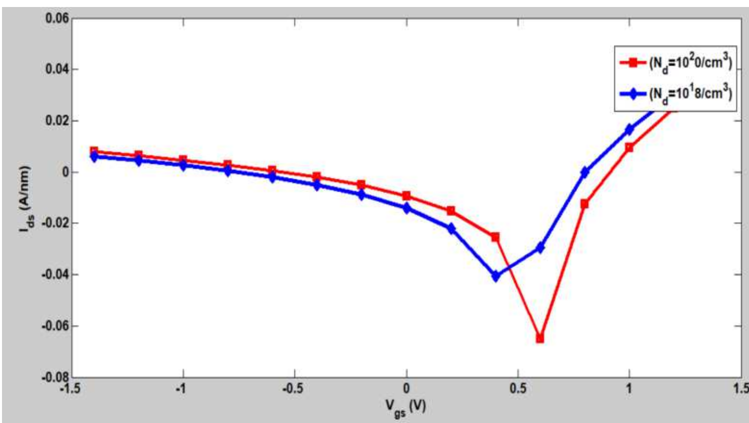

Figure 7(b): Transfer characteristics for different drain doping concentration

Therefore, the proposed structure HDG TFET can be a potential candidate for replacing convention MOSFET in deep submicron region due to larger on-current, lower SS and controlled SCEs as well as reduced ambipolar current which can be further improved by utilizing gate engineering as well as material engineering in the design.

5. Conclusion

A compact analytical model of drain current has been proposed for single gate HDG TFET without any iterative method. The proposed model gives close form without much approximations. The model is derived based on surface potential approach with parabolic approximation. The results of analytical models show a good agreement with 2-D ATLAS simulator results which establish the validity of the proposed model. Due to reduction of work function of tunneling region, a narrow tunneling width is achieved which enhances the on-current in device. It is also observed that a thinner silicon film result in larger drain current. The proposed structure results in lower SS and controlled SCEs due to gate engineering and material engineering combination.

6. Declarations

6.1 Funding:

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6.2 Competing interests

Authors declare that there is no competing interest

6.3 Availability of data and material

In the present paper, there is no data or materials which are required to be disclosed or shared

6.4 Code Availability

NA

6.5 Consent for Publication

Authors are giving their consent for the publication of this research paper

6.6 Authors' contributions

Each author has same contribution

6.7 Acknowledgement

Authors are thankful to Dr Ganapathirao Maradana, NIIT University for his valuable suggestions regarding the mathematical issues.

6.8 Compliance of ethical standard

6.8.1 Disclosure of potential conflicts of interest

There is no conflict of interest involved in this work

6.8.2 Research involving human participants and/or animals

NA

6.8.3 Informed Consent

NA

6.9 Consent to Participate

Authors are giving their consent for participation

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Figures

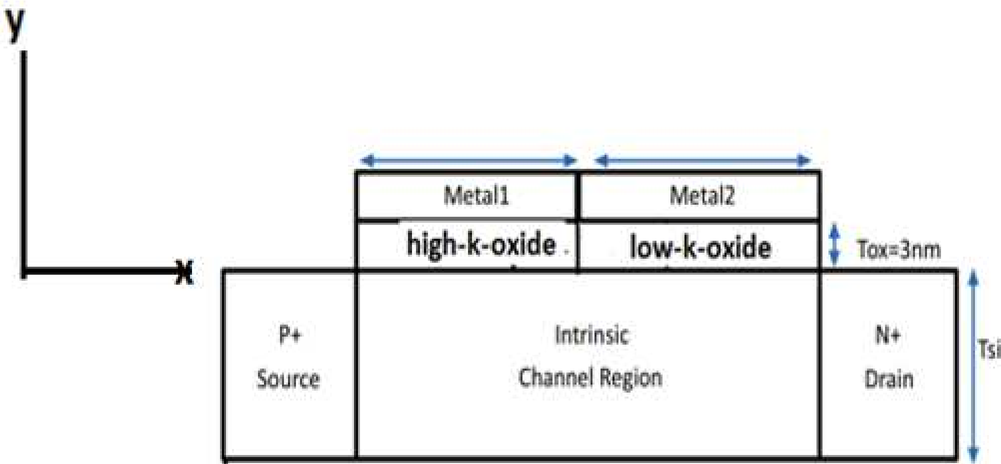

Figure 1

Please see the Manuscript PDF file for the complete figure caption

Surface Potential (mV)
(V_{gs}=0.5 V Model)
(V_{gs}=0.5 V Simulation)
(V_{gs}=1.0 V Model)
(V_{gs}=1.0 V Simulation)
(V_{gs}=1.5 V Model)
(V_{gs}=1.5 V Simulation)
Along the Channel (nm)

a

Surface Potential (mV)
(V_{ds}=0 V)
(V_{ds}=0.5 V)
(V_{ds}=1.0 V)
(V_{ds}=1.5 V)
Along the channel (nm)

b

Surface Potential (mV)
(L1=10 nm)
(L1=15 nm)
(L1=25 nm)
Along the channel (nm))

c

Surface Potential (mV)
(t_{ox1}=t_{ox2})
(t_{ox1}<t_{ox2})
(t_{ox1}>t_{ox2})
Along the Channel (nm)

d

Figure 2

Please see the Manuscript PDF file for the complete figure caption

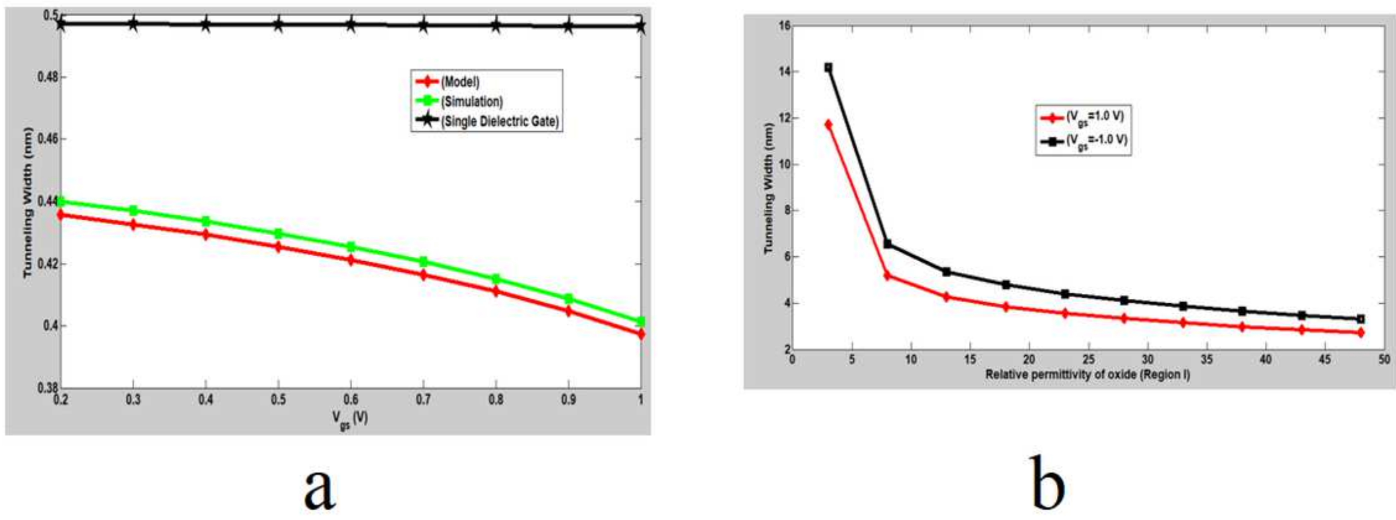

Figure 3

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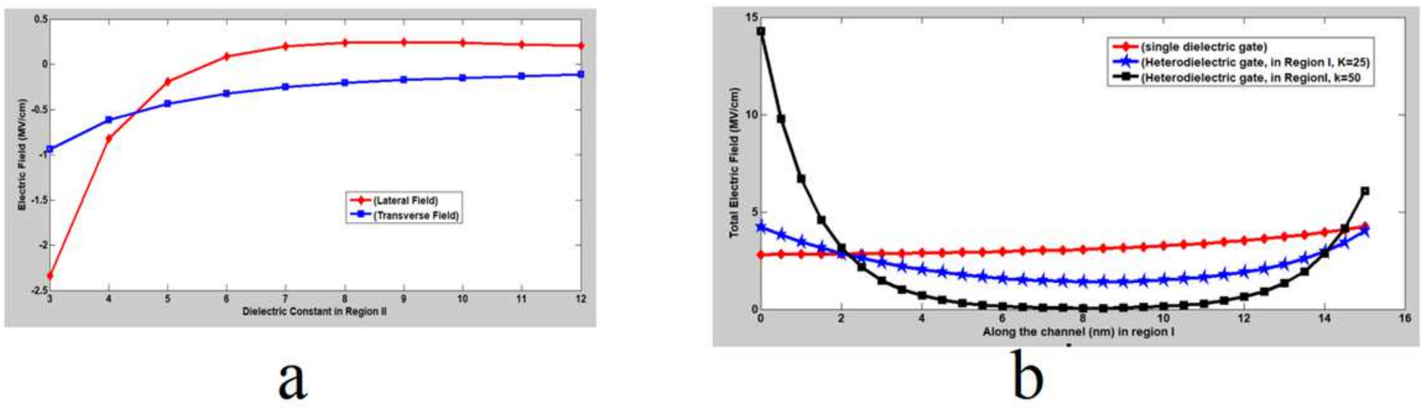

Figure 4

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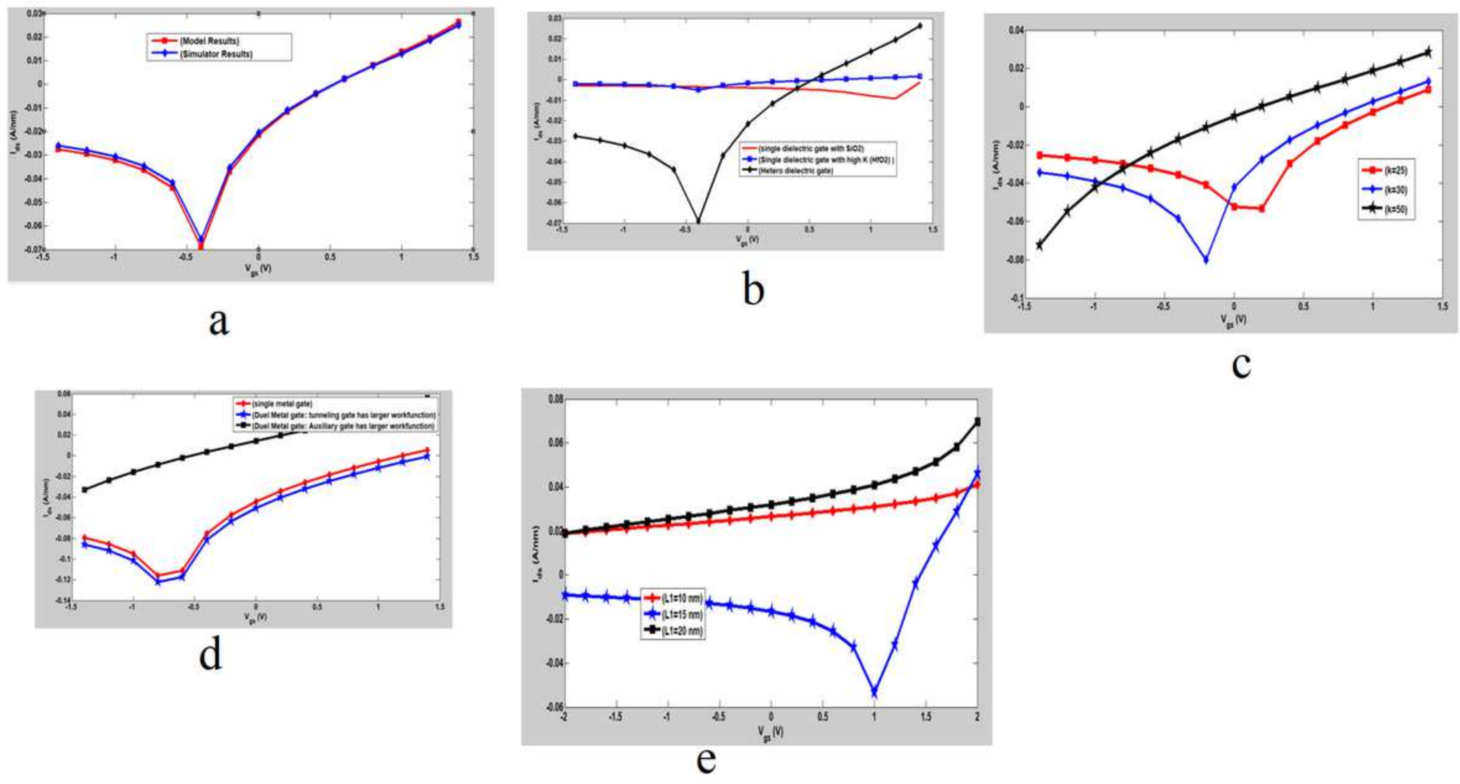

Figure 5

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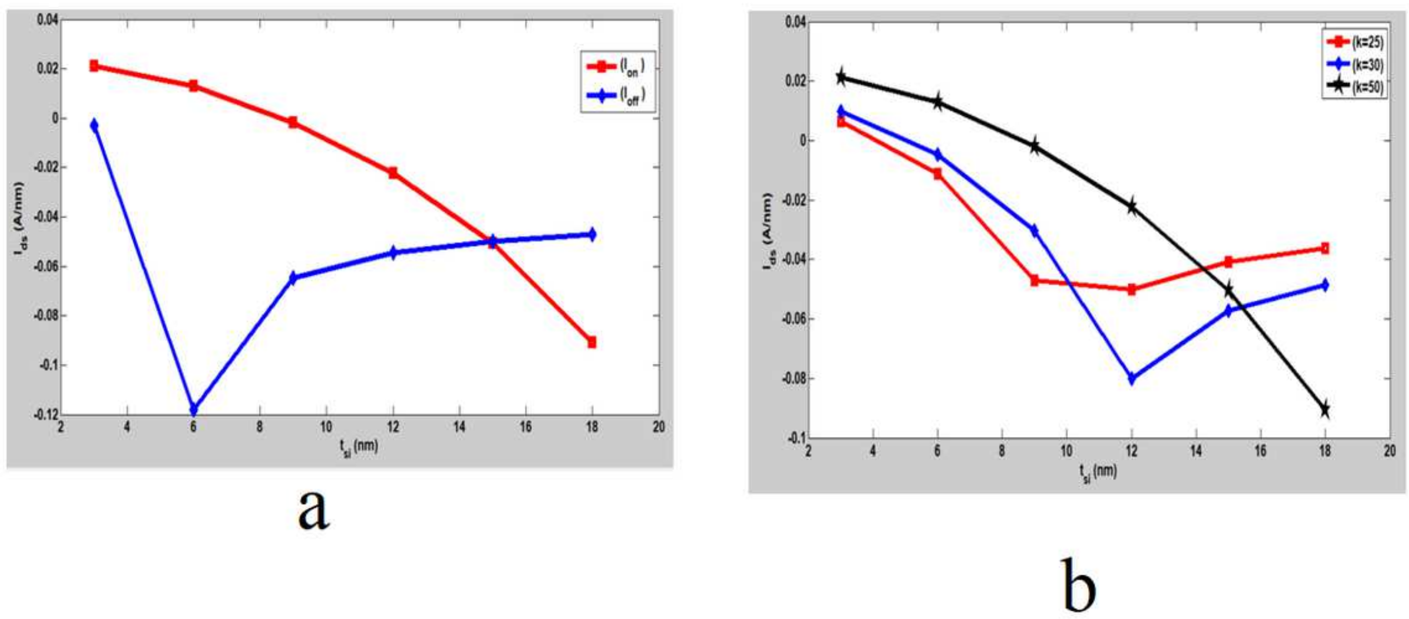

Figure 6

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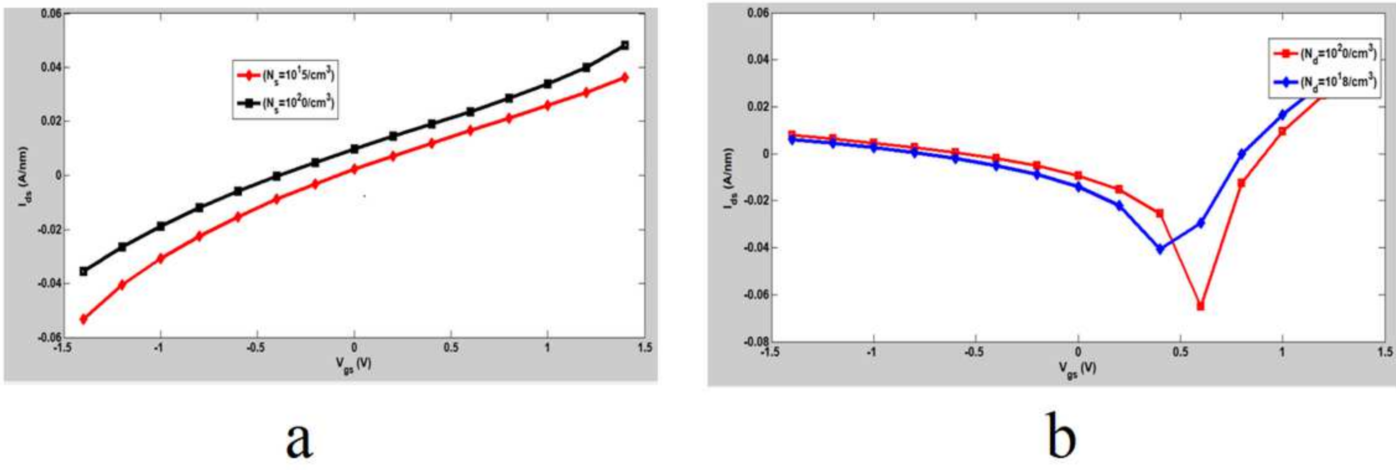

Figure 7

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