# A Low power, Highly Efficient, Linear, Enhanced wideband Class-J mode Power Amplifier for 5G Applications

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**Research Article**

**Keywords:** 5G power amplifier, good efficiency, wide bandwidth, class-J output matching network

**Posted Date:** June 9th, 2021

**DOI:** https://doi.org/10.21203/rs.3.rs-580463/v1



**Version of Record:** A version of this preprint was published at Scientific Reports on May 16th, 2022. See the published version at https://doi.org/10.1038/s41598-022-12235-z.

# A Low power, Highly Efficient, Linear, Enhanced wideband Class-J mode Power Amplifier for 5G Applications

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***Abstract*—** In wireless communication networks, the necessity for high-speed data rates has increased in emerging 5G application areas. The existing Power amplifier (PA) topologies reported to date demonstrated their potential in achieving desired Power Added Efficiency (PAE) and linearity with the aid of different efficiency enhancement and linearization techniques. However, these harmonically tuned switching power amplifiers are restricted to narrow bandwidth, which makes them less appealing for broadband applications. Therefore, the challenge of designing a power amplifier with improved efficiency by maintaining linearity for a dynamic range of bandwidth becomes increasingly critical for PA designers. Recently developed class-J PA topology has proven its potential to obtain good efficiency while maintaining the linearity for wide bandwidth applications. This research work presents a methodology to design a 5 GHz Class-J mode PA topology using Silterra 0.13-µm CMOS technology. This research's main objectives are to determine the $R_{opt}$ of the transistor and design a proper Output Matching Network (OMN) to obtain Class-J PA operation to make it suitable for 5G wireless applications. The simulation results represent that the proposed Class-J PA provides 27 dBm of maximum power output along with a maximum large-signal power gain of 13.8 dB and the small-signal gain of 17dB for a band with more than 500MHz with a 5V power supply into a 50- Ω load.

***Keywords—5G power amplifier, good efficiency, wide bandwidth, class-J output matching network.***

## I.INTRODUCTION

For the past 40 years, each decade has demanded new technology in the wireless communication industry since introducing the first generation (1G) modern mobile phone systems till the near future fifth-generation (5G) wireless Networks. The emerging 5G technology will enable many new applications that are commonly termed as "5G triangle" [1]. To achieve existing author mistakes and requirements of 5G, the research has been started with various techniques like Millimeter waves, Small base stations, Massive MIMO, Beamforming, Full duplexing to implement base stations that will support the “5G triangle” applications [2].

The essential fact to be considered here is the power consumed by the mobile base stations (BST) as well as wireless devices has to be limited to reduce the energy usage for the overall 5G system compared to the existing 4G networks[3]. In addition to this, with a steady increase in the number of subscribers and new application areas that demand higher data rates, there is a need for enhancement of bandwidth for 5G applications.

It is familiar that the power amplifier (PA) is an important block in all RF transmitters as its Power Added Efficiency (PAE) decides the energy consumed by the overall wireless 5G communication system. Therefore, the emerging 5G cellular network requires advancement in power Amplifier (PA) architectures[4] to provide improved efficiency without sacrificing linearity over a wide dynamic bandwidth. . This research work aims to analyze, design, and implement a Radio frequency power amplifier (PA) that satisfies 5G wireless communication networks.

The main objective of this work is designing and implementing a low power, highly Efficient, linear, Enhanced broadband Integrated Power Amplifier with a proper output matching network (OMN) that suits 5G Applications. The existing Power amplifier structures reported to date [5-11] demonstrated their potential in achieving promising results of Power Added Efficiency (PAE) and linearity. But these techniques will not be beneficial for the enhanced mobile broadband (EMBB) 5G applications due to their narrow bandwidth nature of harmonic terminations. It is essential to design a Power amplifier structure that can provide the possible solution for achieving efficiency over a wide bandwidth and linearity simultaneously and with bandwidth. Out of various modes of power amplifiers (PAs) with different topologies, this research reveals that the Class- J PA introduced and developed by S.C.Cripps in [12] can significantly increase the bandwidth required for near future 5G wireless communication applications. This research mainly deals with a class- J mode Power amplifier's analysis and design using a proper OMN to obtain the expecting outputs such as low power consumption, high efficiency without sacrificing linearity, and enhanced wide bandwidth.

In this work, initially, a **π-**type output matching network (OMN) with lumped lossless components is proposed to achieve Class-J mode operation at 5G frequency by simultaneously matching 50-ohm load resistance and optimum load resistance ($R_{opt}$). The proposed lumped element **π-**matching network was investigated in terms of its bandwidth. The proposed method presents the loss performances and their concerns, power loss performances, and considerations and limitations. The proposed class-J PA simulations performed in the Mentor Graphics EDA tool and this paper's structure are described as follows. A brief review on the efficiency, linearity, and bandwidth achieved by the PAs reported in literature and theory of Class-J PA are discussed in Section II. The selection of proper biasing network and the calculation of $R_{opt}$ that is required to find out the impedances to be given to the transistor for obtaining Class-J mode operation is explained in Section III-A lumped element based **π-** type OMN design for matching 50 Ω output load resistance with the class-J optimum load impedances is presented in Section IV. The simulated schematic Class-J PA circuit and it's simulation results are explained in Section V. The conclusion of this proposed research work is shown in Section VI.

## II. BRIEF REVIEW OF SWITCHING MODE PAS AND THEORY OF CLASS-J POWER AMPLIFIER

To date, many Power amplifier structures reported with different techniques to achieve improved efficiency and linear amplification. Out of those, The design of a single-stage CMOS-based Class-E PA with cascade topology that operates at 2.4GHz center frequency for wireless applications is presented in [5]. Even though Class-E PA has circuit simplicity and provides excellent PAE, it has poor linearity due to its switching operation.A 0.13 µm RF CMOS technology-based two-stage PA designed using MOSFET only bias circuits for 2.4GHz WLAN applications achieves reduced power consumption and improved efficiency. But still, it exhibits poor linearity [6]. A CMOS-based 24GHz PA is proposed with a feedforward canceling path for reducing the third-order intermodulation distortion (IMD3) of the PA. Still, there is a small reduction in gain due to the auxiliary path. [7]. Various efficiency enhancement and linearization improvement techniques of power amplifiers of mobile base stations, requirements and recent trends of 5G technology are presented in [8]. Most of those Power Amplifiers such as Class-E, F, $F^{-1,}$ etc., implemented for achieving high-efficiency amplification are switching in nature, which will not be useful for emerging 5G applications such as enhanced mobile broadband (EMBB) due to their narrowband nature and the circuit complexity. Later on, Doherty PA [9] & [10] and alternate approaches like stacked and multi-gate cell PAs [11] are discussed with narrow B. W and circuit complexity, respectively. To provide a solution for such drawbacks, a newly developed Class-J mode PA by S.C.Cripps in [12] has proved its potentiality in achieving high efficiency and wide bandwidth without sacrificing linearity. A Design methodology for high efficient, linear and broadband Class-J PA mode is demonstrated in [13]. The design of 0.5W GaN-based integrated Class-J PA is presented in [14], which takes output matching network element's losses into account for realizing an on-chip Output Matching, but due to the limitation of device technology and the low-Q on-chip matching network losses, its efficiency and output power are less in comparison with discrete Pas. An integrated CMOS Class-J PA is presented in [15], which takes the effect of threshold voltage into account to analyze $2^{nd}$ harmonic losses for deriving modified design equations. However, the staked FET must be used for implementation because of CMOS PA's low breakdown voltage. A 28 GHz integrated, highly efficient and wideband dual-stage Class -J power amplifier is presented in[16], where output matching is designed with lumped element π-type network. However, this low Q factor Output Matching Network suits for broadband. It degrades the output power. The design of GaN-based fully integrated Class-J PA for 5GHz WLAN 802.11ax systems is presented in [17]. The performance of this PA can be enhanced further by employing DPD. A Class-J PA designed for X-Band is presented in [18], uses the Active Load Modulation technique, and facilitates the PA's integrated implementation by eliminating the doubler and filter networks of conventional class-J2 Pas, and achieves High drain-efficiency. But the broad BW is not achieved due to harmonic tuners. The work can be extended further by increasing the BW of the Phase shifter, and elements in OMN can be replaced using an active inductor.

### *A.Theory of Class-J operation mode*

Class-J is one of the power amplifier modes in which the drain voltage ($V_{DS}$) and drain current ($I_D$) can be obtained as half rectified sinusoidal waveforms with a slight overlap between them. The drain current obtained by selecting the Class B biasing point and by considering only fundamental, second harmonics can be expressed as shown in equation (1)

$$I_D|j(\theta) = \frac{I_{max}}{\pi} + \frac{I_{max}}{2\cos(\theta)} + \frac{2I_{max}}{3\pi\cos(2\theta)} \quad (1)$$

Where $I_{max}$ is the peak value of drain current through the transistor. The half-wave rectified sinusoidal drain voltage $V_{DS}$ can be expressed as shown in equation (2)

$$V_{DS}|\, j = V_{th} + (V_{DD} - V_{th})(1 - \cos(\theta))(1 + \alpha\sin(\theta)) \quad (2)$$

where $V_{DC}$ and $V_K$ are the biasing voltage and knee voltages of the transistor, respectively,

This drain voltage $V_{DS}$ can be obtained by giving complex inductive and pure capacitive load impedances to Class-J mode PA's transistor at the fundamental and second harmonic frequencies. These optimum load impedances are extracted from equations (1) &(2) are shown as follows

$$Zf0 = \frac{(V_{DD}-V_{th})(1+j\alpha)}{Imax/2} = R_{opt} + j\alpha R_{opt} \quad (3)$$

$$Z_2f0 = -\frac{(V_{DD}-V_{th})j\alpha}{2\left(\frac{2I_{max}}{3\pi}\right)} = -\frac{j3\pi}{8}\alpha R_{opt} \quad (4)$$

Where$R_{opt}$ is the optimum resistance which can be expressed as shown in equation (5)

$$R_{opt}=2(V_{DD}-V_{th})/I_{max} \quad (5)$$

With these optimum load impedances presented, we can observe that the drain voltage($V_{DS}$) is getting boosted with a phase shift, as shown in Figure.1.

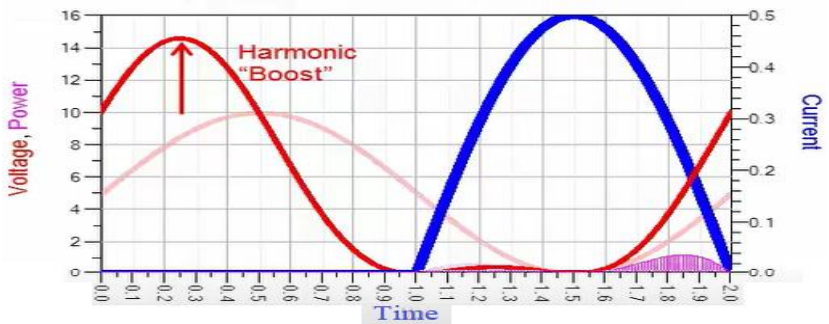


Fig. 1 Class-J voltage and current waveforms at the drain of transitor ($V_{DS}$&$I_D$)

Thus, the phaseshift and boost in drain voltage ($V_{DS}$) causes a slight overlap with drain current ($I_D$), making the class-J power amplifier highly efficient. Even though this waveform shows the feature of switching mode PA, the class-J modePA can provide linearity similar to the class-B or AB modes due to its non-switching mode of operation. Unlike in class B, there is no need for harmonic traps, making it more appealing for broadband applications.

## III. PROPOSED DESIGN METHODOLOGY OF CLASS-J PA IN STANDARD CMOS 0.13 µm SILTERRA PROCESS TECHNOLOGY

As discussed in section-II among various modes of power amplifier (PA) topologies, the Class- J mode PA was introduced and developed by S.C. Cripps in [12] is chosen for this research work because of its potential to provide significant enhancement in bandwidth required for the near future 5G wireless communication applications. From the theory of Class-J operation mode explained in Section II. A , the high-efficiency amplification in broadband can be obtained by giving fundamental ($Z_{f0}$) and second harmonic ($2Z_{f0}$) harmonic optimum load impedances to the NMOS transistor $M_1$ different frequencies over the desired bandwidth as shown in Fig 2.

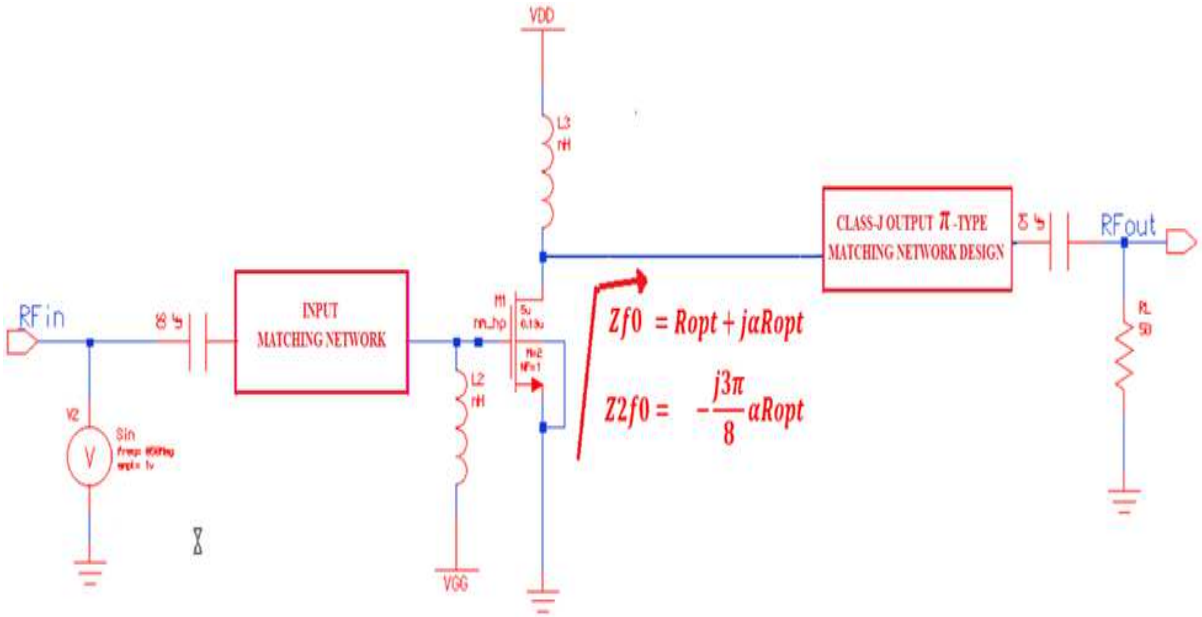


Fig.2 Sample class J mode power amplifier topology

To design the class J mode PA, a proper OMN must be proposed to provide high-efficiency amplification over enhanced bandwidth while maintaining linearity, making the PA suitable for 5G wireless communication applications. The various steps involved in the proposed class J mode power amplifier's design methodology are discussed as illustrated in the flowchart shown in Fig.2(a).

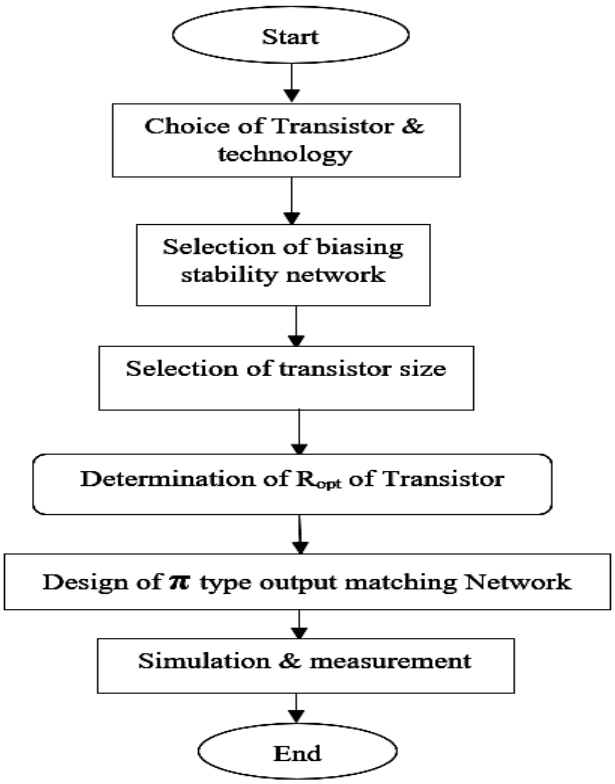


Fig 2(a). Flow chart

**A. SELECTION OF TECHNOLOGY:**

As per the trend of design a power amplifier, the mentor graphics design tool used to design and siltera-130nm technology used for simulation. The nm_hp model MOS transistor is chosen as a high-power transistor in the silterra analogue library. The NMOS transistor threshold voltage ($V_{th}$ ) is determined using its transconductance (gm). To obtain a class-J PA mode, the load impedances as shown in equations (3) and (4) should be presented to this transistor (M1) (i.e., nm_hp) by proper Output Matching Network (OMN).

**B. SELECTION OF BIASING & STABILITY:**

The power amplifier design, can choose any kind of supply voltage. As per design idea of the power amplifier, The supply voltage $V_{DD}$ =5V and Gate voltage $V_{GG} \cong V_K$ (threshold voltage) (i.e., with a quiescent bias current of Iq = 2% of Imax) are chosen to bias nm_hp NMOS transistor ($M_1$) used in this work through fixed bias network to operate as a Class-B PA for obtaining a half rectified sinusoidal drain current ($I_D$),.

One of the most important considerations while designing the power amplifier is that it should be unconditionally stable irrespective of the frequency under normal operating conditions. To ensure PA stability at low-frequencies, a stabilization circuit consisting of an inductor that also provides the path for DC bias to the gate of transistor $M_1$ is employed. Besides, a parallel RC circuit can stabilize the transistor across the entire range of desired frequencies.

## C. SELECTION OF TRANSISTOR SIZE:

Generally, the $R_{opt}$ can be calculated theoretically using equation (5), which depends on the technology and transistor size (or Pout) chosen, and it can be practically determined by conducting LOADPULL simulations**.** As there is no smith chart utility for conducting load-pull simulations, the mentor graphics EDA tool is used for this research work. Initially, a $R_{opt}$ value = 4.5 Ω determined by load-pull simulations is taken as a reference. This $R_{opt}$ value is obtained by altering transistor size in terms of aspect ratio. Because $R_{opt}$ value can be determined using $I_{D,}$ which depends on the transistor's aspect ratio (W/L). For corresponding $V_{DD}$ and $V_{GS}$ values, the transistor size (i.e., 2×5μm) is selected to realize $M_1$to obtain a maximum drain current of about 2.1 A. For $V_{DD}$ = 5V, $V_K$ =0.486V and maximum drain current $I_{max}$=2.1A, the optimum resistance obtained using equation (5) is $R_{opt}$ = 4.3Ω. Using this $R_{opt}$, the theoretical values of optimal load impedances at fundamental and second harmonic frequencies are determined using (3) and (4) as $Z_{f0}$ =4.3+ jα 4.3Ω & $Z_{2f0}$ =-j 5.2 Ω respectively. To verify these theoretically calculated optimum load impedances and to match the load resistance **(RL=50 Ω)** with at least the real part (i.e., $\mathbf{R_{opt}}$) of obtained optimum load impedances that have to be presented to the transistor M1 over a wide Bandwidth proper output matching network (OMN) has to be realized. The desired matching in wideband can be achieved by realizing a high-order output matching network (OMN), which may need a minimum of two series inductors when lumped elements are used. But due to the losses of integrated inductors used in OMN, the power output and the efficiency of PA will be reduced, This reduction is higher than the reduction caused by the load impedance mismatch. A simplified **π**-type OMN with one inductor and two capacitors is chosen for this Class-J PA design, as explained below.

## IV. OUTPUT (π) -MATCHING NETWORK DESIGN

The design of a proper OMN for obtaining Class-J operation mode is challenging as it has to match the output load of RL=50 Ω with the optimum load impedances $\mathbf{Z_{f0}}$ **&** $\mathbf{Z_{2f0}}$ of transistor $M_{1.}$ Out of different methods for realizing OMN such as lumped element matching (i.e., L, T, π topologies) and distributed matching (i.e., using transmission line networks), Initially a lumped element **π**- matching network is chosen for this work because the distributed matching using transmission lines occupies a larger area which in turn increases the cost.

Initially, the **π**-type OMN is designed for a Bandwidth of 500 MHz with the center frequency of 5 GHz (i.e., sub 6 GHz) as the proposed PA has to be operated at 5G frequency. With the desired Bandwidth and center frequency, the quality factor can be calculated as Q = f/BW. In this work, the general design procedure of π- matching network in which the π section will be split into two back-to-back connected L -sections as shown fig .3 is used.

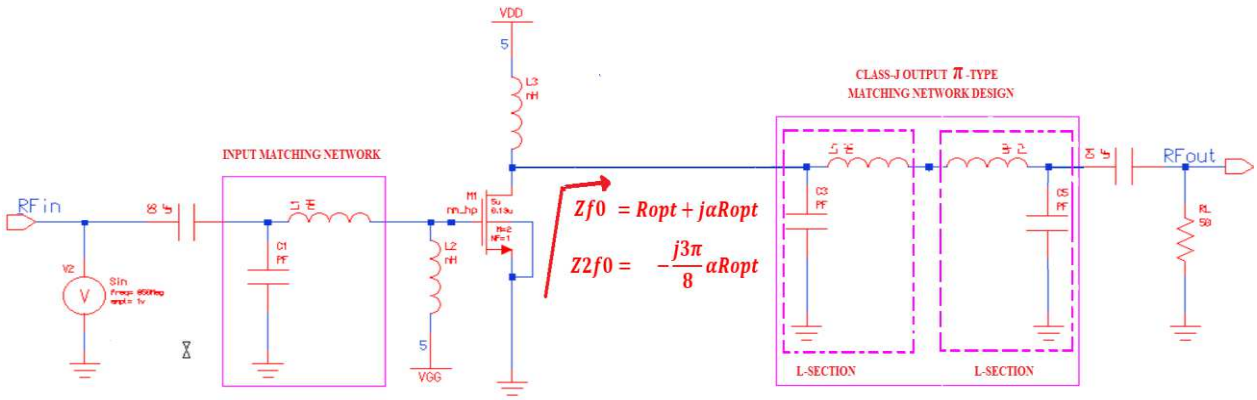


**Fig.3** Sample class J mode power amplifier topology with **π-**matching network

So, the elements of Pi type OMN use the formulae of the L-type matching network. Initially, as π section is split in to 2 back-to-back connected L -sections. The load resistance seen by the first L -section is assumed as Rv [i.e., $R_V$=$R_L$], which can be obtained in terms of $R_{opt}$ as

$$R_v = \boldsymbol{R_{opt}} / (Q^2 + 1) \quad (6)$$

In which the Q is the quality factor that can be expressed as f /B. W where f and BW have desired input frequency and Bandwidth, respectively.

Now with values of Q and $R_V$ the inductor $L_1$ value can be calculated as:

$$XL_1 = QR_L = QR_V\ \Omega \quad (7)$$

$$L_1 = X_{L1}/2\pi f \quad (8)$$

The capacitor $C_1$ value can be calculated as:

$$XC_1 = R_{OPT}/Q \quad (9)$$

$$C_1 = 1/2\pi f X_{C1} \quad (10)$$

In the second L-section, $L_2$ and $C_2$ can be calculated by assuming the value of [$R_V$ = $R_{opt}$] with the load resistance $R_L$ of 50**Ω**.

The L-network relationship can define the quality factor Q of this second L section as

$$Q_{new} = \sqrt{((R_L / (R_{OPT} = R_V)) - 1]} \quad (11)$$

The inductance L2 value can be calculated as:

$$XL_2 = Q_{new} R_{OPT} \quad (12)$$

$$L_2 = (X_{L2}) /2\pi f \quad (13)$$

The capacitor $C_2$ can be calculated as

$$XC_2 = R_L/Q_{new} \tag{14}$$

$$C_2 = 1/2\pi f X_{C2} \tag{15}$$

The capacitance $C_1$ of the π- matching network should be chosen carefully so that it has to take output parasitic capacitance $C_{DS}$ of the transistor into account because this capacitance at the higher order harmonic frequencies is considered as a short circuit . Once the OMN is designed, the capacitive reactance to the load line resistance ratio [$X_{CDS}$ /$R_L$] needs to be calculated. Suppose this ratio is (<=) 1, then the matching network design is considered ideal. But, depending on the device technology used and the frequency, this ratio can also be above the unity.

## V. SIMULATION RESULTS

As explained in sections III &IV, a class-J PA is designed using standard CMOS 130 nm silterra process technology in the MENTOR GRAPHICS EDA tool. As discussed in section III, the theoretically calculated reference $R_{opt}$ value using equation (5) is 4.3 Ω. To verify this theoretically calculated reference $R_{opt}$, We should obtain the values of threshold voltage ($V_{th}$) and the peak drain current ($I_{Dmax}$ )of the chosen NMOS transistor (i.e., nm_hp model NMOS). The threshold voltage ($V_{th}$) of the transistor can be extracted from the value of transconductance (gm), which is a figure of merit to indicate how well the device converts the voltage to current. It can be represented as $dI_D/dV_{GS}$.Using the waveform calculator utility of the EZ wave plot in the MENTOR GRAPHICS EDA tool, the drain current ($I_{DS}$) is differentiated w.r.t $V_{GS}$ to get transconductance( gm). After obtaining the transconductance( gm) value, it is also differentiated w.r.t $V_{GS}$ to extract threshold voltage (Vth). The gate voltage $V_{GS}$ at which the dgm /$dV_{GS}$ value is maximum is considered as the threshold voltage (Vth) as shown in Figure 4.

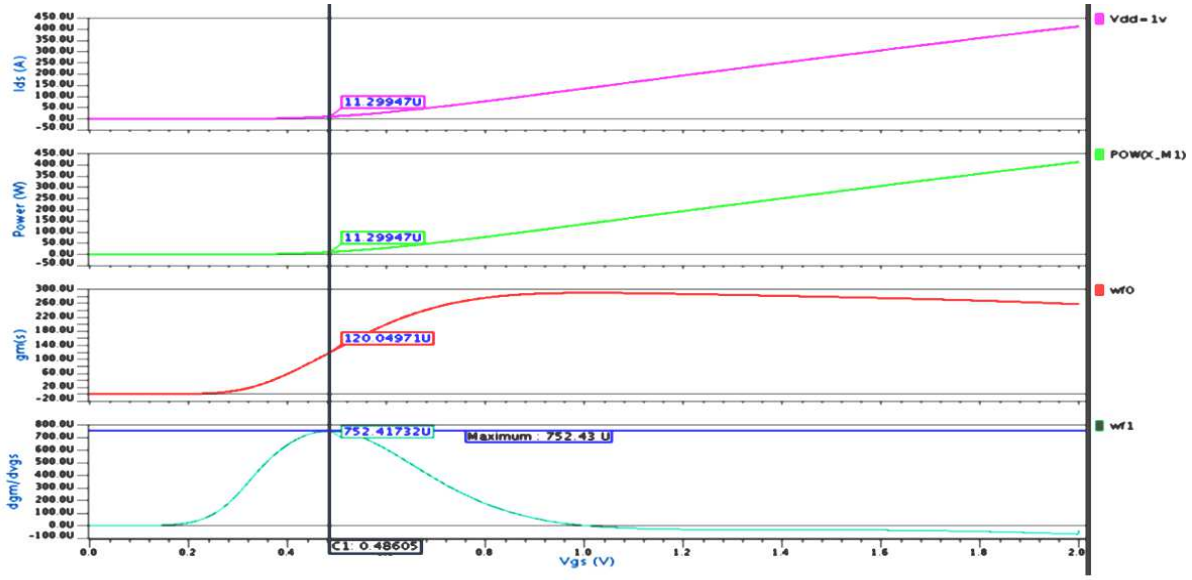


Fig. 4. $V_{th}$ of nm_hp model NMOS transistor

After extracting the threshold voltage($V_{th}$), to obtain the maximum drain current $I_{Dmax}$ corresponding to the chosen reference $R_{opt,}$ Class-B biasing point is chosen. The transistor's sizing is selected as explained in Section III.C. The peak value of drain current $I_{Dmax}$ obtained for the transistor's biasing and sizing and the corresponding $R_{opt}$ value calculated using the waveform calculator, which is almost the same as the theoretically calculated reference $R_{opt}$ value as shown in figure 5.

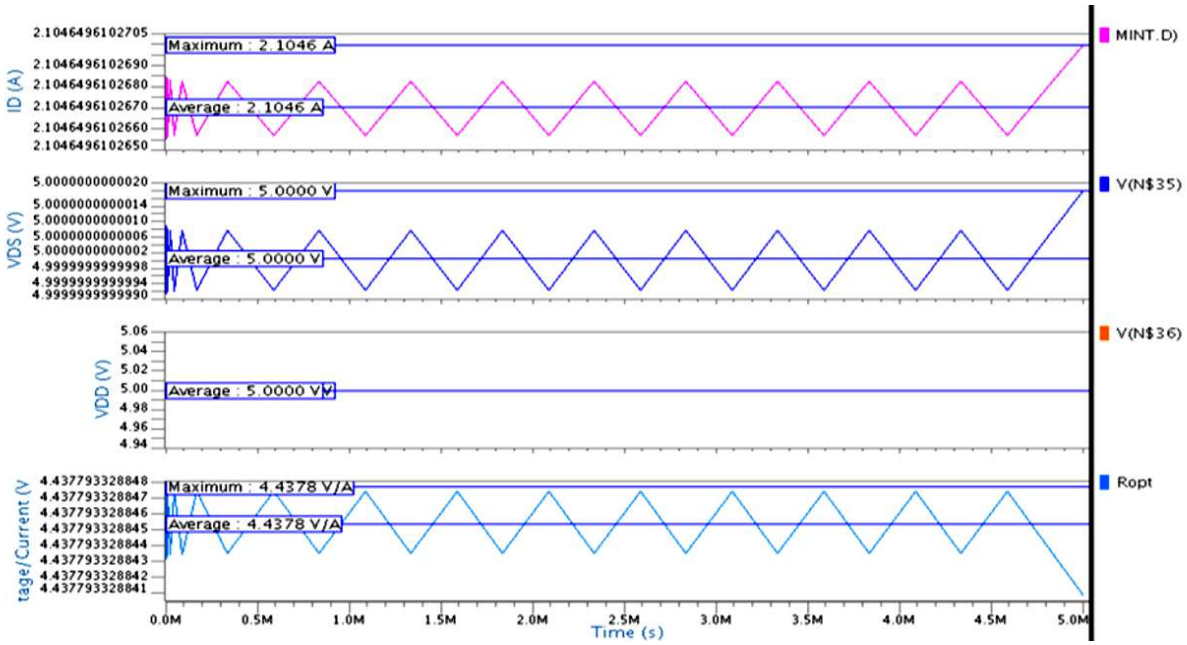


Fig.5. $R_{opt}$ obtained from the waveform calculator

By taking the $R_{opt}$ obtained from the waveform calculator as reference (i.e., $R_2$)initially, a π-matching network with a sinusoidal input source at 850MHz frequency is designed using the design equations discussed in section IV to verify whether the maximum power is getting a transfer from the source to load. The schematic circuit of the π-matching network to match $R_L$(i.e., $R_3$) with $R_{opt}$ (i.e., $R_2$) and its transient response are shown in figures 6(a) & 6(b).

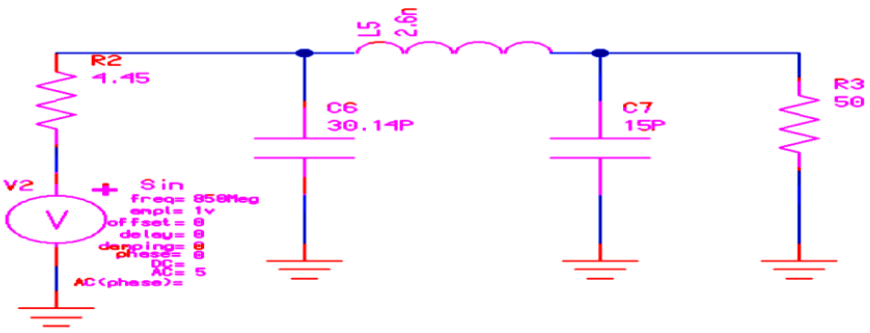


Fig.6(a). Schematic circuit of the π-type matching network

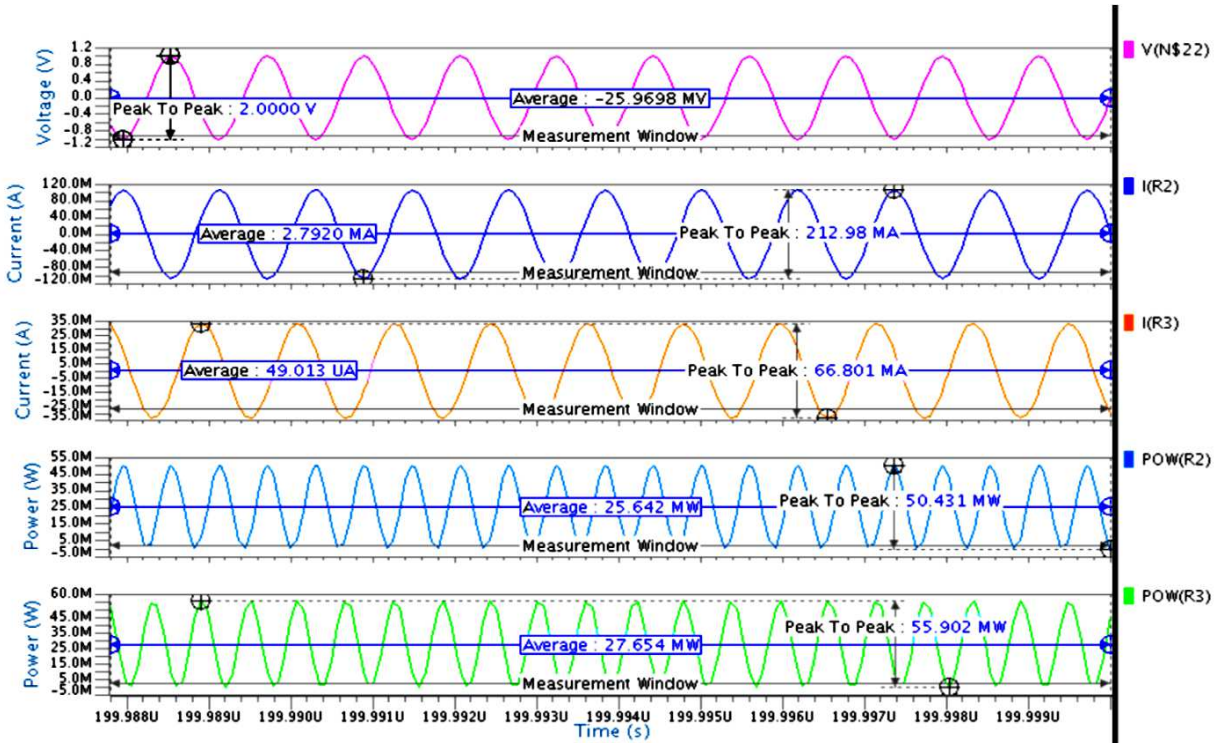


Fig.6(b). Transient response of $\boldsymbol{\pi}$-type matching network

From the graph shown in fig6(b), it can be observed that for a sinusoidal input source with a peak to peak of 2V (i.e., the amplitude of 1V ) at 850MHz frequency, the power measured across Load resistance $R_3$(i.e., $R_L$) is 27mW which is nearly the same as the power measured across the source resistance $R_2$ (i.e$R_{opt}$) is 26mW even though the average current across load resistance is less(i.e., 49μA) compare to the average current across source resistance (i.e., 2.8mA) which means that the maximum power is transferred to load resistance from source resistance by means of a $\boldsymbol{\pi}$-type matching network as shown in Fig6.(a).

Initially, the proposed Class-J PA is designed by realizing this π-matching network with a sinusoidal input source at 850MHz. The schematic Class-J PA circuit and its transient response are shown in Figures 7(a) & 7(b).

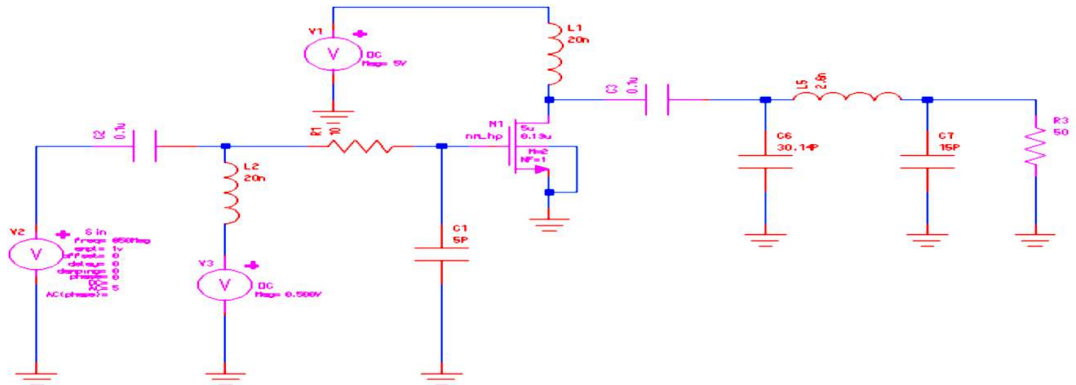

Fig.7(a). The schematic circuit proposed a Class-J PA with a sinusoidal input source at 850MHz.

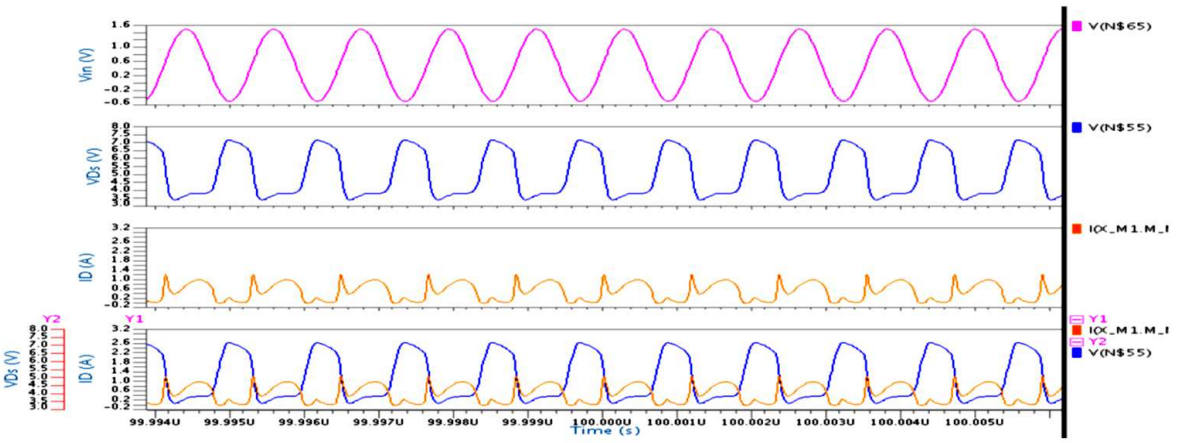


Fig.7(b). Transient response of proposed class J power amplifier with sinusoidal input source at 850MHz

The simulated transient response waveforms shown in Fig.7(b) are obtained by presenting the required optimum load impedances in terms of $R_{opt}$ at fundamental and second harmonic frequencies to the transistor to realize the $\boldsymbol{\pi}$-type matching network.

The proposed Class -J power amplifier is designed by realizing this π-matching network with a Fourier input source at 850MHz as RF input. The schematic Class-J PA circuit and its transient response are shown in figures 8(a) & 8(b).

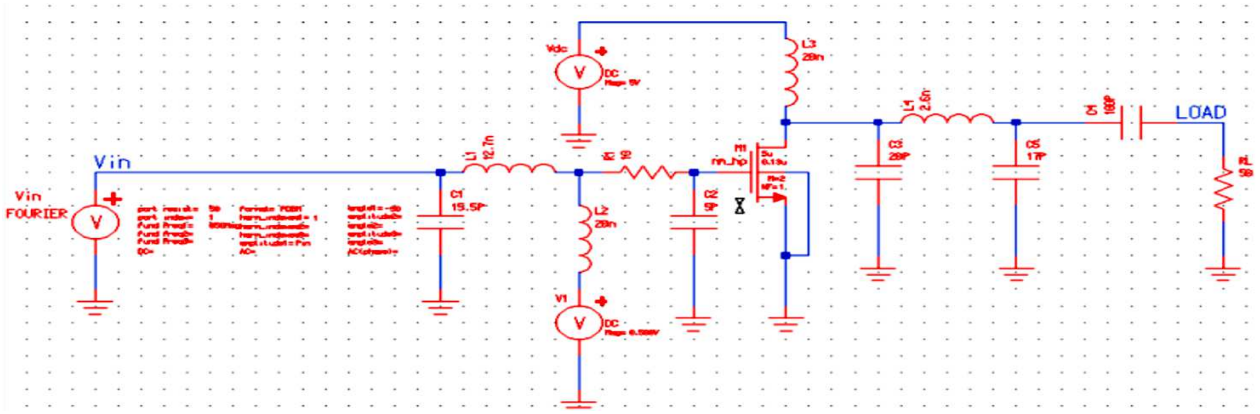


Fig. 8(a). Schematic circuit of the proposed class J power amplifier with Fourier input source at 850MHz.

The simulated voltage and current waveforms at drain of the transitor ($V_{DS}$ & $I_D$) are shown in fig.8(b). We can observe that nearly half rectified drain current ($I_D$) is obtained due to class B biasing. The drain voltage ($V_{DS}$) is obtained as a half rectified sine wave with the harmonic boost and phase shift in it by presenting optimum load impedances to transistor $M_1$ at fundamental and second harmonic frequencies, which exhibits the Class-J PA mode as explained in section II.

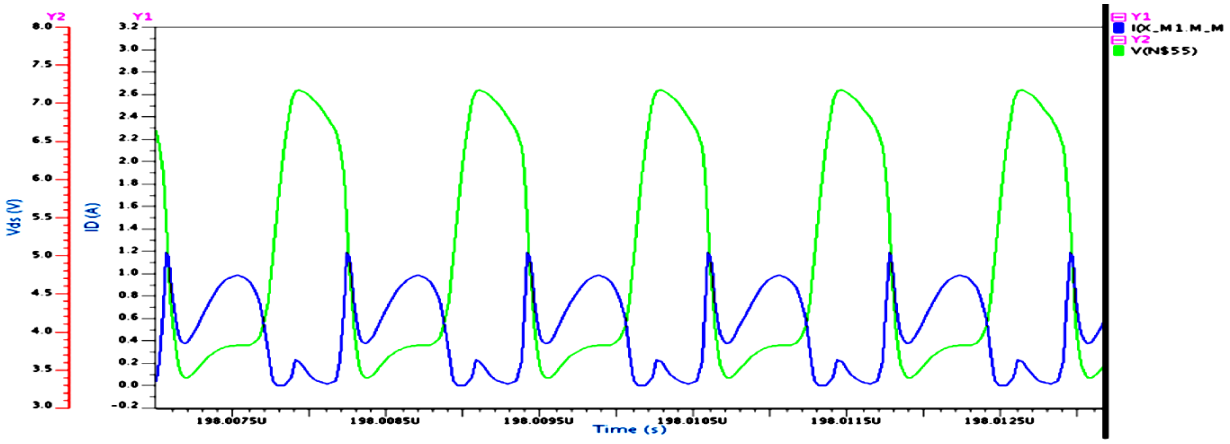


Fig.8(b). Intrinsic voltage and current waveforms at the drain of proposed Class-J PA ($V_{DS}$ &$I_D$) with Fourier input source at 850MHz

After obtaining the expected Class-J mode voltage and current waveforms, the important performance parameters such as power Gain, Pin dBm, power Output (Pout dBm), Power Added Efficiency (PAE), and Drain efficiency (DE) of designed PA needs to be obtained. The extraction of these parameters is performed for each Pin value swept during parametric sweeping using Steady-state (SST) analysis.Theoretically, the Drain Efficiency(D.E) can be calculated as output power delivered to load divided by DC power consumed by the PA, Power Added Efficiency (PAE) can be calculated as the difference between output power and input power devided by the total DC power consumption and the gain can be calculated by subtracting the input power from the output power when measured in dB. These parameters are obtained in graphical representation by typing these theoretical formulae as. EXTRACT commands in the SST analysis command window in the Mentor graphics EDA tool. The steady-state analysis results of performance parameters for the Class-J PA designed at 850 MHz center frequency are shown in Fig.8(c)

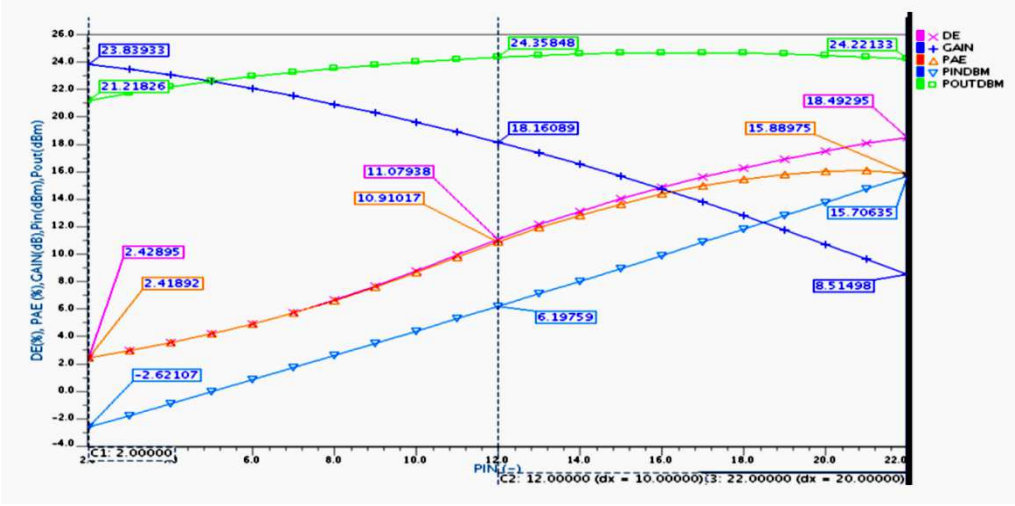


Fig. 8(c). Measured gain, output power (Pout dBm), PAE, PE, as a function of input power (Pin=2dBm-22dBm) at 850MHz.

As this research work is mainly focused on the design of PA that suits for 5G wireless communication applications, later on, the same proposed class J power amplifier is designed by realizing this π-matching network with Fourier input source at a 5-GHz frequency (i.e., sub-6-GHz suits for 5G technology) as RF input. The schematic Class-J PA circuit and its transient response are shown in Figures 9(a) & 9(b).

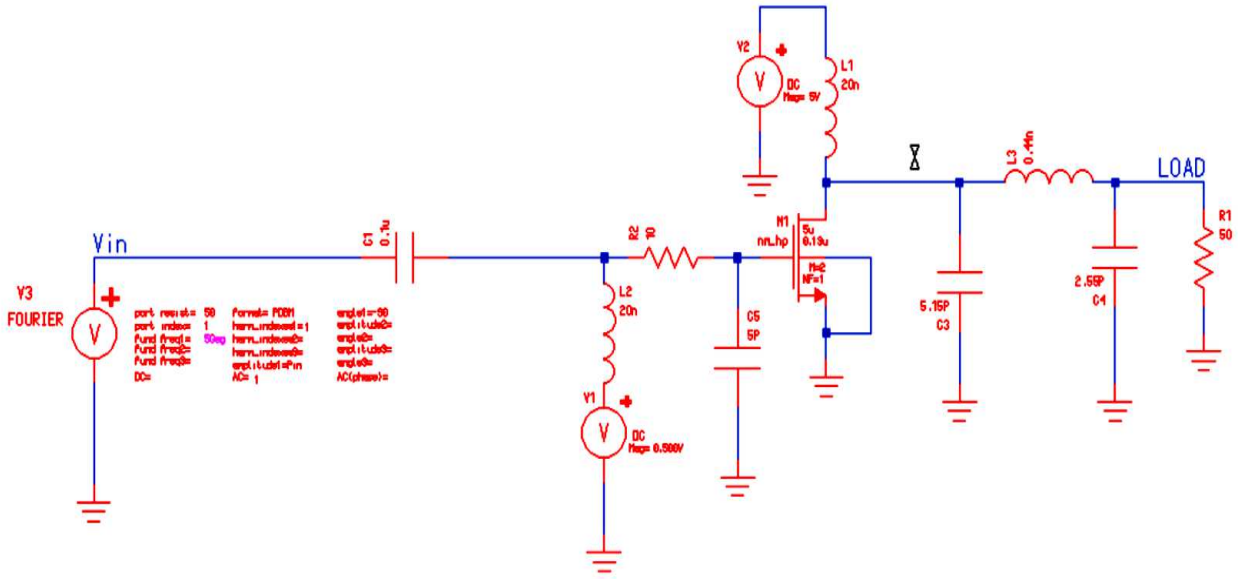


Fig. 9(a). Schematic circuit of the proposed Class-J PA with Fourier input source at 5GHz.

The waveforms of voltage and current at the drain of the transistor ($V_{DS}$ &$I_D$) obtained from the simulation of Class-J PA with the proper realization of the $\boldsymbol{\pi}$-matching network at 5GHz frequency will exhibit a phase overlap between them as shown in Fig.9(b), and these waveform shapes are similar to the waveforms reported in [10], It is the key feature of the Class-J mode PA as explained in section II.

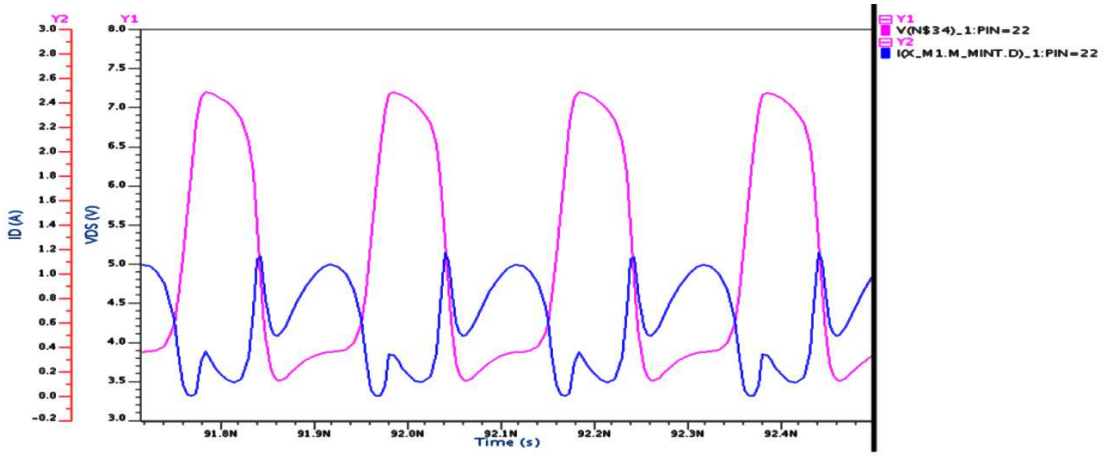


Fig.9(b). Intrinsic voltage and current waveforms at the drain of proposed Class-J PA ($V_{DS}$ &$I_D$) with Fourier input source at 5GHz

The important steady-state analysis results of performance parameters such as Gain, Pin dBm, Pout dBm, PAE and DE of the Class-J PA designed at 5GHz center frequency that was obtained in the same manner as explained for the Class-J PA at 850 MHz center frequency in Fig.8(c) are represented in Fig.9(c).

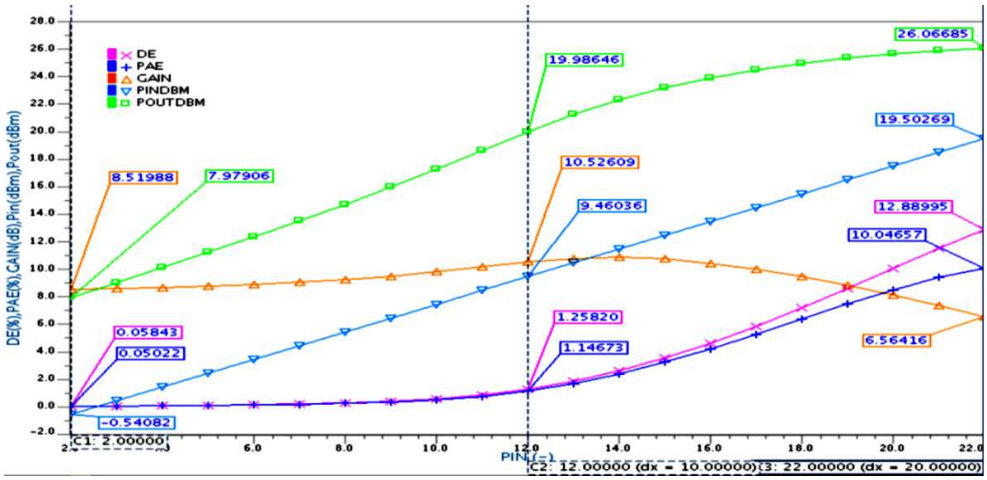


Fig.9(c). Measured gain, output power (Pout dBm), PAE, PE, as a function of input power (Pin=2dBm-22dBm) at 5GHz

As an alternate approach to find the accurate $R_{opt}$ value, the output impedance of the nm_hp NMOS transistor $Z_{out}$ is calculated using the .def wave command in terms of S-parameters obtained from the schematic circuit shown in Fig.10 (a).

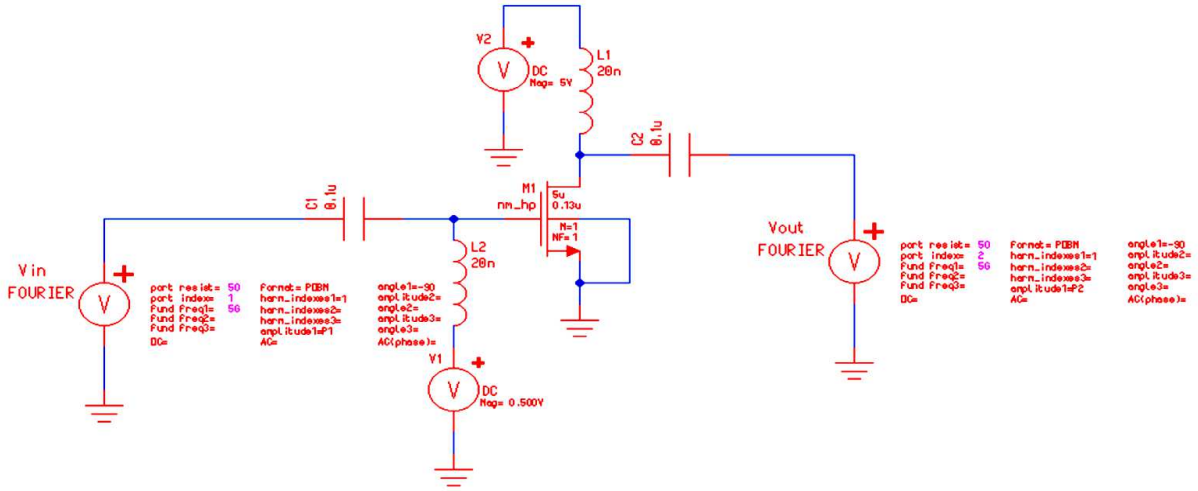


Fig.10(a) S-Parameter and $Z_{out}$ extraction of nm_hp NMOS Transistor at 5GHz frequency

The maximum small signal gain $S_{21}$ that can be achieved from the S-parameter a simulation is 17 dB at 5 GHz as shown in Figure 10(b).

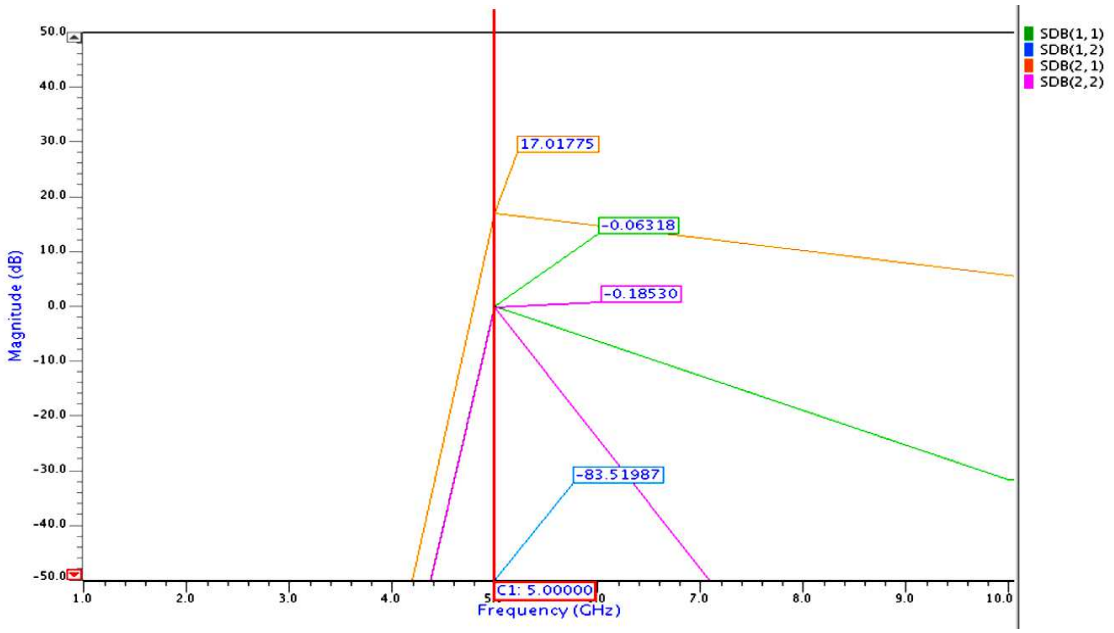


Fig 10 (b) S parameters of nm_hp NMOS Transistor at 5GHz frequency

After simulating class J PA, the small-signal gain obtained over the frequency 4.3-5.6 GHz is 16.85 dB, as shown in Fig10(c)

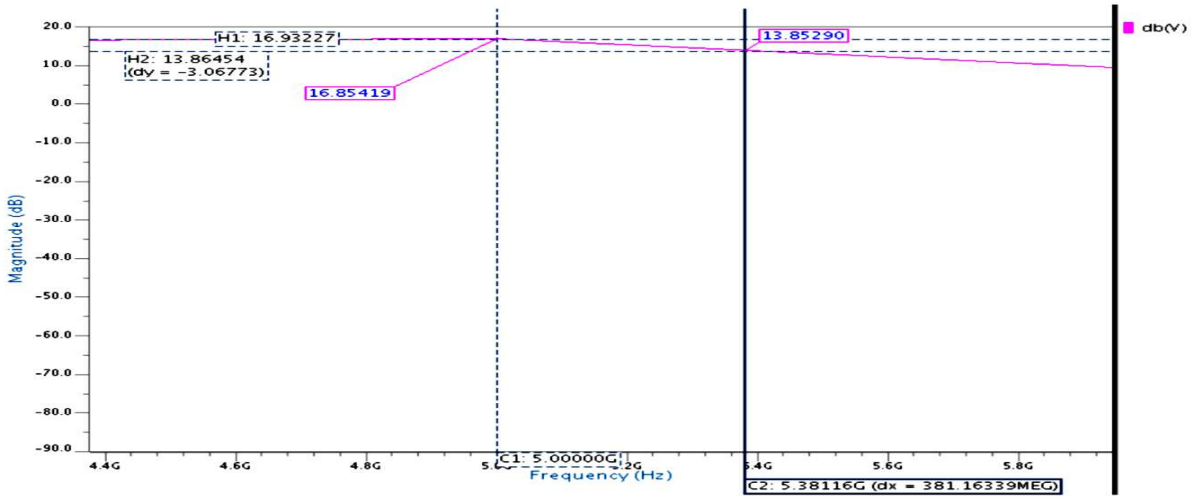


Fig. 10(c) small-signal gain obtained from AC analysis of class J PA

Based on the $R_{opt}$ value obtained, including $Z_{out}$ of transistor, the proposed class J power amplifier is designed by realizing this $\boldsymbol{\pi}$-matching network with Fourier input source at a 5-GHz frequency. The schematic circuit and its transient responses are shown in Figures 11(a) & 11(b).

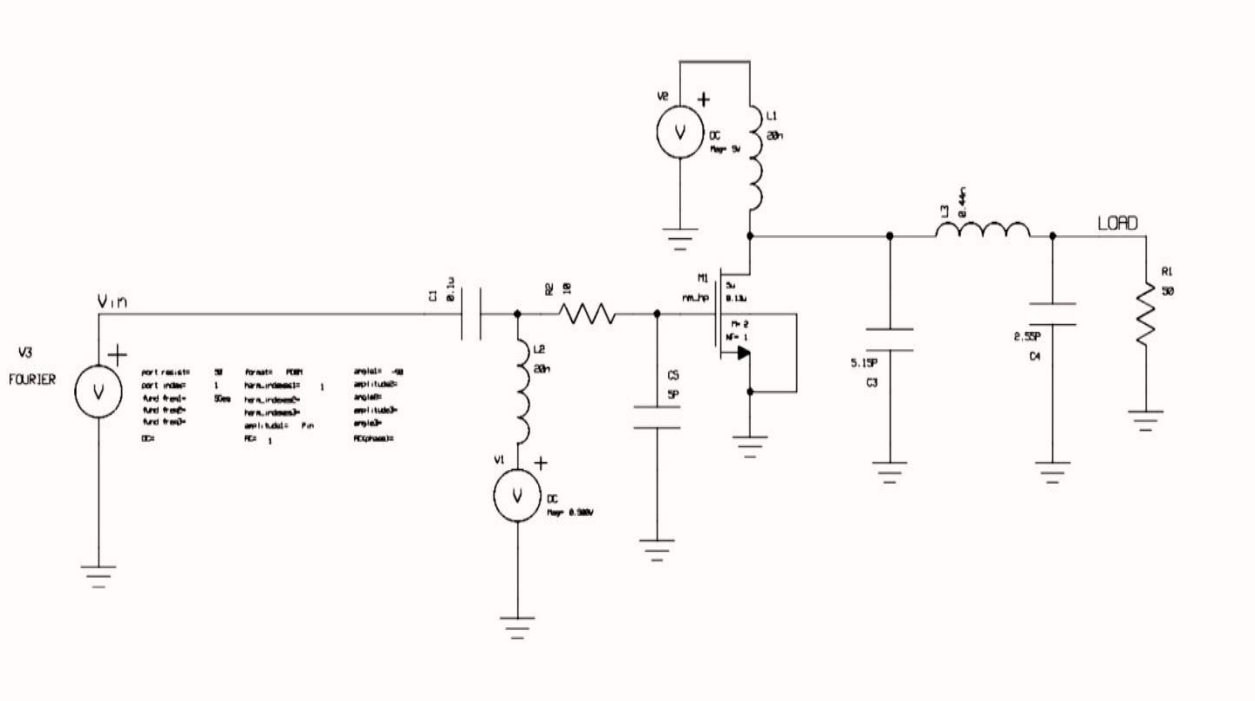


Fig. 11(a). Schematic circuit of the proposed Class-J PA with Fourier input source at 5GHz.

The simulated voltage and current waveforms at the drain of the transistor ($V_{DS}$ &$I_D$) are obtained similarly as explained in Fig 9(b) are shown in fig.12(b), which exhibits the key feature of Class-J PA mode as discussed in Section II.

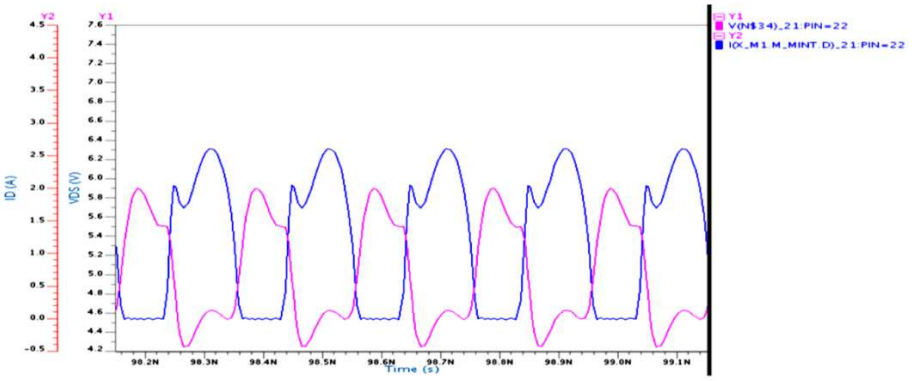


Fig.11(b). Intrinsic voltage and current waveforms at the drain of proposed Class-J PA ($V_{DS}$ &$I_D$) with Fourier input source at 5GHz

The important steady-state analysis results of performance parameters such as Gain, Pin dBm, Pout dBm, PAE, and DE of the Class-J PA designed based on the Ropt value obtained, including Zout of the transistor at 5GHz center frequency that was obtained in the same manner as explained for the Class-J PA designed at 850 MHz center frequency in Fig.8(c) are shown below in Fig.11(c) obtained

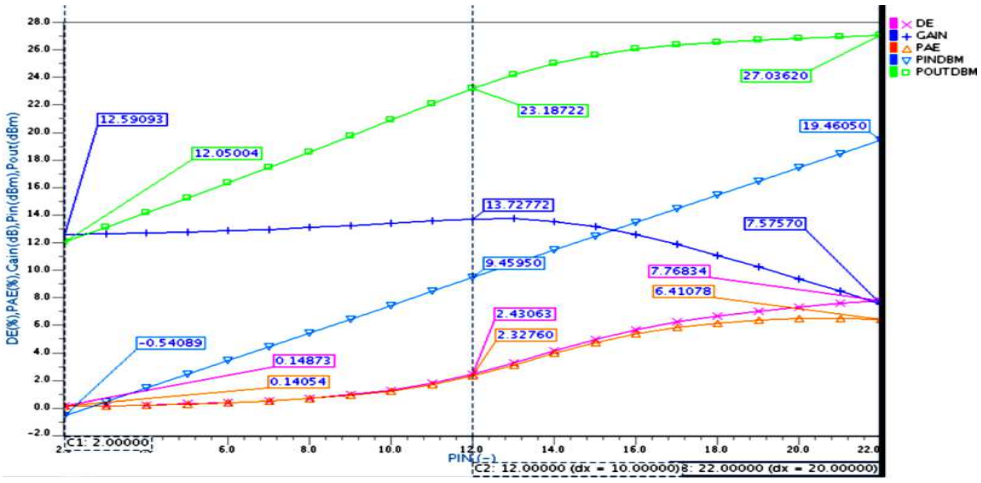


Fig.11(c). Measured gain, output power (Pout dBm), PAE, PE, as a function of input power (Pin=2dBm-22dBm) at 5GHz

In Table-3, the maximum /peak values of the performance parameters are computed with an.EXTRACT command using MAX function using the SST analysis command window are a summarized. From this table -3, the proposed class J PA provides 24 dBm of maximum power otput with a maximum large-signal power gain of 23.8 dB. over a bandwidth of 212MHz at a centre frequency of 850MHz for a 5V supply to a 50 Ω load. But when the same class J PA is designed at the centre frequency of 5GHz, it provides a maximum power output of 26 dBm with a maximum large-signal power gain of 10.5 dB. over the bandwidth of 500 MHz.It is also observed that a maximum power output of 27 dBm with a maximum large-signal power gain of 13.8 dB. over the bandwidth of 500 MHz was obtained when the same Class-J mode PA designed based on the Ropt value obtained, including Zout of transistor extracted from S-parameter analysis at 5GHz centre frequency.

**Table-3**

| **Value** | **Frequency 850MHz** | **Frequency 5GHz** | **Frequency 5GHz** |
|---|---|---|---|
| **Feature** | Class-J | Class-J | Class-J |
| **Freq.** | 850 MHz | 5 GHz | 5 GHz |
| **VSupply [V]** | 5 | 5 | 5 |
| **Gain [dB]** | 23.8 | 10.5 | 13.8 |
| **Pout[dBm]** | 24 | 26 | 27 |
| **PAE max [%]** | 16 | 20 | 6.5 |
| **DE max [%]** | 18 | 13 | 8 |
| **BW [MHz]** | 212 | 500 | 500 |

**Table -4**

Performance Comparison Of Class -J PAs

| REF | This work | [12] |
|---|---|---|
| CMOS Technology | 130 nm | 180nm |
| Feature | Class-J | 2 stack/Class-J |
| VSupply [V] | 5 | 3.3 |
| Frequency. | 5 GHz | 3.5 GHz |
| BW [GHz] | 4.3-5.4 | 2.1-4.5 |
| Pout[dBm] | 27 | 22 |
| Small signal Gain [dB] | 17 | 17.4 |
| Max power gain [dB] | 13.8 | - |

Table 4 summarizes CMOS PA reported in [12] and this research work. The proposed Class-J PA has obtained a similar small-signal gain while achieving higher peak output power and power gain. This Class-J PA topology is simple to compare to the switching mode PAs.Therefore, the Class-J PA is more feasible for integration.

## IV.CONCLUSION

A 5GHz Class-J PA with output matching designed using a lumped π-type network is presented in this paper. This class-J PA obtained a peak output power of 27 dBm, a maximum large-signal gain of 13.8 dB, and a small signal gain of 17dB at 5GHz.A small overlap is observed between the half-wave rectified voltage and current waveforms at the drain, which is the class-J mode PA's key feature. Even though this waveform shows the feature of switching mode PA (i.e., the power dissipation across the transistor is very less), it can provide the linearity similar to the class-B or AB modes due to its non-switching mode of operation. , There is no need for harmonic traps, unlike in class B, which makes it more appealing for broadband applications. The bandwidth, PAE, and DE of the proposed Class-J PA have to be enhanced. This work is in progress to achieve High PAE and BW enhancement.

## ACKNOWLEDGEMENT

We would like to express our sincere thanks to the Multimedia University and Ministry of Higher Education (MOHE), Malaysia, for funding this research work through FRGS.

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# Figures

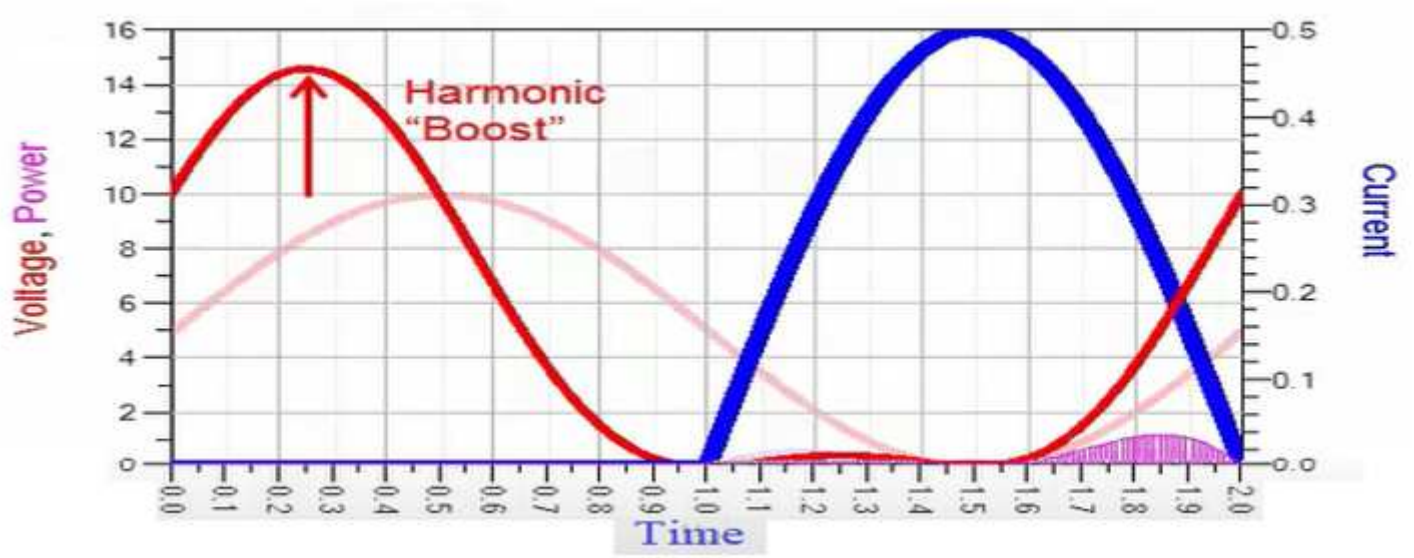
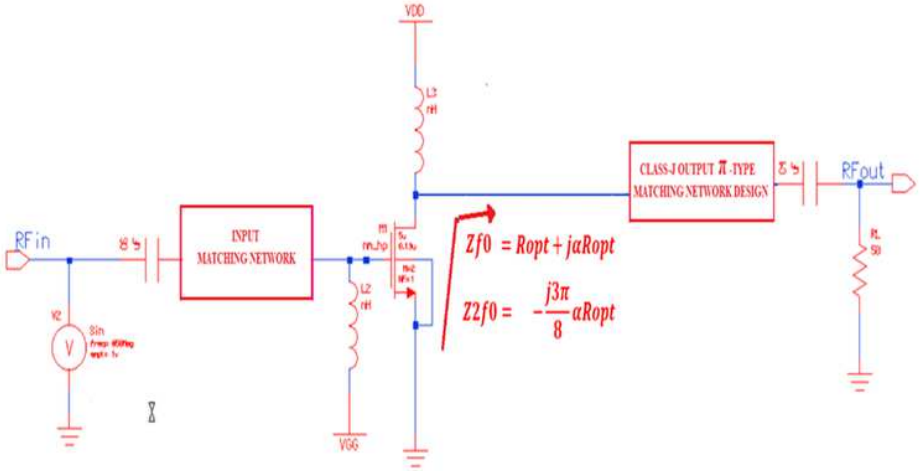



**Figure 1**

Class-J voltage and current waveforms at the drain of transitor (VDS&ID)



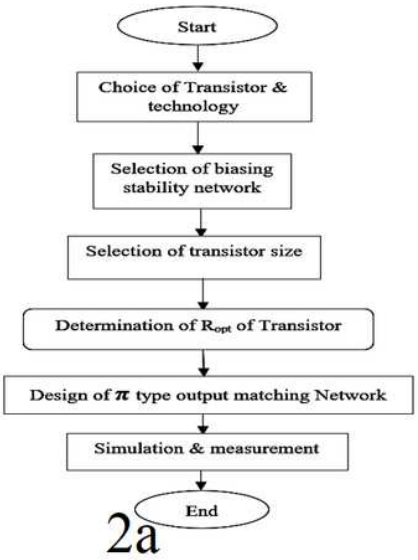
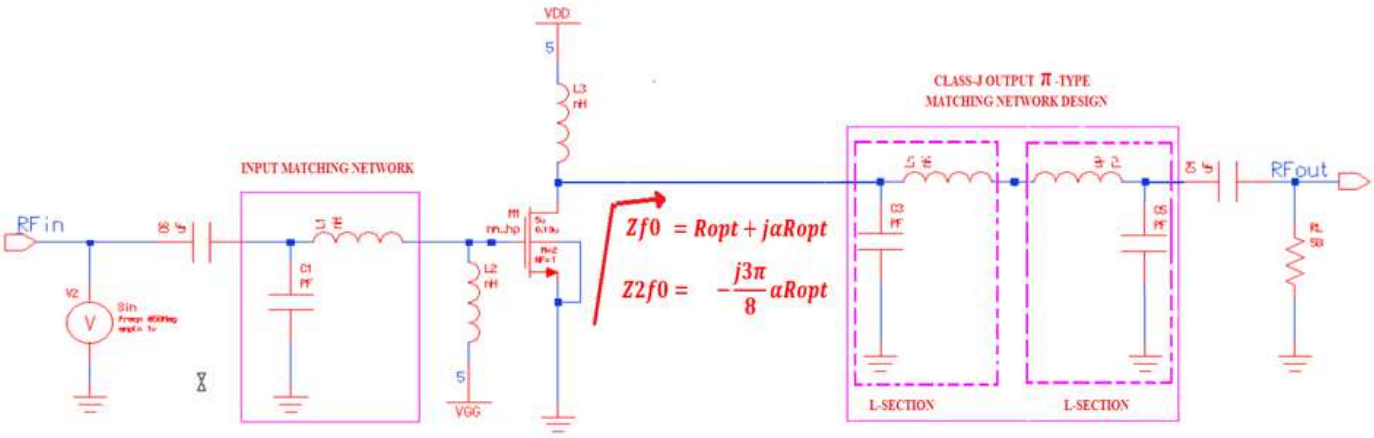



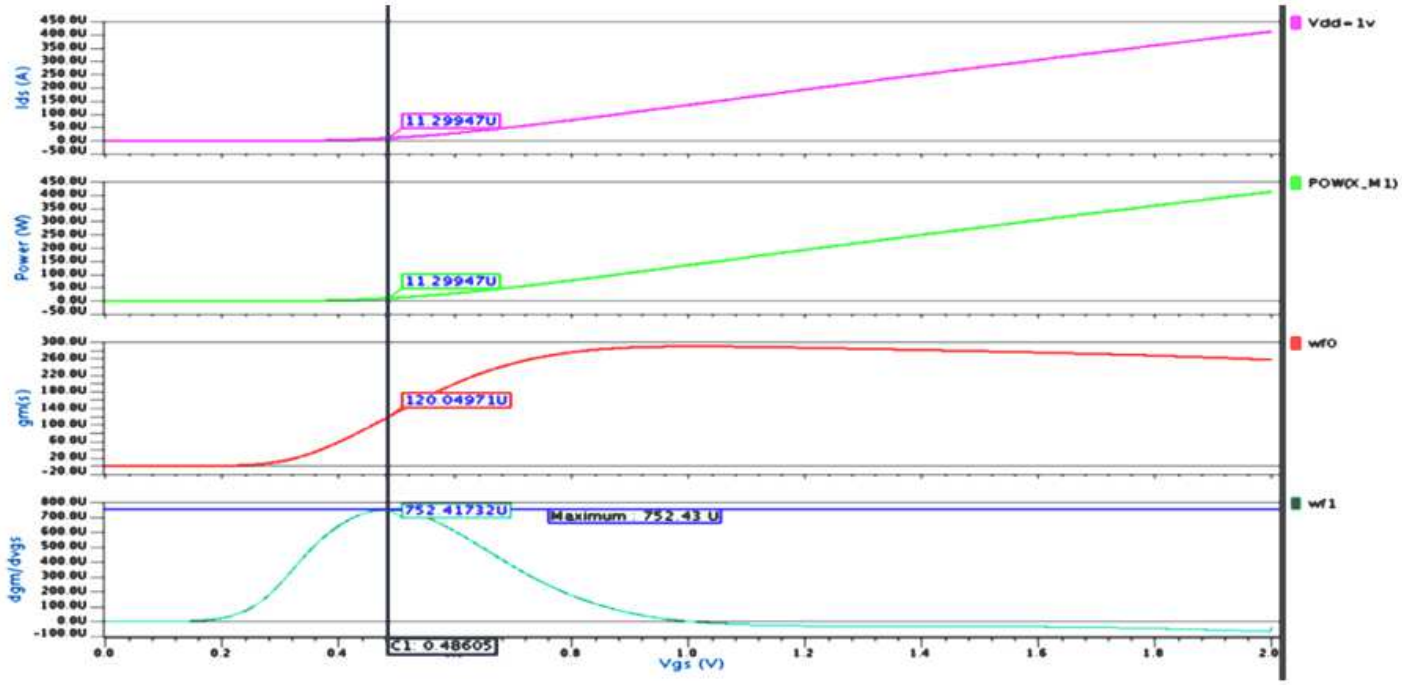

**Figure 2**

Sample class J mode power amplifier topology 2(a). Flow chart



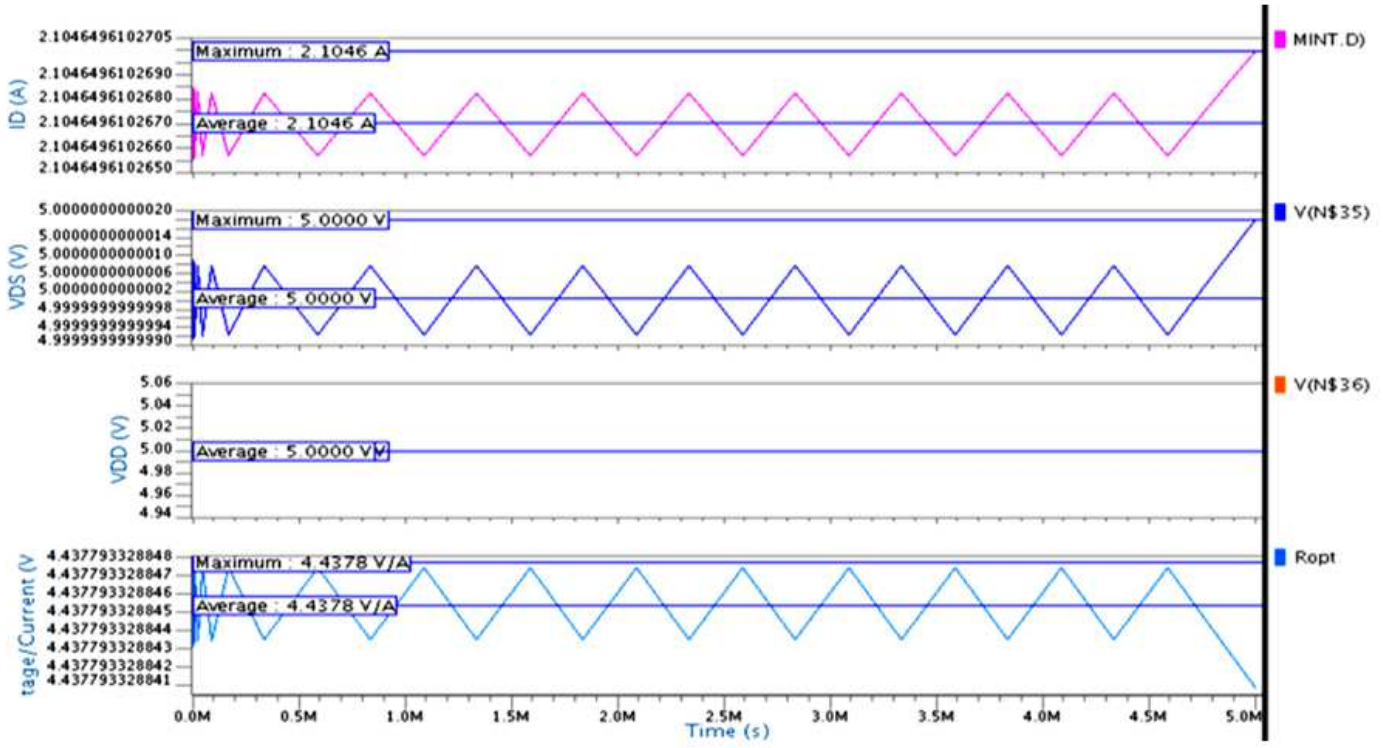

## Figure 3

Sample class J mode power amplifier topology with π-matching network



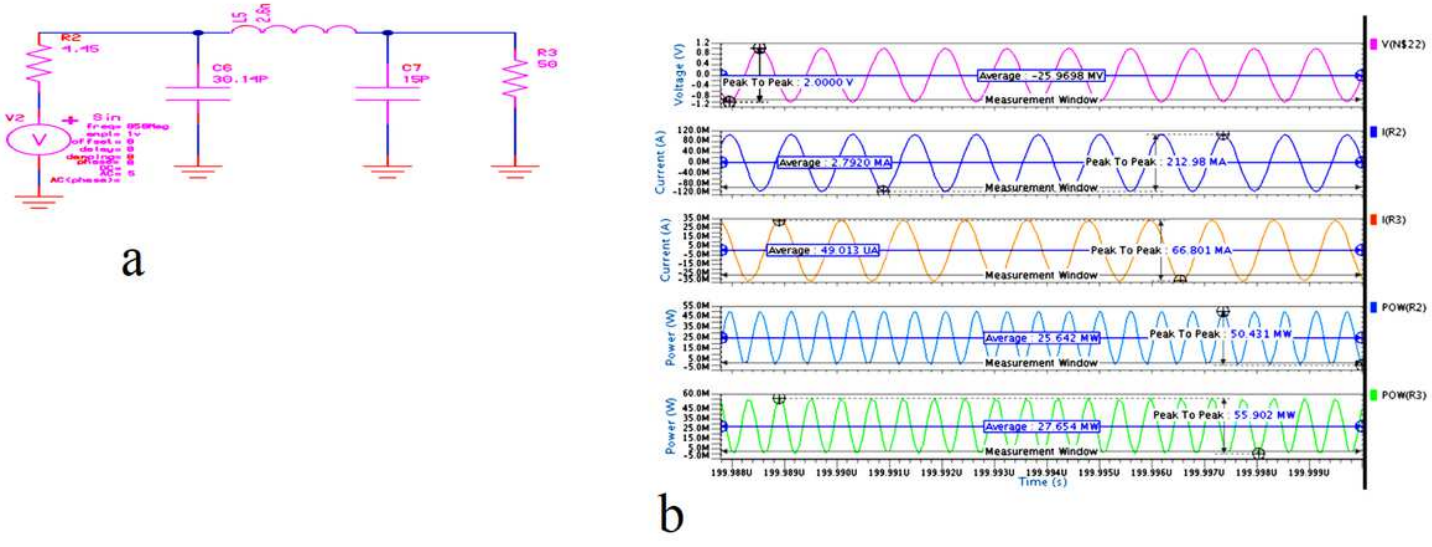

## Figure 4

Vth of nm_hp model NMOS transistor




## Figure 5

Ropt obtained from the waveform calculator




## Figure 6

(a). Schematic circuit of the π-type matching network (b). Transient response of π-type matching network

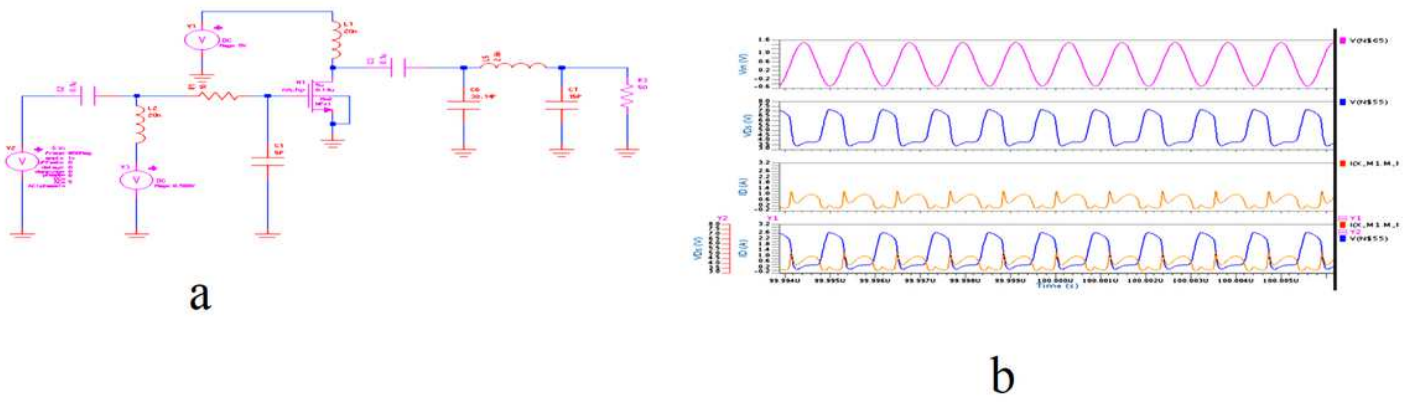



**Figure 7**

(a). The schematic circuit proposed a Class-J PA with a sinusoidal input source at 850MHz. (b). Transient response of proposed class J power amplifier with sinusoidal input source at 850MHz

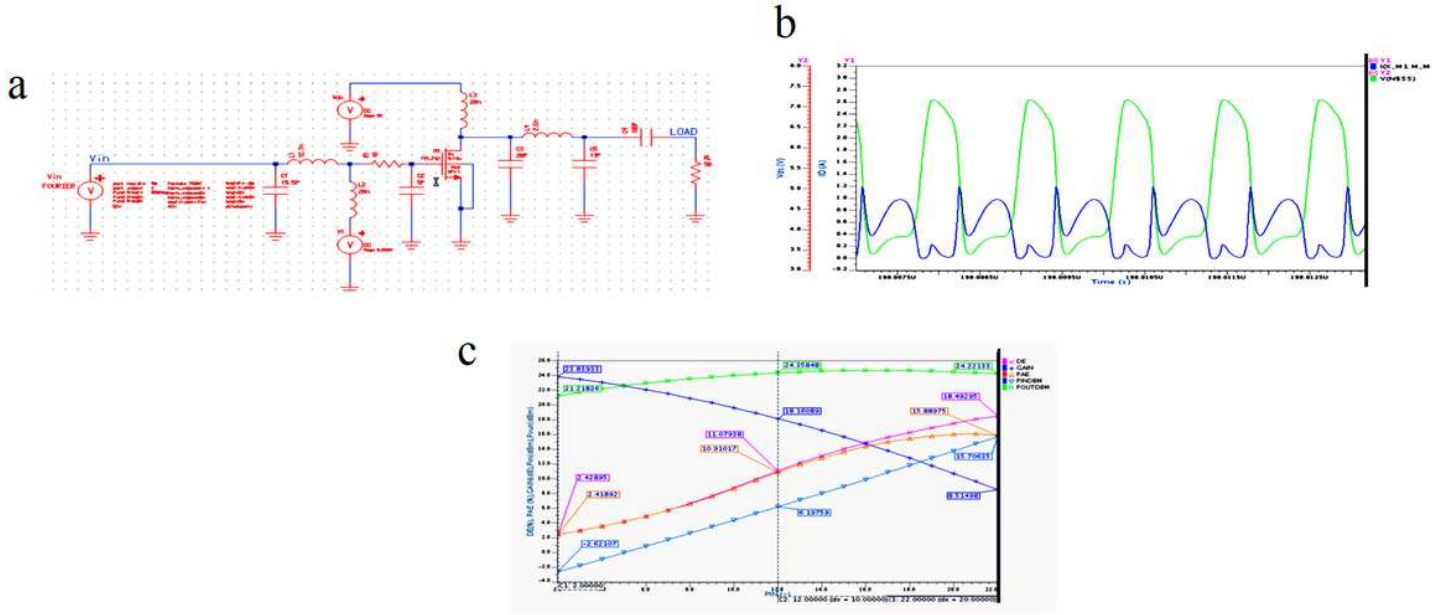



**Figure 8**

(a). Schematic circuit of the proposed class J power amplifier with Fourier input source at 850MHz. (b). Intrinsic voltage and current waveforms at the drain of proposed Class-J PA (VDS &ID) with Fourier input source at 850MHz (c). Measured gain, output power (Pout dBm), PAE, PE, as a function of input power (Pin=2dBm-22dBm) at 850MHz.

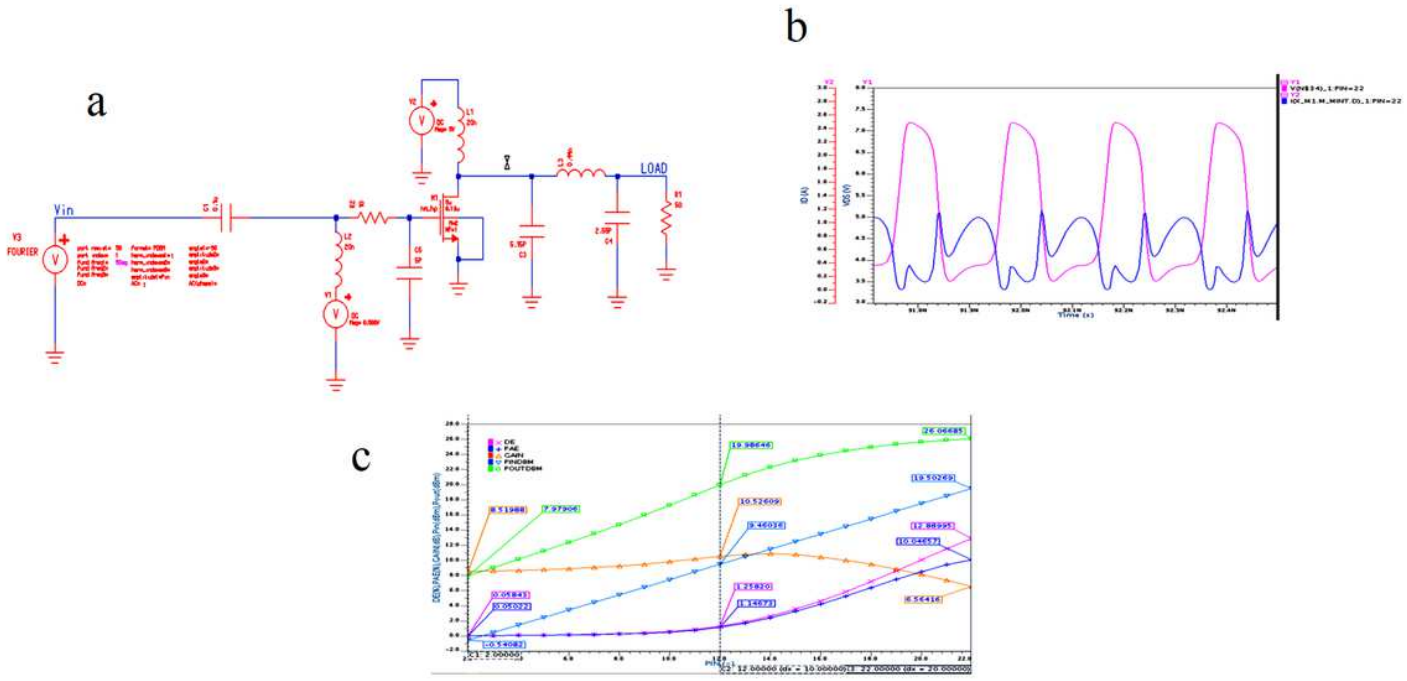



**Figure 9**

(a). Schematic circuit of the proposed Class-J PA with Fourier input source at 5GHz. (b). Intrinsic voltage and current waveforms at the drain of proposed Class-J PA (VDS &ID) with Fourier input source at 5GHz (c). Measured gain, output power (Pout dBm), PAE, PE, as a function of input power (Pin=2dBm-22dBm) at 5GHz

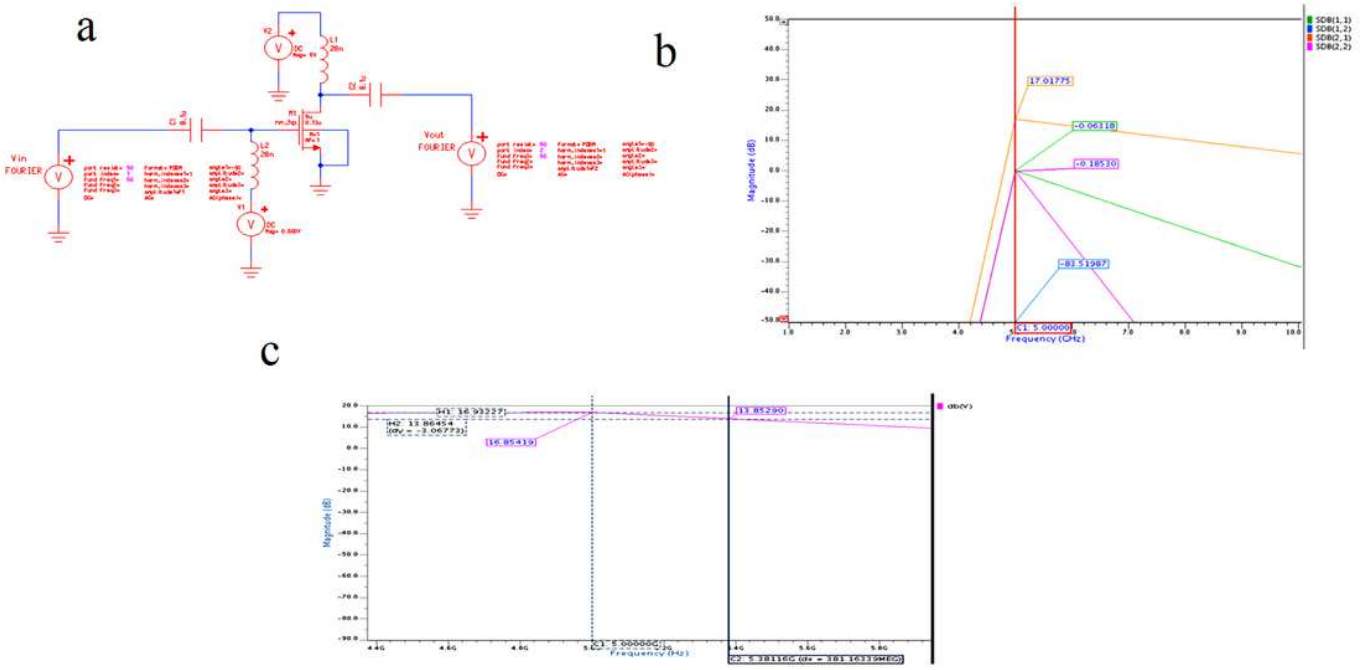



**Figure 10**

(a) S-Parameter and Zout extraction of nm_hp NMOS Transistor at 5GHz frequency (b) S parameters of nm_hp NMOS Transistor at 5GHz frequency (c) small-signal gain obtained from AC analysis of class J PA

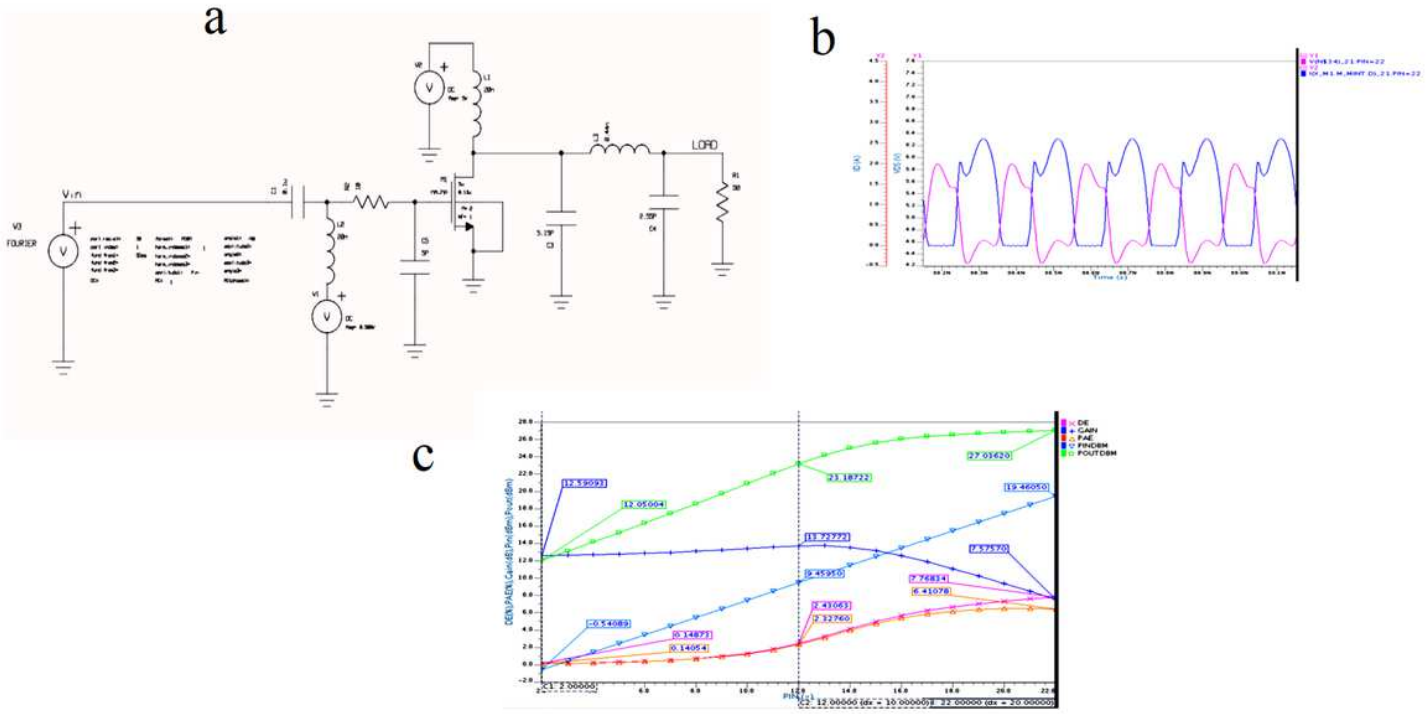



**Figure 11**

(a). Schematic circuit of the proposed Class-J PA with Fourier input source at 5GHz. (b). Intrinsic voltage and current waveforms at the drain of proposed Class-J PA (VDS &ID) with Fourier input source at 5GHz (c). Measured gain, output power (Pout dBm), PAE, PE, as a function of input power (Pin=2dBm-22dBm) at 5GHz