Highly Reliable Memory Operation of High Density Three-Terminal Thyristor Random Access Memory

Hyangwoo Kim
POSTECH: Pohang University of Science and Technology
Hyeonsu Cho (hscho21@postech.ac.kr)
POSTECH: Pohang University of Science and Technology https://orcid.org/0000-0002-8779-5816
Hyeon-Tak Kwak
POSTECH: Pohang University of Science and Technology
Myunghae Seo
POSTECH: Pohang University of Science and Technology
Seungho Lee
POSTECH: Pohang University of Science and Technology
Byoung Don Kong
POSTECH: Pohang University of Science and Technology
Chang-Ki Baek
POSTECH: Pohang University of Science and Technology

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Abstract

Three-terminal (3-T) thyristor random-access memory is explored for a next generation high-density nanoscale vertical cross-point array. The effects of standby voltages on the device are thoroughly investigated in terms of gate-cathode voltage ($V_{GC,ST}$) and anode- cathode voltage ($V_{AC,ST}$) in the standby state for superior data retention characteristics and low-power operation. The device with the optimized $V_{GC,ST}$ of -0.4 V and $V_{AC,ST}$ of 0.55 V shows the continuous data retention capability without refresh operation with a low standby current of 0.13 pA. In addition, a memory array operation scheme of 3-T TRAM is proposed to address array disturbance issues. The presented array operation scheme can efficiently minimize program, erase and read disturbances on the adjacent unselected cells by adjusting gate-cathode voltage. The standby voltage turns out to be beneficial to improve retention characteristics: over 10 s. With the proposed memory array operation, 3-T TRAM can provide excellent data retention characteristics and high-density memory configurations comparable with or surpass conventional dynamic random-access memory (DRAM) technology.

1. Introduction

The scaling down of dynamic random-access memory (DRAM) cell has been continuously required for high- density, high-speed, and low-power operations [1–3] However, the conventional *one transistor-one capacitor* (1T- 1C) DRAM are facing an inevitable problem: it is increasingly difficult to achieve the required capacitance to differentiate the two states (~ 10 fF/cell) with the smaller cell area [4]. Even though there have been many studies to improve the capacitor technologies, such as new high-*k* materials [5–7] and a high-aspect-ratio 3D capacitor structure [8, 9], these approaches possess the issue of increasing fabrication complexities and high cost [2–3]. To overcome these challenges, a capacitorless 1T DRAM structure, namely a *thyristor-based random-access memory* (TRAM), has been proposed as an alternative in which the charge is stored at the internal *p-base and n-base* storage area [10–16]. The TRAM can operate as a two-terminal (2-T) device by modulating the energy band with only the anode and cathode biases [10–12]. 2-T TRAM has the advantage of its simple structure that allows a cost-effective cross-point array fabrication with conventional Si processes. Yet, the drawbacks are the low data retention and array disturbance that stem from the weak controllability of the storage area [10–12]. On the other hand, a three-terminal (3-T) TRAM, whose gate bias controls the energy band of the storage region, can remedy these drawbacks; the proper adjustment of gate-cathode voltage (V_{GC}) can improve the retention characteristics and the array disturbance immunity by anode-cathode voltage (V_{AC}) [13–16]. In addition, if a vertical channel transistor (VCT) is adopted, $4F^2$ memory feature size can be achievable with the 3-T TRAM [17, 18].

This paper aims at providing guidelines on the operating voltage conditions for the 3-T TRAM in array configurations. The effects of the gate-cathode voltage on the standby state ($V_{GC,ST}$) are thoroughly investigated for low-power operations and better retention characteristics. To maintain the stored charges in the storage area with the lowest standby current, a minimum anode-cathode voltage on the standby

state ($V_{AC,ST}$) is obtained from the anode current-anode voltage characteristics (I_A-V_{AC}). Furthermore, for a reliable array operation, the operating conditions are suggested to avoid any possible array disturbance using the optimal standby voltage.

2. Simulation Details

Figure 1 shows a schematic diagram of a 3-T TRAM unit cell and a possible cross-point vertical array configuration. The 3-T TRAM consists of physical p^+-anode – n-base – p-base – n^+-cathode layers with a gated p-base. The anode and cathode areas are highly doped with a doping concentration of 1×10^{20} cm^{-3}, and the doping concentration of base areas (p- and n-base) is 1×10^{18} cm^{-3}. The lengths of both n- and p-bases are set to 100 nm considering the junctions' depletion widths [12]. The channel area is 20×20 nm^2, and the thickness of the gate oxide is 5 nm. The gate and cathode electrodes are designed as a word-line (WL) and a bit-line (BL), respectively.

Si-based 3-T TRAM cells are simulated using Sentaurus technology computer-aided design (TCAD) [19]. Usual Drift-Diffusion transport model with Fermi-Dirac distribution is used. Philips unified mobility model is adopted to consider the carrier-impurity and carrier-carrier scatterings [20], and the high-field saturation and doping-dependent mobility models are also used. Oldslotboom bandgap narrowing model [21] is used to consider the highly doped silicon regions. Doping-dependent Shockley-Read-Hall (SRH) [22] and Auger recombination [23] models are adopted to account for the carrier recombination at the junctions. In addition, the Si-SiO_2 surface recombination model is included to account for the leakage current at the interfaces. The avalanche generation [24] and band-to-band tunneling [25] models are also considered to calculate the carrier generations and the tunneling. The pulses applied to all memory operations have the rise time (T_{rise}) and the fall time (T_{fall}) of 0.25 ns, while the hold time (T_{hold}) is 2 ns [12]. The operation speed inferred from these pulse parameters is comparable to the modern DRAM memory clock rate [26].

3. Results And Discussion

A. Optimization of standby voltages

Figure 2(a) shows two possible approaches to program a cell. In both approaches, the cathode voltage (V_C) is defined as 0.0 V. However, the voltage differences between the gate and the cathode in the standby state ($V_{GC,ST}$) are set to two different values. -0.4 V (right) is the optimized value, while 0.0 V (left) is the conventional case for a comparison. The device with the $V_{GC,ST}$ of -0.4 V has a low program anode-cathode voltage ($V_{AC,P}$) of 1.2 V, and this is only a half of $V_{AC,P}$ required when $V_{GC,ST}$ is 0.0 V. This low $V_{AC,P}$ is attributed to the accumulated holes in p-base by the negative $V_{GC,ST}$. When the V_{GC} rapidly rises to 0.4 V for a program operation, the accumulated holes by the negative $V_{GC,ST}$ (-0.4 V) reduce the energy band barrier height in the p-base (H_P). As such, the device with the optimized $V_{GC,ST}$ minimizes the power consumption in program operation since a smaller $V_{AC,P}$ is required to reduce the H_P. Figure 2(b) shows the stored hole density in the p-base (N_P) as a function of standby time at state-1 ($T_{ST,1}$) after the

program pulse. As the $T_{ST,1}$ increases, the N_P decreases due to the carrier recombination at the junctions. Due to the low $V_{AC,P}$, the device with $V_{GC,ST}$ of -0.4 V exhibits lower N_P than the case of 0.0 V in the early stage ($T_{ST,1}$ < 1 μs). However, the N_P in the later stage ($T_{ST,1}$ > 1 μs) is higher than the case of 0.0 V. This higher N_P is the result of the low recombination rate caused by the depletion of electrons in the *p*-base due to the negative $V_{GC,ST}$. Figure 2(c) shows the energy band diagrams of 3-T TRAM at 1 ms after a program pulse to investigate the data retention characteristic depending on $V_{GC,ST}$. The left side is for $V_{GC,ST}$ = 0.0 V, and the right side is for $V_{GC,ST}$ = -0.4 V. The H_P difference between the state-0 and state-1 at 1 ms after a program pulse exhibits a high value of 0.25 eV with the optimized $V_{GC,ST}$ of -0.4 V due to the long-lasting N_P. This indicates that the device with an optimized $V_{GC,ST}$ has an improved data retention characteristics that can maintain the low-resistance state (state-1) for a longer time.

Figure 3(a) shows I_A-V_{AC} characteristics for the V_{AC} pulse with T_{rise} of 1000 s, T_{hold} of 2 ns, and T_{fall} of 1000 s when V_{GC} is fixed at -0.4 V. It has been previously reported that the I_A-V_{AC} curve with long T_{fall} of 1000 s can effectively provide the minimum $V_{AC,ST}$ to improve the data retention characteristics [12]. When V_{GC} is fixed to -0.4 V, the device exhibits a rapid increase of I_A at V_{AC} = 2.2 V representing a switching from the state-0 to the state-1. This indicates that a higher V_{AC} is required to switch the state as long as V_{GC} is maintained below − 0.4 V, and thus the state is well protected. As mentioned above, for a normal programing, only 1.2 V of $V_{AC,P}$ is required since V_{GC} is increased from − 0.4 V to 0.4 V. As such, for $V_{AC,P}$ less than 2.2 V applied to the bit-line (BL) in array operation, 3-T TRAM can avoid unwanted program errors if the voltage of the word-line (WL) is fixed to $V_{GC,ST}$ = -0.4 V or below.

In the downward V_{AC} sweep (T_{fall}), the switching of the state occurs at 0.55 V as evidenced by the sharp slope (red dashed line in Fig. 3(a)). Thus, the state-1 can be maintained at $V_{AC,ST}$ of 0.55 V. To investigate this drastic change by the voltage difference as small as 0.01 V, N_P as a function of $T_{ST,1}$ is examined for two different $V_{AC,ST}$ of 0.54 V and 0.55 V. For $V_{AC,ST}$ = 0.54 V, the stored holes disappear rapidly after 1 ms, but for $V_{AC,ST}$ = 0.55 V, the device can maintain a high N_P of about 1.66×10^{18} cm^{-3} for more than 10 s which is 10^4 times larger. Figure 3(c) shows the energy band diagrams of 3-T TRAM at $T_{ST,1}$ =10 s for two different $V_{AC,ST}$ of 0.54 V and 0.55 V. With $V_{AC,ST}$ of 0.55 V, holes more than the amount recombine are injected into the base region, and the state-1 band shape along with the stored charge are maintained. With $V_{AC,ST}$ of 0.54 V, on the other hand, the holes injection is not enough to compensate the loss of holes by recombination, and the stored charge rapidly disappears, returning the band shape back to that of the state-0. A device with $V_{AC,ST}$ lower than 0.54 V will face similar level or faster charge loss. Considering the clock speed of modern VLSI circuit, the 3-T TRAM with $V_{AC.ST}$ of 0.55 V can exhibit the continuous state-1 virtually without a refresh operation. In addition, despite the high $V_{AC,ST}$ of 0.55 V, the device has a standby current as low as 0.13 pA, suggesting that the 3-T TRAM with the $V_{AC,ST}$ of 0.55 V is suitable for a low-power operation.

B. Memory Operation of 3-T TRAM array

Compared to the 2-T TRAM without the gate terminal, the 3-T TRAM has a strong state immunity against the change of anode-cathode potential due to the gate terminal. On the other hand, the shift in gate-cathode potential in the 3-T TRAM easily interferes with the stored information. This disturbance is studied by assuming an operation pulse applied to a nearby cell. The cell under the study is initially at unselected bias condition, and the subject cell's states after the disturbance are observed. Figure 4 shows the schematic of a memory-cell-array configuration of 3-T TRAM. Our study shows that, with a proper operating scheme (maintaining fixed V_{GC} to the unselected cells), this memory-cell-array configuration can prevent unselected cells' unwanted changes. For an efficient adjustment of V_{GC} in the memory operation, the gate and cathode electrodes are set to the WL and BL, respectively. The anode electrode is fixed at 0.55 V. Table. 1 shows the operating voltage conditions for the 3-T TRAM array. To maintain the stable state-0 and state-1 in the standby state, V_G and V_C in the standby state are set to -0.4 V and 0.0 V with the V_A of 0.55 V. The operation strategies to prevent the array disturbance, found through our study, are summarized for each operation (Program, Erase, and Parallel Read) as the followings.

Program

To program the selected cell, the selected V_C decreases from 0.0 V to -0.8 V as shown in the Table 1. This decreased V_C can facilitate the influx of carriers into the base region. As such, the selected cell is programmed with the V_{GC} of 0.4 V and V_{AC} of 1.35 V. Figure 5(a) shows the simulated energy band diagrams of the cell under programming at $T_{ST,0}$ and $T_{ST,1}$ = 10 s. The selected cell for the program operation can maintain the state-1 with low H_P even at the high $T_{ST,1}$ of 10 s. However, the problem with the above approach is that all cells in the selected BL experience unwanted program operation by the V_{GC} of 0.4 V and V_{AC} of 1.35 V, which are larger than the V_{GC} of 0.4 V and $V_{AC,P}$ of 1.2 V, respectively. To prevent this unwanted programming, V_G in all WLs except for the selected WL can be decreased from − 0.4 V to -1.2 V. In this way, the V_{GC} can be recovered back to -0.4 V from 0.4 V. Figure 5(b) shows the simulated energy band diagrams of the unselected cells at $T_{ST,0}$ and $T_{ST,1}$ = 0 s. The unselected cells exhibit no change in energy band with the V_{AC} of 1.35 V if V_{GC} is below − 0.4 V. Thus, the selected cell exhibits the continuous state-1, while the unselected cells can avoid the unwanted program disturbance.

Erase

To erase a selected cell, the V_G of the selected WL should be increased from − 0.4 V to 0.4 V as shown in the Table 1. In Fig. 6(a), the N_P is investigated as a function of $T_{ST,0}$ after the erase operation at $T_{ST,1}$ of 2.5 ns. When $T_{ST,0}$ is 1 ns, N_P is 1.02×10^{17} cm^{-3}, which is about 20 times less than 2.02×10^{18} cm^{-3} at $T_{ST,1}$ of 2.5 ns. This reduced N_P is due to the depletion of stored holes in the *p*-base as the V_G increases. As the $T_{ST,0}$ becomes 1 ms, the N_P increases to 4.22×10^{17} cm^{-3}, and then if $T_{ST,0}$ gets longer, the N_P decreases to 0 cm^{-3}, which represents the complete state-0. To investigate the reason, the energy band diagram at $T_{ST,0}$ of 1 ns is examined and compares with the energy band at $T_{ST,1}$ of 2.5 ns (Fig. 6(b)). After the erase operation, the *n*-base (H_N) energy band height decreases as the H_P increases. The holes in

the anode flow into the *p*-base over the lowered H_N, and the N_P increases at $T_{ST,0}$ < 1 ms. On the other hand, at $T_{ST,0}$ > 1 ms, the number of injected holes decreases due to the increased H_N by the recombination process, so the N_P is reduced as $T_{ST,0}$ increases. The highest N_P of 4.22×10^{17} cm^{-3} is low enough compared to the value representing the state-1 so that the unwanted program error can be avoided. From this result, it is found that the cell selected for the erase operation can exhibit the state-0 with the sufficiently high H_P at any $T_{ST,0}$. However, the erasing method with only the increased V_G of the selected WL can cause a problem of erasing all cells on the same WL. To avoid this issue, the V_{GC} should be reduced from 0.4 V to -0.4 V by increasing V_C from 0.0 V to 0.8 V on all BLs except for the selected BL (Table 1). Accordingly, the erase disturbance pulse with V_{AC} = -0.25 V and V_{GC} = -0.4 V applies to the unselected cells on the same WL. The state-1 should be detectable at any time even if this erase disturbance pulse is repeated after the N_P is saturated to the lowest value of 1.66×10^{18} cm^{-3}. To confirm this, as shown in Fig. 6(c), the N_P is examined as a function of the number of this erase disturbance pulse. Despite the repeated disturbance pulses, N_P exhibits a negligible decrease near 1.5×10^{18} cm^{-3} so that the device can maintain the state-1. In addition, the slightly reduced N_P can readily return to its original state-1 by applying read operation. Therefore, the 3-T TRAM can overcome the erase disturbance by controlling the V_{GC} in unselected cells.

Parallel Read

To perform the parallel read operations on the cells that share the same BL, the V_C of the selected BL and the V_G of all WLs are set to -0.8 V (Table 1). If the V_C in the selected BL is decreased to -0.8 V, not only V_{AC} increases to 1.35 V but also V_{GC} increases to 0.4 V. This high V_{GC} lowers the H_P and causes unwanted program errors of the cells in the selected BL. To avoid this, the V_G in all WLs should be decreased to -0.8 V so that 0.0 V of V_{GC} and 1.35 V of V_{AC} are applied to the cells in the selected BL. To investigate the effect of the read operation on the state-0, the operating voltage and anode current are extracted after ten consecutive read operations are applied following an erase operation as shown in Fig. 7(a). Although the ten continuous read pulses are applied to the device after the erase operation, the read current gradually decreases, confirming that the state-0 stably is maintained. This result indicates that the 3-T TRAM with the suggested array configuration for reading exhibits a reliable disturbance immunity for the state-0. Additionally, to confirm the detectability of the state-1, the operating voltage and anode current for a program and a read with the $T_{ST,1}$ of 10 s are extracted (Fig. 7(b)). The read pulse can detect the state-1 continuously with a high current even at a long $T_{ST,1}$ of 10 s.

4. Conclusion

We have investigated the effects of the $V_{GC,ST}$ and $V_{AC,ST}$ of the nanoscaled 3-T TRAM for low-power operation and better retention characteristics. The optimized $V_{GC,ST}$ of -0.4 V allows a lower $V_{AC,P}$ due to the accumulated holes in the standby state. In addition, a low H_P remains for a longer time because the optimized $V_{GC,ST}$ effectively maintains the high N_P by reducing carrier recombinations at the junctions.

The investigation of I_A-V_{AC} characteristics suggests that a minimum $V_{AC,ST}$ of 0.55 V enables the device to exhibit the continuous state-1 without refresh operation while allowing a small standby current of 0.13 pA. Furthermore, a memory array operation strategy of 3-T TRAM is presented for the first time to implement reliable array operations without disturbances. The adjustment of V_{GC} can effectively minimize the program, erase and read disturbances in unselected cells. Along with the high immunity against array disturbances, the 3-T TRAM with the optimum strategy for array operations exhibits superior data retention capability than conventional 1T-1C DRAM technology. Thus, the proposed memory array operation scheme can provide a way to realize capacitorless 1T DRAM with 3-T TRAM.

Declarations

Acknowledgments

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Tables

Table. 1. Operating voltage condition of 3-T TRAM array

Operation Mode	V_A, (V)	Word-line (WL), V_G (V)		Bit-line (BL), V_C (V)	
		Selected	Un-sel	Selected	Un-sel
Standby	0.55	-0.4		0.0	
Program		-0.4	-1.2	-0.8	0.0
Erase		0.4	-0.4	0.0	0.8
Read		-0.8	-0.8	0.0	

Figures

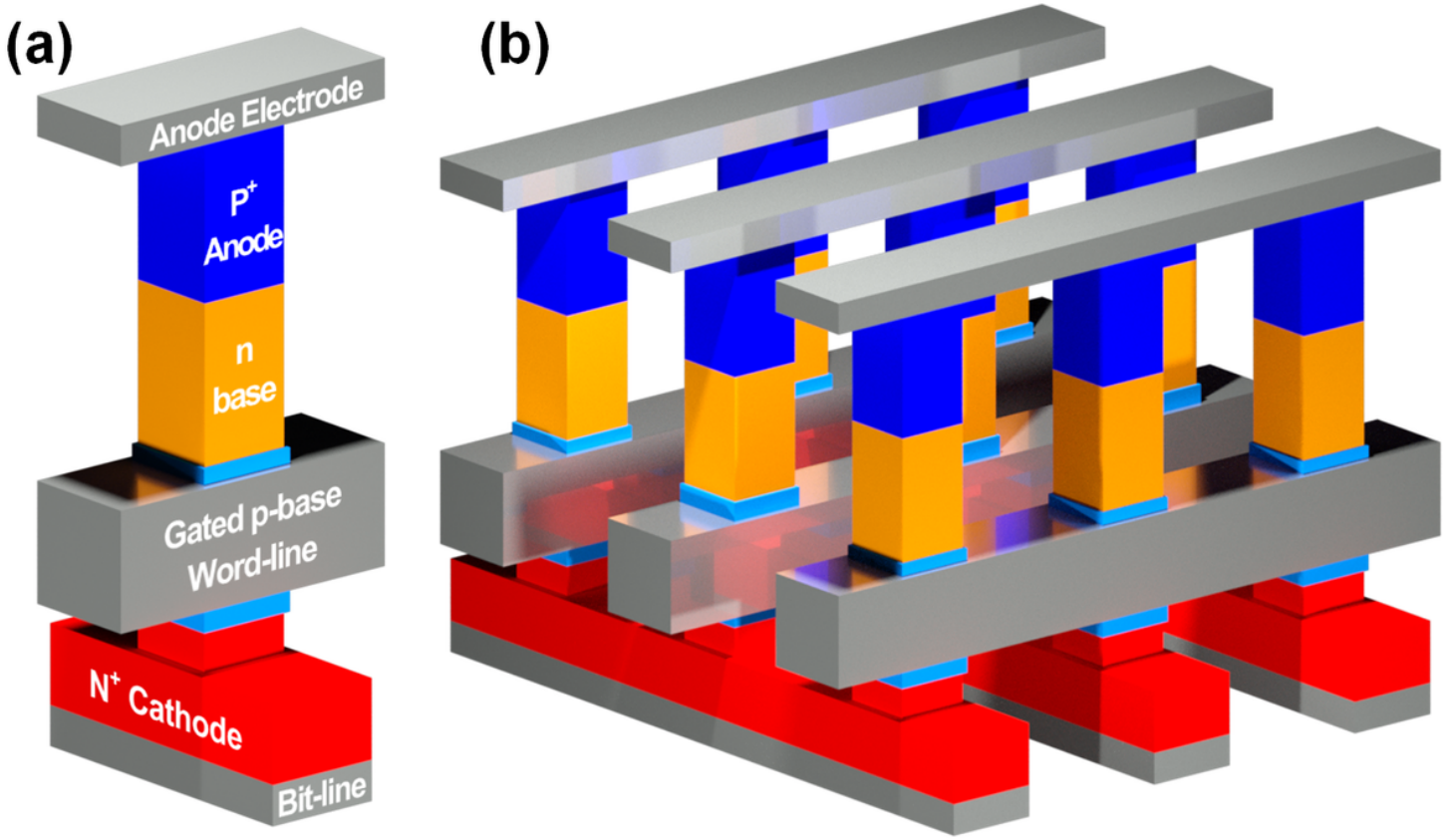

Figure 1

Schematic diagrams of (a) 3-T TRAM unit cell and (b) cross-point vertical 3-T TRAM array.

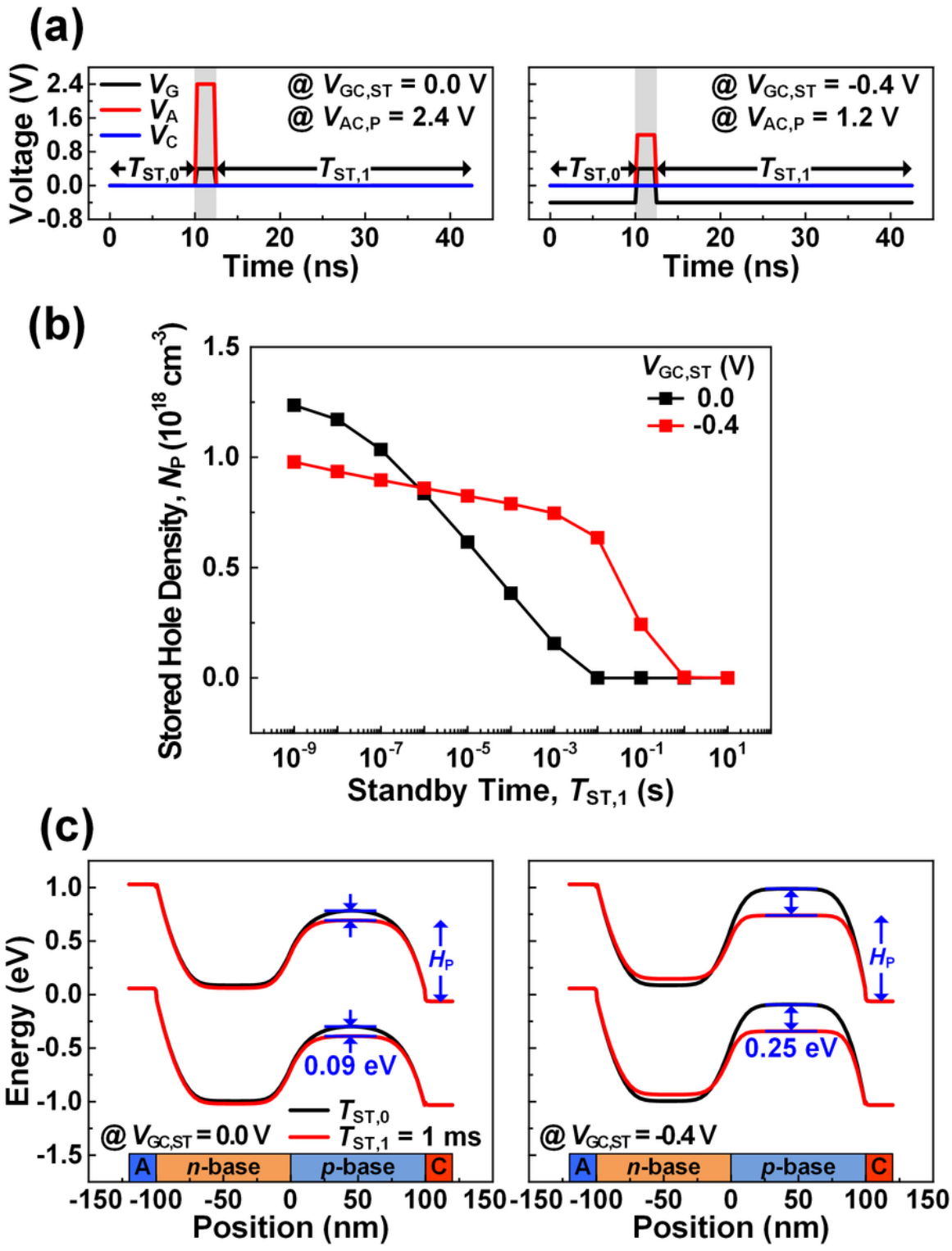

Figure 2

(a) Program operation conditions at a VC of 0 V when a VGC,ST is 0.0 V (left) and -0.4 V (right). (b) NP as a function of TST,1 at different VGC,ST of 0.0 V (black line) and -0.4 V (red line). (c) Energy band diagrams at 1 ms of TST,1 when VGC,ST is 0.0 V (left) and -0.4 V (right).

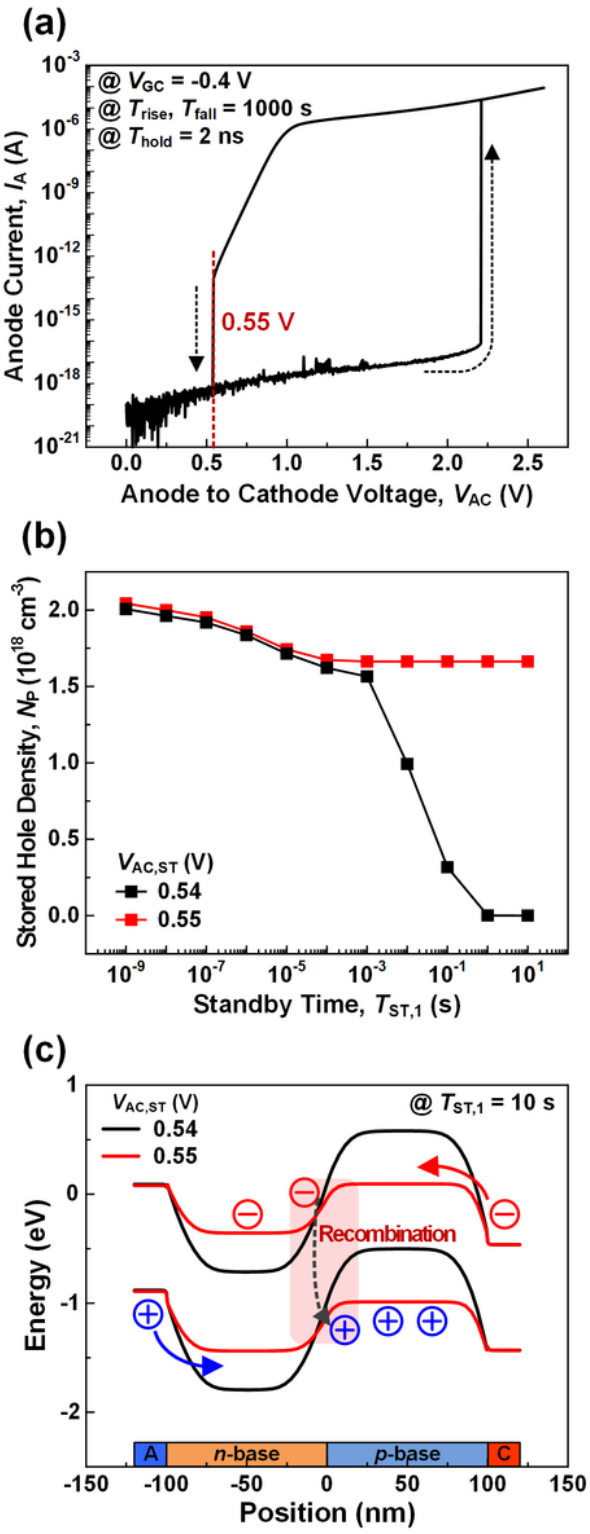

Figure 3

(a) IA-VAC characteristics of the 3-T TRAM by the VAC pulse with Trise, Tfall = 1000 s, Thold = 2 ns when the VGC is fixed at -0.4 V. (b) NP as a function of TST,1 at different VAC,ST of 0.54 V (black line) and 0.55 V red line). (c) Energy band diagrams at TST,1 = 10 s with different VAC,ST of 0.54 V and 0.55 V.

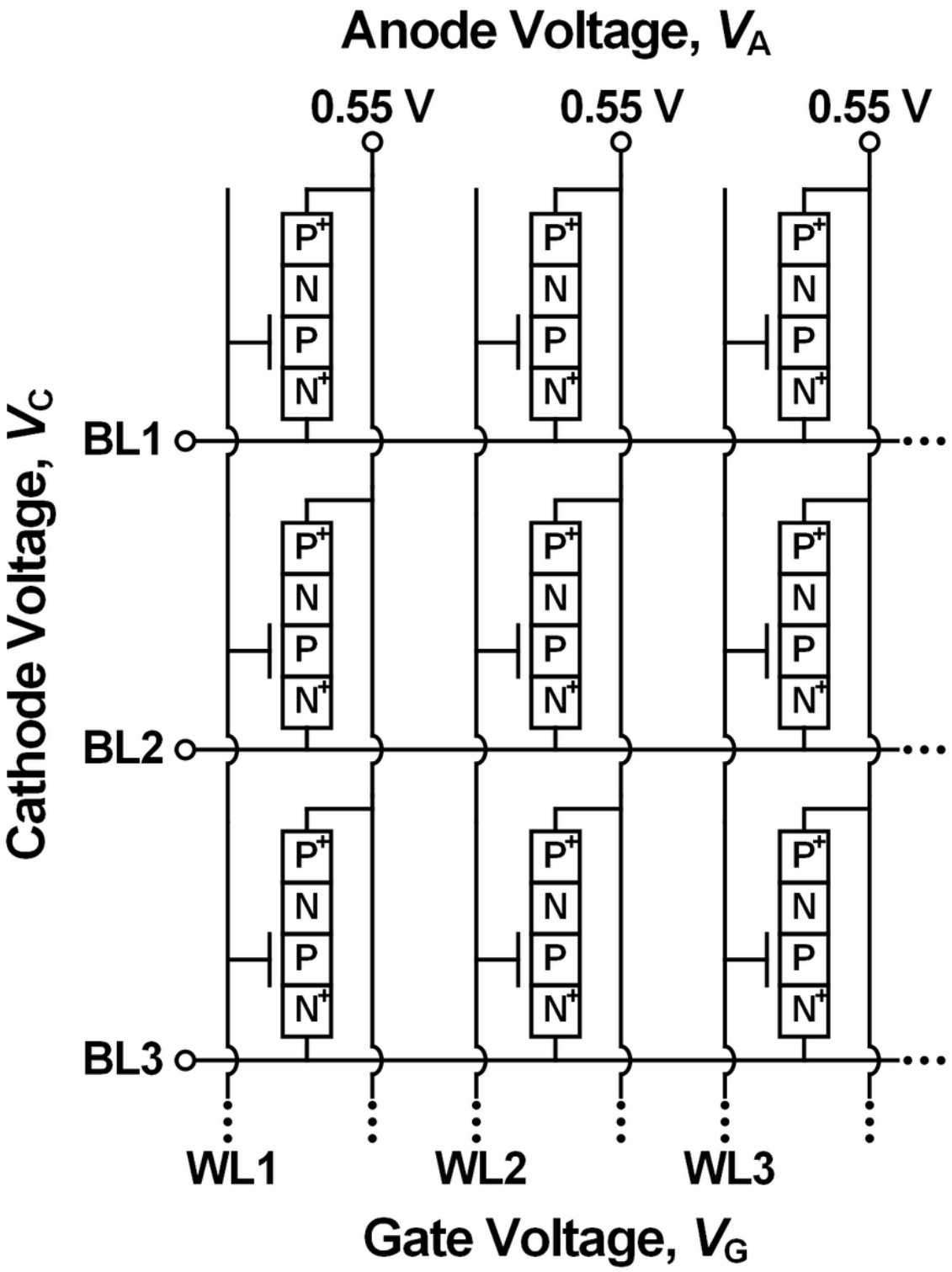

Figure 4

Schematic diagram of the 3-T TRAM memory-cell-array configuration.

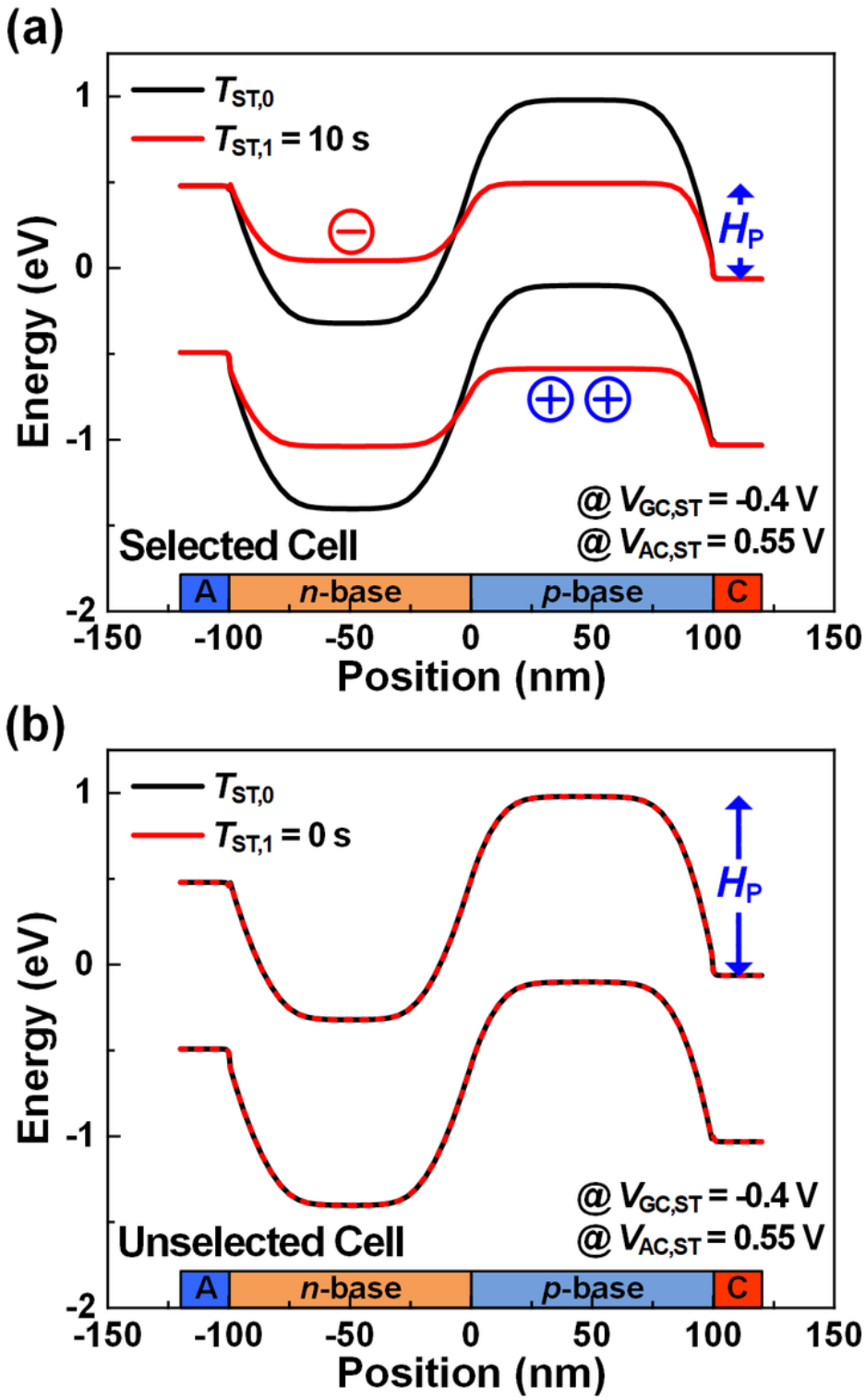

Figure 5

Energy band diagrams of (a) the selected cell for programming at TST,0 (black line) and TST,1 = 10 s (red line) and that of the unselected cells at TST,0 (black line) and TST,1 = 0 s (red line).

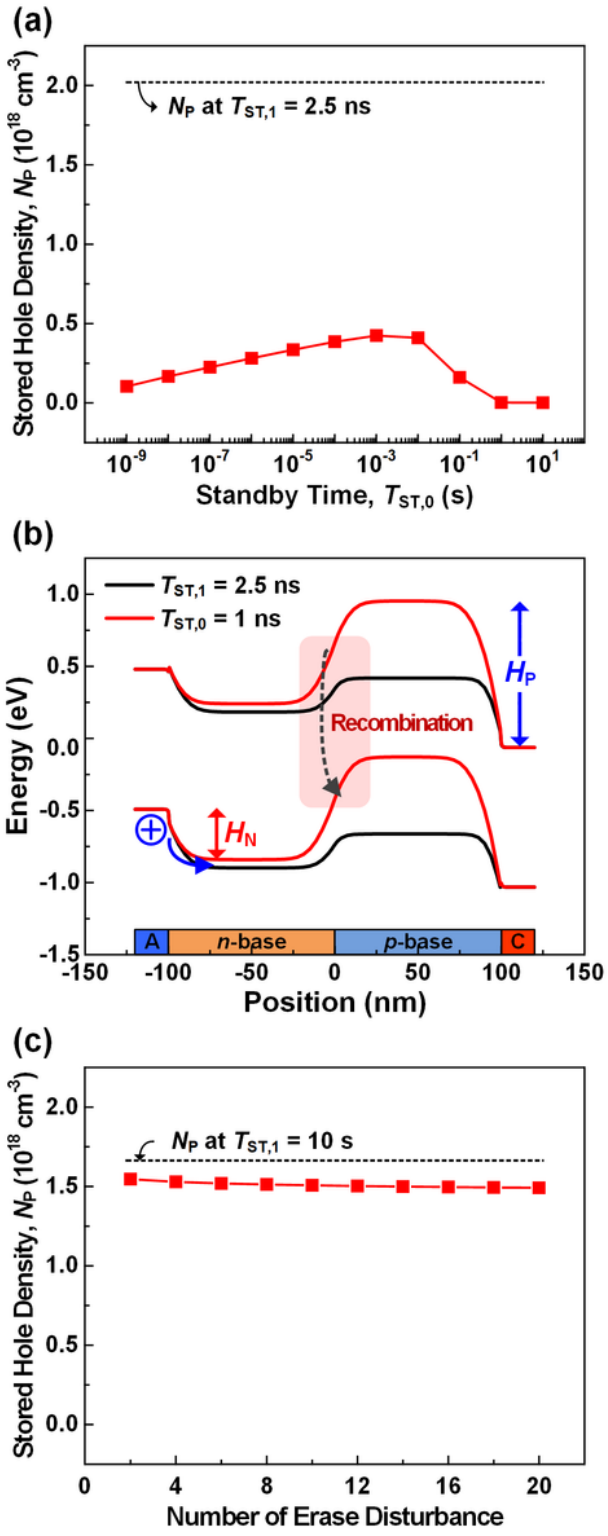

Figure 6

(a) NP as a function of TST,0 after the erase at TST,1 = 2.5 ns. (b) Energy band diagrams at TST,1 = 2.5 ns and TST,0 = 1 ns. (c) NP as a function of the number of the erase disturbance pulse.

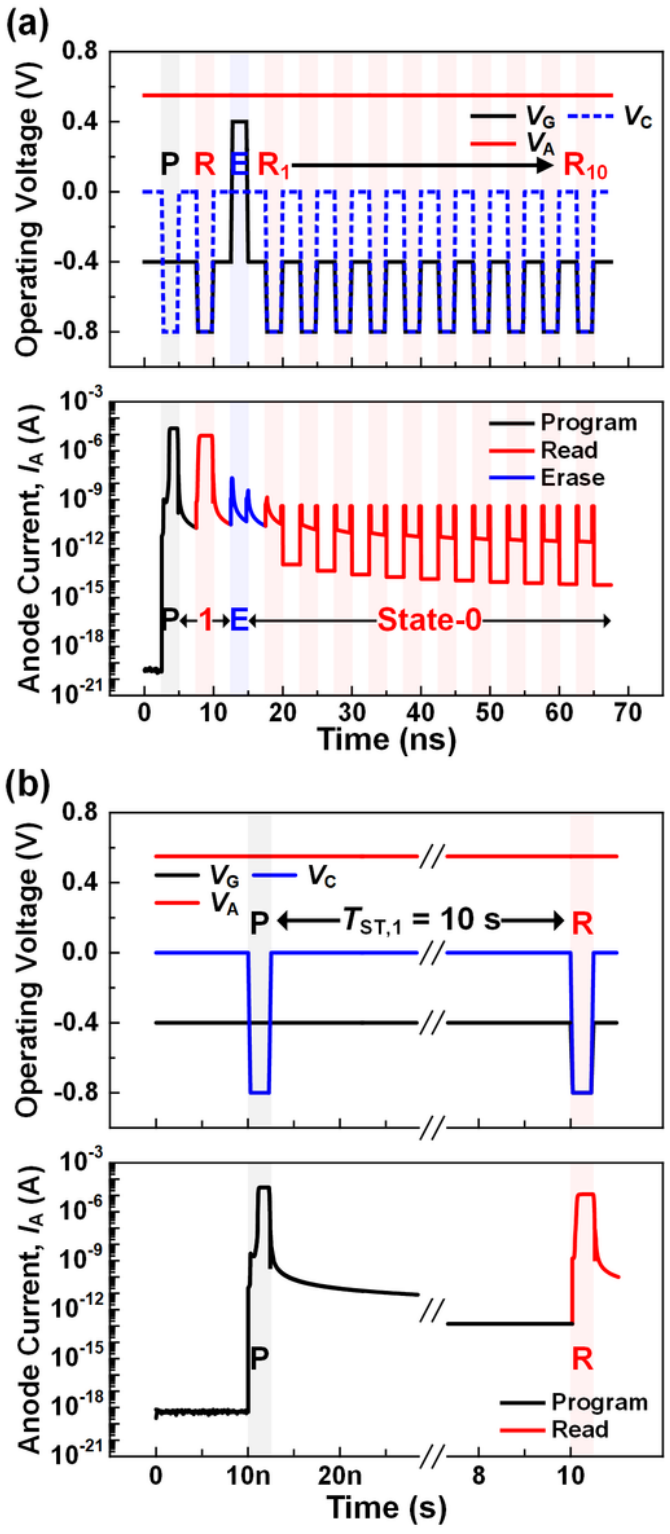

Figure 7

Operating voltage and anode current (a) when ten consecutive read operations are applied after the erase operation and (b) when a read operation is applied at TST,1 = 10 s.