Effect of positive and negative interface trap charges on the performance of M-FinFET and its RF/linearity analysis

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Research Article

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Abstract

Multiple Fins structured FinFET (M-FinFET) is a promising semiconductor device for future improvisation of CMOS technology. In this paper, we investigate the impact of interface trap charges (positive and negative trap) at the HfO2/Si interface in M-FinFET for the first time. The various important DC attributes, RF/analog, and linearity metrics are studied in presence and absence of traps. Simultaneously, the various trap concentration effect on the characteristics of M-FinFET are also observed. The results show that the introduction of interface trap charges (ITC) has optimized the ON current, OFF current, and also improves sub-threshold swing (SS) characteristics as compared to no trap condition. It is observed that positive trap having trap concentration of $10^{12}/cm^2$ enhances the I_{ON} ~5.14x, SS by 44.75%, and various important RF/analog parameter such as transconductance (G_m) improves by a factor 5, device efficiency by 7.4% and intrinsic gain (A_v) 80.4%. On the other hand, linearity parameters like VIP2, VIP3 and 1 dB compression point show better performance in presence of positive and negative trap.

Introduction:

Advancement of technology means scaling of device attributes in nanometer range [1-2], replacement of conventional materials like integration of HfO_2 material instead of SiO_2 [3], and various modification techniques such as gate material engineering, gate oxide engineering, work function engineering, and space engineering, etc.[4-5]. The outcomes are reduction of supply voltage, low leakage current whereas various transistors can be integrated into a single chip that reduces the power consumption with better performance [6-7]. Various MOS[8] initiative structures such as double-gate MOSFET, dual material gate (DMG) MOSFET, surrounding gate (SG) MOSFET, etc. have been proposed by Gordon Moore to increase the efficiency [9-11]. Aggressive downscaling of device parameters limits the performance of these all planar MOS structures [12] to meet the requirements of the International Technology Roadmap for Semiconductor Projection (ITRS) [13] and device faced a serious unwanted problem called short channel effects (SCEs). Drain-induced barrier lowering (DIBL), sub-threshold swing (SS), threshold voltage variation, and mobility degradation are the various SCEs [14-15].

To minimize these SCEs issues, the researcher developed various ultra-modern structures which operated in high frequency. Fin Field-effect transistor (FinFET) [16-18], 3D dimensional, is one of the mainstream candidates in the semiconductor industry over planar conventional devices [19-20] in the 22nm to sub 10nm regimes which have superior gate controllability on channel [21-22], high transconductance, less leakage current, ideal sub-threshold swing, and high switching speed [23-24]. The number of Fin increases the drive capability as the total channel width also increased. Nowadays researcher has shown their interest to build up a multiple Fin based FinFET structure [25-26] whereas multiple parallel Fins between source and drain are placed. Multi-Fin FET (M-FinFET) structure is very useful for RF application in high frequency and well suppressed in SCEs issues. K. Tachi et al. in [27] have investigated multi-channel Field-Effect Transistors (Mc-FETs) architecture to reduce the source-drain

resistance by combining Ion implantation and in-situ doped SEG (Selective Epitaxial Growth) which increases the current gain. On the other hand, Emilie Bernard et al. in [28] have proposed the multi-channel Field-Effect Transistor (Mc-FET) and investigated the performances of electrical parameters such as I_{ON} and I_{OFF}. They showed that Mc-FET contributes ultra-low I_{OFF} and high I_{ON} which are satisfying low standby power (LSTP) and high performance (HP) applications. Wen-Kuan Yeh et al. [29] investigates the effect of carrier quantization on multi-fin high K/Metal tri-gate n-type and p-type FinFET where several Fins exhibited superior device performance. Nevertheless, the above research towards M-FinFET is mainly focused on device characteristics without focus on the effects of interface trap charges.

It has been also reported that the presence of interface trap charges at the oxide-channel interface impacts device reliability [30]. Variation in process, stress, radiation, and hot carriers effect is the reason behind the introduction of interface traps at the oxide-channel interface [31]. It is reported device is more immune to interface trap effects and improves the electrical characteristics of the device. [32] Investigates the impact of interface trap at Si-SiO_2 interface in negative capacitance FinFET structure and found that the smaller variation of the threshold voltage is observed in presence of interface trap. Paper [33] investigates the impact of negative capacitance on Ge FinFET in presence of positive and negative trap charges (PTC and NTC). They revealed that PTC improves the device reliability and introducing of Ferroelectric layer with NTC enhances the output performance. Paper [34] demonstrates the influence of interface trap charges on GaAs/Al_2O_3 JL FinFET and found that proposed device gives better immune to interface trap charges and improves $I_{ON/OFF}$. . However, a very few studies have been reported to analysis the impact of interface trap charges on FinFET device in details. Specially, there is no literature of interface trap effect on M-FinFET device which motivates us to implement the same.

In this work, the impact of interface traps at the Si-HfO_2 interface on the performance of the M-FinFET structure has been newly investigated. Various interface traps such as positive trap and negative trap with various trap concentrations have been introduced and their influences are studied to analyze the RF/analog performance. The research paper has been arranged in the following sections. Section 2 describes the proposed structure with dimensions and various activated models are mentioned for the simulation study. Section 3 discusses the simulation results. Finally, concluding observation is given in section 4.

Design And Simulation:

The 3D and 2D views of Multi-Fin based FinFET (M-FinFET) structure are shown in fig. **1**a & **b**. 3 numbers Fin are placed in between source and drain region where all Fin is in equal dimensions. Silicon used as Fin material and HfO_2 used as gate dielectric material is wrapped over three Fin. Titanium (φ_m=4.4eV) to be considered as gate material and SiO_2 as an oxide material. The channel region is lightly doped to minimize the adverse effect like mobility degradation and tunneling issue and the doping concentration value is 10^{17} cm^{-3}. And the source/drain region is uniformly doped and the doping concentration value is

10^{22} cm^{-3}. The length of the source and drain region is 20 nm. The thickness and height of SiO_2 buried oxide are taken 14nm and 15nm. Gate length value of M-FinFET is considered 10nm whereas Fin width= 2nm and Fin height= 8nm are considered to simulate the structure. The simulation of the M-FinFET structure is done by TCAD sentaurus software [35].

In this paper, we proposed an M-FinFET structure and study the effect of different interface traps such as positive trap and negative trap and uncover the performance regarding linearity and RF/analog applications. Various models are activated to simulate the M-FinFET structure. Phonon scattering and Coulomb scattering models are considered to account for the effect of mobility degradation due to high doping concentration in semiconductor devices. SRH model is turned on in a simulator for the recombination and generation process. Band narrowing effect leads to activation of Old Slotboom model. To checking velocity saturation and mobility of charge carrier purposes, the velocity saturation model and mobility Masetti model are activated. For carrier transportation, the drift-diffusion model is taken.

Result And Discussion:

This section studied the impact of different interface trap charges such as positive and negative trap at Si-HfO_2 interface in M-FinFET structure. The various trap concentration (TC) value are $10^{12}/cm^2$, $3x10^{12}/cm^2$, $7x10^{12}/cm^2$, and $10x10^{12}/cm^2$. Drain to the gate voltage of 0.5V is considered for the whole simulation study. The drain current with RF/analog and linearity parameters performance of M-FinFET structure has been shown in the presence and absence of traps. Section 3.1 discusses the input/output characteristics of M-FinFET in presence of an interface trap. Section 3.2 portrays the analog performance of the M-FinFET structure where 3.3 observe the RF performance of the M-FinFET structure. Section 3.4 demonstrates the linearity performance.

Input/output Characteristics Of M-FinFET:

The comparison of drain current between conventional FinFET (C-FinFET) and multi-Fin structure M-FinFET is portrayed in Fig.**2** where all the dimensions remain same except Fin part. It is observed that proposed structure exhibits better I_{ON} than conventional FinFET. The SS value is also minimum (=87mV/dec) for proposed device whereas C-FinFET has SS value of 92mV/dec. A comparative analysis of proposed device with other recent existing structures has shown in table **1.** It is clearly noticed that proposed structure M-FinFET contributes better I_{ON} than other existing structures. For all these advantages, the impact of interface trap charges has done on the proposed structure.

Fig. **3a** demonstrates the comparison of drain current characteristics of M-FinFET in the presence and absence of trap where the positive and negative trap having trap concentration value of $10^{12}/cm^2$. It is observed that the device is more efficient with interface trap charges. The band gap energy is enlarged due to introduction of positive and negative trap charges as results ON current has improved as

compared to no trap condition. It is all about 5.14 times improvement of I_{ON} than no trap condition. Two insets are added to clear visualization of output variation.

The various DC parameters such as V_{th}, SS, I_{ON}, and switching ratio are tabulated in table **1**. It is reported that sub-threshold swing improves in presence of interface traps whereas a slight enhancement of SS can be seen without trap condition that degrades the device performance. On the other hand, the variation of the threshold voltage is less in absence of a trap.

The output characteristics I_D-V_{ds} of the M-FinFET device has presented in Fig. **3b** and comparative analysis are shown for with and without traps condition. It is noticed that there is a substantial increment of drain current in presence of traps as compared to without trap condition. A maximum ON current of 9.14mA has been achieved under the influence of a negative trap.

The input characteristics I_D-V_{gs} of M-FinFET device has been demonstrated for various trap concentration (TC) of negative trap in Fig. **4a**. It can be perceived that there is a negligible impact of trap concentration on drain current from low gate bias to high drain bias. Two insets are added to visualize the variation of drive current for negative traps having different trap concentrations.

The impact of positive trap for different trap concentrations, when the gate bias is varying within their range (0V to 1.5V), on drain current characteristics is shown in Fig. **4b.** It is examined that there is a significant increment in drain current and decrement of threshold voltage as positive trap concentration value decreases. An enhancement of ON current is observed for the positive trap of $10^{12}/cm^2$ trap concentration. The two important DC attributes like Vth and SS are shown in Fig. **4c** and **4d** for positive and negative traps having different trap concentrations. TCAD simulator shows that by keeping trap concentration of positive trap charges low, V_{th} and SS value can be improved whereas negative trap with various TC has an insignificant variation of Vth (~0.26V) and SS (~82mV/dec).

Study of Analog performance:

Various analog parameters performance like transconductance (G_m), drain conductance (G_d), device efficiency, intrinsic gin (A_v), and early voltage (V_{EA}) [39] have been demonstrated in Fig. **5** for trap/without trap circumstance to evaluating the overall analog performance of M-FinFET.

Transconductance measures the amount of gate controllability on the drain current and it's related to the gain of the transistors. It is found that G_m performance varies with gate voltage and peak value of G_m has been observed at low gate bias for the presence of traps (positive and negative trap) shown in Fig. **5a** and G_m falls at high gate voltage due to mobility degradation. The variation of G_d as a function of gate voltage with or without interface trap condition is shown in Fig. **5b**. From Fig. **5b** it is seen that drain conductance is fully suppressed without trap conditions due to increment of output resistance that improved the analog performance with better driving capability.

Device efficiency is an important attribute that can be recognized by the ratio of transconductance to drain current of any circuit. Fig. **5c** aiming to compare the device efficiency performances with gate voltage variation for M-FinFET structure in the presence and absence of trap. Interestingly, an insignificant variation of device efficiency has been observed for the trap/without trap condition. Device efficiency value is highest at very low gate bias for all variation and in the strong inversion region, device efficiency value is very low that indicating the power dissipation of any device.

Intrinsic gain (A_v) and early voltage performance have been shown in Fig. **5d** and **5e**. The ratio of transconductance (G_m) to output conductance (G_d) is called intrinsic gain (A_v). To obtain higher A_v, the G_d value should be less in analog circuit design. The intrinsic gain value increases under the influence of positive trap charges shown in Fig. **5d**. On the other hand, the opposite scenario can be seen in the early voltage performance of the M-FinFET device. Without trap condition, M-FinFET contributes an efficient value of early voltage.

Study of RF performance:

To evaluate the RF performance [40], various figures of merit (FOM) such as gate capacitance (C_{gg}), transconductance frequency product (TFP), cut-off frequency (F_t), gain frequency product (GFP), and transconductance frequency product (GTFP) have been demonstrated shown in Fig.6.

The gate capacitance and cut-off frequency performance are investigated by including the introduction of trap/without trap charges shown in Fig. 6a &b. C_{gg} and F_t performance of the M-FinFET device is affected by the influence of trap charges. C_{gg} value increases as gate bias increased. And in presence of positive and negative traps, C_{gg} performance is prominent.

. On the other hand, cut-off frequency ($F_t=G_m/2\pi C_{gg}$) is defined as the frequency at which gain is one. It is seen from Fig. 5b F_t increases at very low gate voltage due to

higher value of G_m and lower value of C_{gg} that enhances the gate controllability and highest value of F_t is obtained due to various interface traps effect.

Another, two RF parameters like gain frequency product (GFP) and gain transconductance frequency product (GTFP) [41] against gate voltage have been shown in Fig. 6c&6d respectively.

GFP and GTFP can be determined by

$$GFP = \left(\frac{G_m}{G_d}\right)F_t \quad \text{..... (1)}$$

$$GTFP = \left(\frac{G_m}{G_d}\right)\left(\frac{G_m}{I_d}\right)F_t \quad \text{..... (2)}$$

The effect of positive and negative traps has a substantial impact on the GFP and GTFP characteristics of the device. As result, the value of GFP and GTFP is more due to interface traps as compared to without trap condition. And peak value of GFP and GTFP is examined under the guidance of a positive trap at very low gate voltage.

Transconductance frequency product ($TFP=G_m/I_d*F_t$) is a very useful RF parameter and TFP versus V_{GS} has shown in Fig. 6e. An insignificant variation of TFP is observed from low gate bias to high gate bias due to positive and negative trap effects. As G_m and F_t value increases at very low gate bias, TFP value also increases that indicating lesser mobility degradation in the device.

Study of Linearity performance:

Linearity analysis is very essential for any circuit performance [42]. Linearity of parameters signifies less distortion at the output. Voltage intercept point (VIP) is very essential for linearity parameters and becomes very fundamental in RF application [43]. The second-order harmonics called VIP2 can be defined as

$$VIP2 = 4\frac{G_m}{G_{m_2}} \quad \text{..... (3)}$$

Third-order harmonics called VIP3 can be determined as

$$VIP3 = \sqrt{24\frac{G_m}{G_{m_3}}} \quad \text{..... (4)}$$

VIP2 and VIP3 performance of M-FinFET with/without trap condition has shown in Fig. **7a&b.** The higher value of VIP2 and VIP3 indicates better linearity performance of the device. With a negative trap condition, a peak value of VIP2 is obtained. On other hand, the M-FinFET device with a positive trap exhibits maximum VIP3 as compared to other variations.

Another essential linearity parameter called 1dB compression point and its efficiency can be improved if the input power level provides less amount of output power level. The 1dB compression point performance against gate bias has shown in Fig. **7c** in the presence and absence of traps. A larger degradation of 1dB compression point is noticed in without trap condition whereas interface trap (positive and negative trap) provides an efficient value of 1dB compression point due to high value of transconductance. It indicates M-FinFET device has a remarkable impact for various interface traps (positive and negative trap).

Conclusion:

In this work, we have successfully investigated the impact of different interface trap charges (ITC) on the device performance of the M-FinFET structure. Various interface traps such as positive and negative traps having different trap concentrations have been studied to examine the dependability of device performance. The various DC parameters such as I_{ON}, V_{th}, SS, G_{mpeak}, and $I_{ON/OFF}$ (switching ratio) are calculated with the consideration of the presence and absence of traps, comparatively. The important highlights from this simulation study are: the presence of interface trap at oxide/channel interface maximizes the drive current without degrading of I_{OFF} in M-FinFET device. And about 5.14 times enhancement of ON current can be noticed as compared to no trap condition. Careful optimization of trap concentration of positive trap reduces the V_{th} and SS when trapping concentration value is decreases from $10^{13}/cm^2$ to $10^{12}/cm^2$. While we analyzed, the device has a negligible effect of negative trap concentration on V_{th} (~0.26V) and SS (~82mV/dec). A high value of GTFP, GFP, F_t, C_{gg}, and A_v has

achieved in presence of positive and negative traps which helps to promote this device for high frequency (RF) applications. Superior enhancement of linearity performance like VIP2, VIP3, and 1dB compression point has developed with interface trap effect.

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Tables:

Table 1 comparative analysis of M-FinFET with other FinFET devices

Reference	Device structure	parameters	Output performance(I_{ON})
[36]	GaN SOI FinFET	Lg=8nm,	0.8mA
[37]	NC Ge FinFET	Lg=20nm	10^{-5}A
[38]	TG JL SOI FinFET	Lg=5nm	$1.89x10^{-4}$A
Proposed structure	M-FinFET	Lg=10nm	3.51mA

Table 2 DC parameters of M-FinFET in presence and absence of trap

parameter	Without traps	Positive trap	Negative trap
I_{ON}(mA)	3.46	18.44	18.62
Vth(V)	0.199	0.274	0.260
SS(mV/dec)	87	60.1	82.4
G_{mpeak}(mS)	3.61	16.033	16.030
Switching ratio	$1.15x10^{16}$	$1.8x10^{14}$	$2.78x10^{14}$

Figures

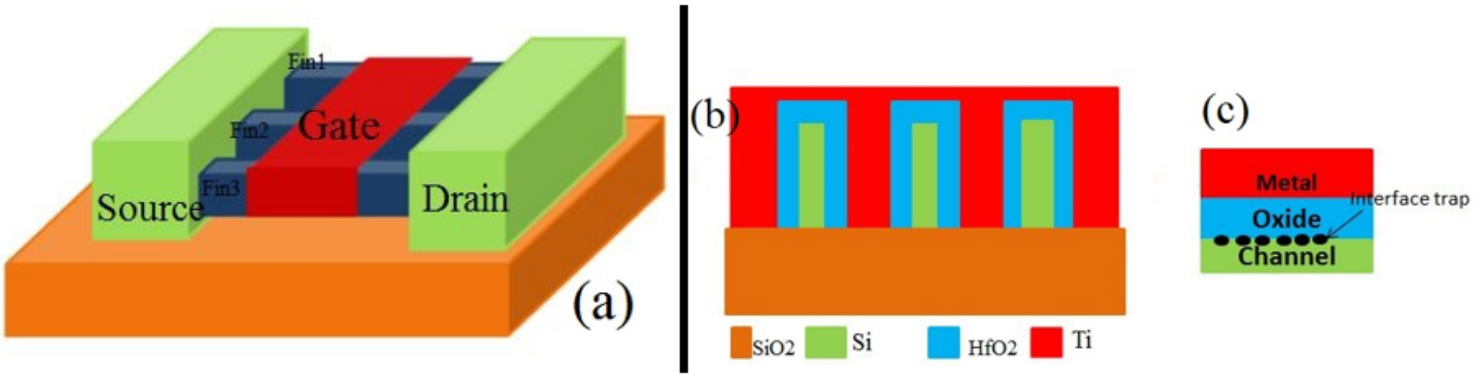

Figure 1

M-FinFET structure (a) 3D view (b) 2D cross-section view (c) enlarged view

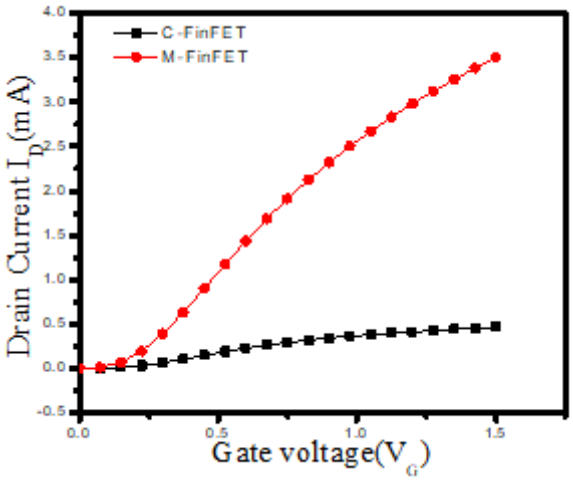

Figure 2

Id –Vgs transfer characteristics of Conventional FinFET& M-FinFET

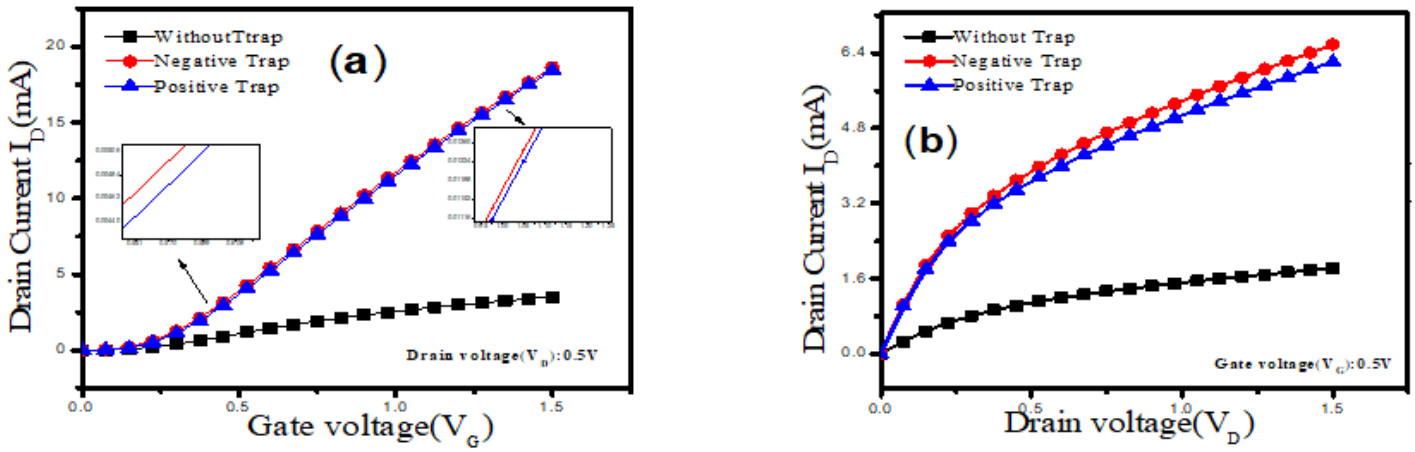

Figure 3

Transfer characteristics of M-FinFET structure (a) ID –Vgs (b) ID –Vds

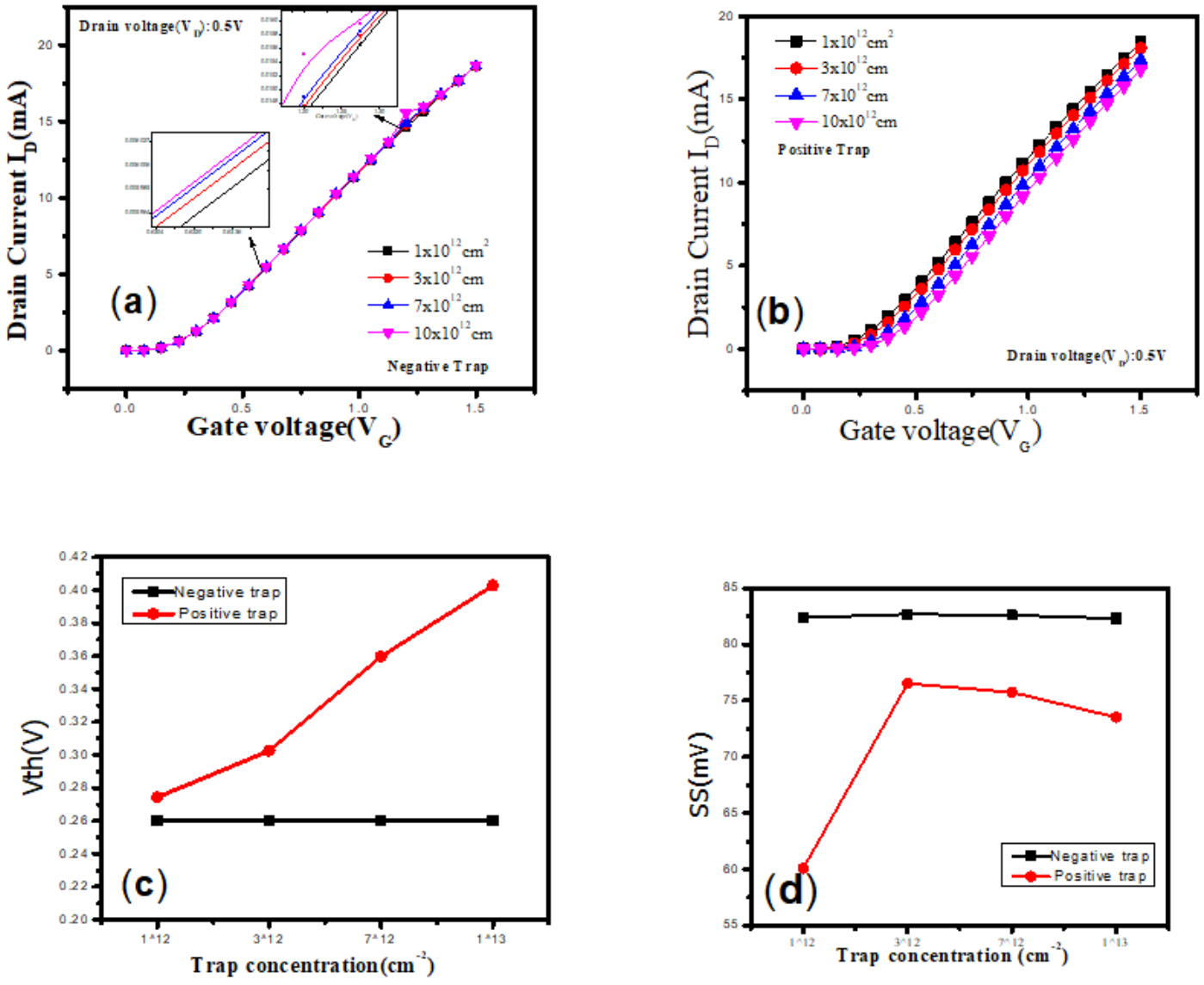

Figure 4

Transfer characteristics of M-FinFET structure (a) ID –Vgs (b) ID –Vds and SCEs performance (c) Vth-TC (d) SS-TC

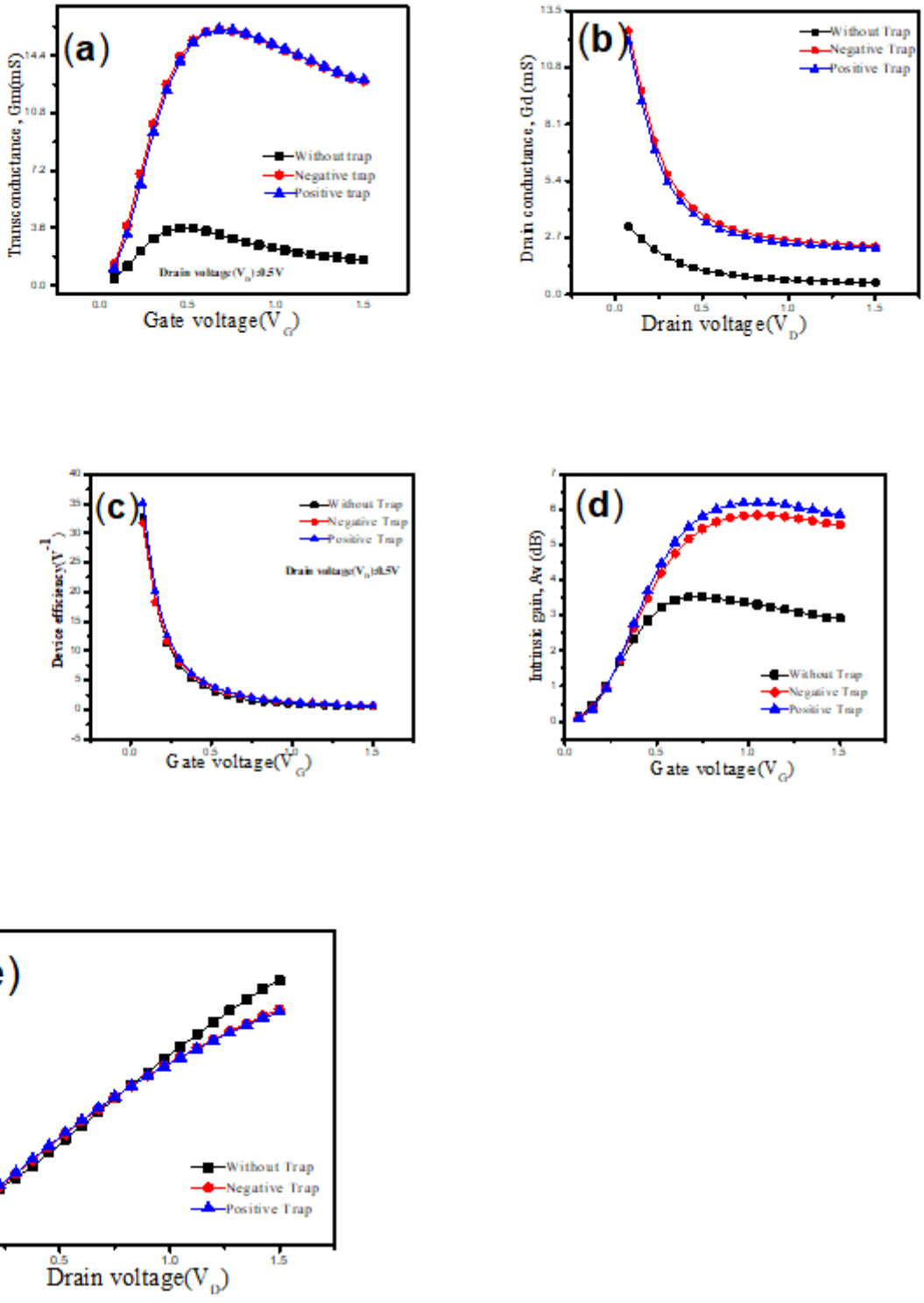

Figure 5

Analog performance (a) transconductance ~gate voltage (b) drain conductance ~drain voltage (c) device efficiency ~ gate voltage (d) intrinsic gate ~gate voltage e early voltage ~Drain voltage

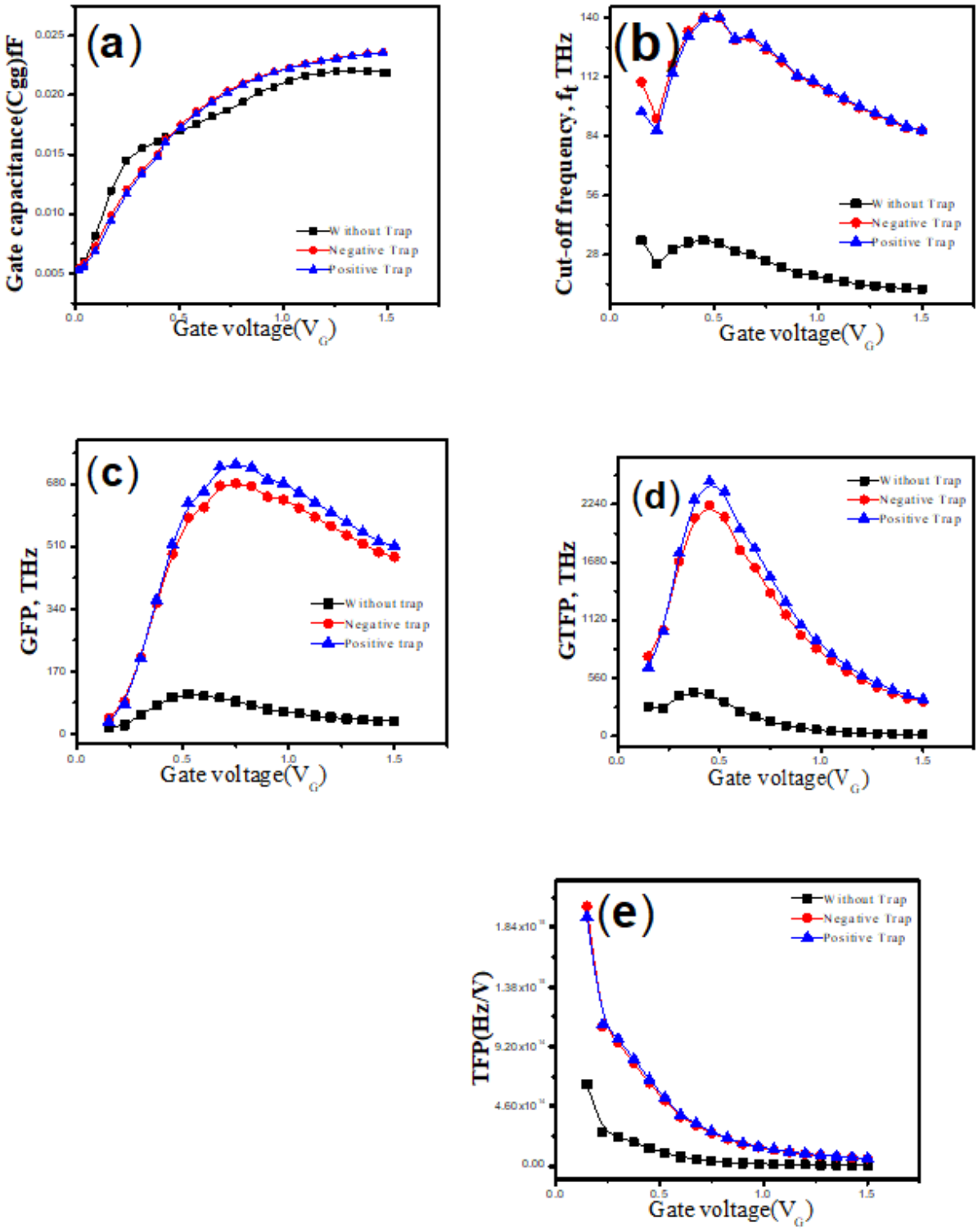

Figure 6

RF performance (a) gate capacitance ~gate voltage (b) cut-off frequency ~gate voltage (c) GFP ~gate voltage (d) GTFP ~gate voltage (e) TFP ~gate voltage

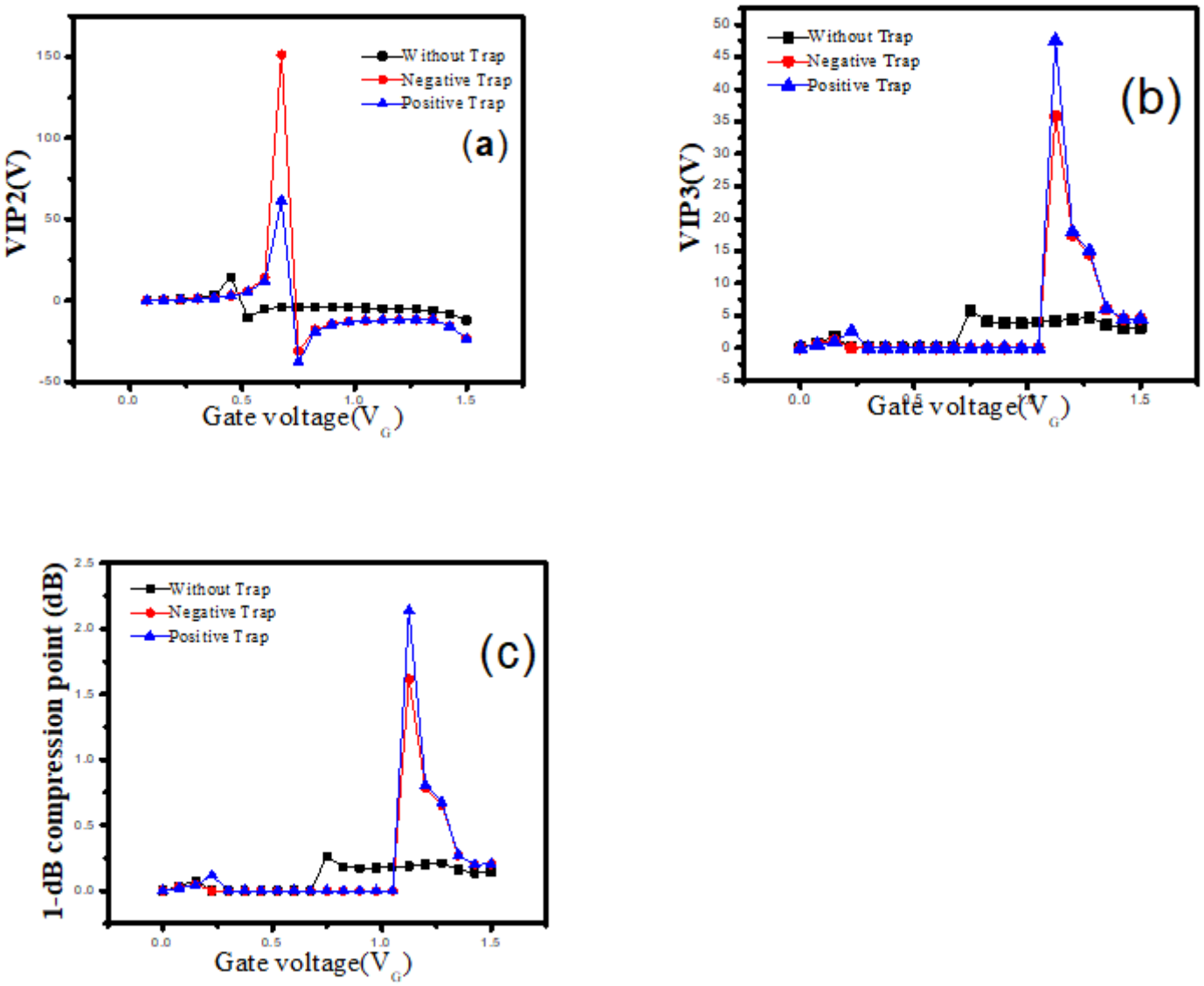

Figure 7

Linearity performance (a) VIP3~gate voltage (b) VIP3~ gate e voltage (c) 1dB compression point ~ gate voltage