

# Drain Current Modeling of Tunnel FET using Simpson's Rule

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## Research Article

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# Drain Current Modeling of Tunnel FET using Simpson's Rule

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**Abstract** Tunnel Field Effect Transistor can be introduced as an emerging alternate to MOSFET which is energy efficient and can be used in low power applications. Due to the challenge involved in integration of band to band tunneling generation rate, the existing drain current models are inaccurate. A compact analytical model for simple tunnel FET and pnpn tunnel FET is proposed which is highly accurate. The numerical integration of tunneling generation rate in the tunneling region is performed using Simpson's rule. Integration is done using both Simpson's 1/3 rule and 3/8 rule and the models are validated against numerical device simulations. The models are compared with existing models and it is observed that the proposed models show excellent agreement with device simulations in the entire region of operation with Simpson's 3/8 rule exhibiting the maximum accuracy.

**Keywords** Band to band tunneling · Drain current modeling · Simpson's Rule · Tunnel Field Effect Transistor

## 1 Introduction

Tunnel Field Effect Transistor (TFET) has been identified as a viable alternate to MOSFET in the nano scale semiconductor device category [1] - [4]. Since the device operates on band to band tunneling (BTBT) [5] - [6] phenomena, it shows better resistance against short channel effects observed in MOSFET. The major advantage of TFET over MOSFET is that it provides a sub threshold slope lesser than the minimum achievable limit of 60 mV/decade for MOSFET. Though the device is ambipolar in nature, the OFF current is comparatively low which makes it popular among memory devices and the device is particularly suitable for low power applications. Developing an accurate and computationally efficient drain current model for TFET becomes important for performing fast and error free circuit simulations. The problem with the TFET device is that it has low ON current. The band-to-band tunneling rate has an exponential dependence [7] on the lateral electric field. Due to the low lateral electric field, the planar p-i-n TFET has low ON state current. TFET with n+ pocket between source and channel is generally known as pnpn TFET and exhibits significant improvement in ON state current. This is because the n+ pocket increases the electric field in the lateral direc-

tion, modulates the energy band profile, and shortens the tunneling width [8].

Several numerical models for TFET drain current [9] [12] reported in literature are computationally complex and hence it is inefficient to do circuit simulations using these models. Investigations on various modeling approaches [13] - [17] point out the need to develop an accurate and computationally efficient analytical model for drain current of TFET. Integration of BTBT generation rate is a major challenge in drain current modeling due to the presence of exponential and polynomial terms. Tangent line approximation [18] - [19] is one of the preferred method for integration of BTBT generation rate. The tangent line approximation can be used to approximate functional values that deviate slightly from exact values. Another method is to perform integration by approximating the function as exponential and neglecting the polynomial term [15].

This paper reports a compact analytical drain current model for planar TFET which is accurate in the entire operating range. The model is extended to pnpn TFET structure and it shows commendable accuracy. Here, the drain current model is formulated by numerical integration of BTBT generation rate using Simpson's rule. Both 1/3 and 3/8 rule is employed for model derivation and the models are compared for its accu-

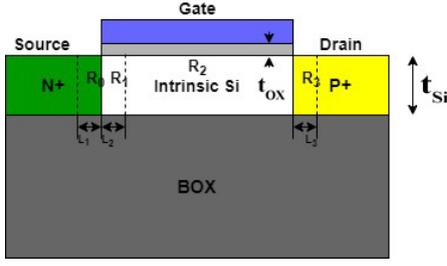


Fig. 1 Schematic view of p-channel SOI TFET

racy. BTBT generation rate is a function of electric field which is derived from surface potential. The model is validated against 2D numerical device simulation using Silvaco Atlas [20]. The device simulation tool is calibrated against published experimental data [16] - [17] [21] - [28]. A Cross section of p-channel SOI TFET used for simulation and validation is shown in Fig. 1.

The drain current model published in literature [17], due to its tangent line approximation of the parabolic function has limited accuracy. Simpson's rule approximates BTBT generation rate function as parabolic segments. Hence, the proposed method of drain current formulation demonstrates excellent match with the device simulations.

The paper is organized in the following manner. Section II discusses model development followed by model validation in section III. Section IV concludes the work.

## 2 Model Development

The investigation is performed on a planar p-channel SOI TFET having with channel length ( $L$ ) = 200 nm, length of source region ( $L_S$ )=50 nm, length of drain region ( $L_{D_r}$ )=50 nm, body doping ( $N_A$ ) =  $10^{15}/\text{cm}^3$ , source ( $N_S$ ) =  $10^{20}/\text{cm}^3$ , drain doping ( $N_{D_r}$ ) =  $10^{19}/\text{cm}^3$ , thickness of oxide layer ( $t_{ox}$ ) = 2 nm, thickness of silicon film ( $t_{Si}$ ) = 10 nm, and work function of gate-metal is  $\phi = 4.8$  eV [13].

Drain current is formulated by the integration of generation rate over the entire volume. An accurate surface potential model and an error free integration method result in drain current model with high level of accuracy.

### 2.1 Surface Potential and Electric Field

The surface potential of p-channel TFET with respect to distance along the channel is plotted in Fig. 2. From the plot it is observed that in region  $R_2$  the potential is almost constant and is represented as  $\psi_C$ . Since  $\psi_C$  is

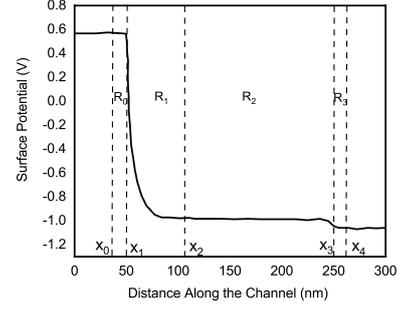


Fig. 2 Plot of surface potential vs distance along the channel showing the classification of regions of the p-channel TFET for  $V_{GS} = -1$  V and  $V_{DS} = -0.5$  V [17]

constant in this region, the electric field in this region becomes negligible.

2D Poisson equation for the surface potential of TFET [17] is given by

$$\frac{\delta^2}{\delta x^2} (\psi, y) + \frac{\delta^2}{\delta y^2} (\psi, y) = \frac{qN_A}{\epsilon_{Si}} \quad (1)$$

Applying parabolic approximation [26] of potential in  $y$  direction and substituting  $y=0$  in equation (1) to obtain surface potential as

$$\psi_{sj}(x) = C_j \exp\left(\frac{x}{L_{dj}}\right) + D \exp\left(\frac{-x}{L_{dj}}\right) + \psi(G) - \frac{qN_A L_{dj}^2}{\epsilon_{Si}} \quad (2)$$

where  $L_{dj}$  is the characteristic length and in region  $R_1$ , it is given by

$$L_{d1} = \sqrt{\frac{t_{Si} t_{ox} \epsilon_{Si}}{\epsilon_{ox}}} \quad (3)$$

The gate potential  $\psi(G)$  can be expressed as

$$(G) = V_{GS} - V_{FB} \quad (4)$$

where  $V_{FB}$  is the flat band voltage.

Applying boundary conditions, the final solution for the surface potential in  $R_1$  [17] is

$$\psi_{s1}(x) = (\psi_C - \psi_G) \cosh^{-1} \left( \frac{x - (L_{d1} \cosh^{-1}(V_{bi}/(\psi_C - \psi_G)))}{L_{d1}} \right) + \psi_G \quad (5)$$

and in  $R_2$

$$\psi_{s3}(x) = \psi_C \quad (6)$$

The electric field is given by

$$E(x) = -\frac{\delta \psi_{sj}(x)}{\delta x} \quad (7)$$

This field is applied to the tunneling generation rate to find the drain current.

## 2.2 Surface Potential in Source Body and Drain body Depletion Regions

The parabolic approximation adopted in region  $R_1$  is valid for depletion regions. Considering the gate fringing field, boundary conditions relating to continuity of electric field varies in the depletion region. This is due to the modified gate body capacitance generally known as fringing capacitance. The gate body capacitance is modified by applying conformal mapping techniques [29], and is shown in equation(8)

$$C_{oxf} = \frac{2}{\pi} C_{ox} \quad (8)$$

So the boundary condition changes as

$$\frac{\partial \psi}{\partial y} (\text{at } y = 0) = \frac{-C_{oxf}(\psi_G - \psi_{s0})}{\epsilon_{Si}} \quad (9)$$

Applying this boundary condition in Region  $R_0$

$$\psi_{s0} = C_0 \exp\left(\frac{x - x_i}{L_{d0}}\right) + D_0 \exp\left(-\frac{x - x_i}{L_{d0}}\right) + \psi_G - \frac{2qN_0 L_{d0}^2}{\epsilon_{Si}} \quad (10)$$

where

$$L_{d0} = \sqrt{\frac{\pi t_{Si} t_{ox} \epsilon_{Si}}{2\epsilon_{ox}}} \quad (11)$$

and

$$\psi_G - \frac{2qN_j L_{dj}^2}{\epsilon_{Si}} = \psi_{Cj} \quad (12)$$

where  $N_j$  is the doping in  $j^{\text{th}}$  region. Similar equations can be written in drain body depletion region.

In the source body depletion region, the boundary conditions in x direction are

$$\psi_{s0}(x_i) = V_S + V_{bi0} \quad (13)$$

$$\frac{\partial \psi_{s0}}{\partial x} (\text{at } x = x_i) = 0 \quad (14)$$

where  $V_{bi0}$  is the built-in voltage of the source body region. Similarly, boundary conditions in x direction at drain body depletion region are

$$\psi_{s3}(x_2) = V_{DS} + V_{bi2} \quad (15)$$

$$\frac{\partial \psi_{s2}}{\partial x} (\text{at } x = x_2) = 0 \quad (16)$$

where  $V_{bi2}$  is the built-in voltage of the drain body region. At the source body and drain body interface, applying boundary continuity of surface potential and electric field displacement the surface potential is obtained as

$$\psi_{sj}(x_{j-1}) = \psi_{sj-1}(x_{j-1}) \quad (17)$$

$$\frac{\partial \psi_{sj}}{\partial x} (\text{at } x = x_{j-1}) = \frac{\partial \psi_{sj-1}}{\partial x} (\text{at } x = x_{j-1}) \quad (18)$$

Substituting equation (10) into equation (17) and equation (18)

$$2D_{j+1} = \left(1 - \frac{L_{dj+1}}{L_{dj}}\right) e^{-\frac{L_j}{L_{dj}}} C_j + \left(1 + \frac{L_{dj+1}}{L_{dj}}\right) e^{\frac{L_j}{L_{dj}}} D_j + (\psi_{Cj} - \psi_{Cj+1}) \quad (19)$$

$$2C_{j+1} = \left(1 - \frac{L_{dj+1}}{L_{dj}}\right) e^{-\frac{L_j}{L_{dj}}} C_j + \left(1 + \frac{L_{dj+1}}{L_{dj}}\right) e^{\frac{L_j}{L_{dj}}} D_j + (\psi_{Cj} - \psi_{Cj+1}) \quad (20)$$

By applying diode approximation, the depletion region lengths are given by

$$L_1 = \sqrt{\frac{2\epsilon_{Si} |\psi_{C2} - V_S| N_2}{q |N_1| (|N_1 + N_2|)}} \quad (21)$$

$$L_3 = \sqrt{\frac{2\epsilon_{Si} |V_{DS} - \psi_{C2}| N_2}{q |N_4| (|N_4 + N_2|)}} \quad (22)$$

$C_0$ ,  $C_2$ ,  $D_0$  and  $D_2$  are obtained by solving equations (19) and (20).

## 2.3 BTBT Generation Rate

Kane's band to band tunneling model [30] is derived with constant electric field applied to time independent Schrodinger equation. In this model, the basis function was represented using Bloch function. For evaluating transmission probability, Kane applied perturbation theory. Though the derivation involved in Kane's model is complex, an expression for tunneling per cubic centimeter can be derived which is given by.

$$G_{BTB} = \frac{E^2 m^{*1/2}}{18\pi \hbar^2 E_g^{1/2}} \exp\left[\frac{-\pi E_g^{3/2} m^{*1/2}}{2\hbar E}\right] \quad (23)$$

where  $E$  is the uniform electric field,  $m^*$  is the effective mass of the carrier and  $E_g$  represents the band gap energy. Equation (23) can be reduced to

$$G_{BTB} = A E^2 \exp\left[\frac{-B}{E}\right] \quad (24)$$

Keldysh *et.al* [31] modified equation (24) to

$$G_{BTB} = A E^{2.5} \exp\left[\frac{-B}{E}\right] \quad (25)$$

In both cases, the parameters  $A$  and  $B$  are linear and exponential parameters respectively.

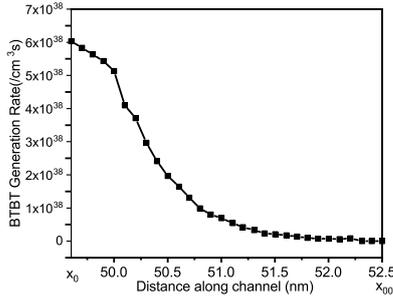


Fig. 3 Plot of BTBT generation rate along the channel

#### 2.4 Drain Current Model using Simpson's Rule

The band to band tunneling generation rate in source body depletion region is given by equation (25) and is plotted in Fig 3. The expression contains polynomial as well as exponential terms which limits direct integration. Extensive modeling approximation can be adopted in such cases, by eliminating the polynomial term, if the accuracy is not compromised. Here, if such approximations are made, the drain current model becomes highly inaccurate. So band to band tunneling generation rate is numerically integrated over the entire tunneling volume to obtain the drain current. The numerical method used here is Simpson's rule which is an extension of trapezoidal rule. Numerical integration is performed using both Simpson's 1/3 rule and 3/8 rule.

#### 2.5 Model using Simpson's 1/3 rule

In this approach, the integrand is obtained by approximating it as second order polynomial. The drain current is given as

$$I_D = q \int G_{BTB}(x) dx \quad (26)$$

The tunneling region along the channel is defined from  $x_0$  to  $x_{00}$  as shown in Fig. 3. The  $G_{BTB}$  function is approximated to a second order polynomial and integrated over the tunneling region yields

$$\int_{x_0}^{x_{00}} G_{BTB}(x) dx = \int_{x_0}^{x_{00}} (a_0 + a_1x + a_2x^2) dx \quad (27)$$

$$\int_{x_0}^{x_{00}} G_{BTB}(x) dx = a_0(x_{00} - x_0) + a_1 \frac{x_{00}^2 - x_0^2}{2} + a_2 \frac{x_{00}^3 - x_0^3}{3} \quad (28)$$

To evaluate the polynomial coefficients  $a_0$ ,  $a_1$  and  $a_2$ , choose three points in the  $x$  axis of the graph shown

in Fig.3. The three points are  $x_0$ ,  $x_{00}$  and the mid point of  $x_0$  and  $x_{00}$ .  $x_{00}$  is the point where BTBT tunneling generation rate approaches zero.

$$G_{BTB}(x_0) = a_0 + a_1x_0 + a_2x_0^2 \quad (29)$$

$$G_{BTB}\left(\frac{x_0 + x_{00}}{2}\right) = a_0 + a_1\left(\frac{x_0 + x_{00}}{2}\right) + a_2\left(\frac{x_0 + x_{00}}{2}\right)^2 \quad (30)$$

$$G_{BTB}(x_{00}) = a_0 + a_1x_{00} + a_2x_{00}^2 \quad (31)$$

solving above three equations yields

$$a_0 = \frac{x_0^2 G_{BTB}(x_{00}) + x_0 x_{00} G_{BTB}(x_0) - 4x_0 x_{00} G_{BTB}\left(\frac{x_0 + x_{00}}{2}\right) + x_0 x_{00} G_{BTB}(x_0) + x_{00}^2 G_{BTB}(x_{00})}{x_0^2 - 2x_0 x_{00} + x_{00}^2} \quad (32)$$

$$a_1 = -\frac{x_0 G_{BTB}(x_0) - 4x_0 G_{BTB}\left(\frac{x_0 + x_{00}}{2}\right) + 3x_0 G_{BTB}(x_{00}) + 3x_{00} G_{BTB}(x_0) - 4x_{00} G_{BTB}\left(\frac{x_0 + x_{00}}{2}\right) + x_{00} G_{BTB}(x_{00})}{x_0^2 - 2x_0 x_{00} + x_{00}^2} \quad (33)$$

$$a_2 = 2 \frac{G_{BTB}(x_0) - 2G_{BTB}\left(\frac{x_0 + x_{00}}{2}\right) G_{BTB}(x_{00})}{x_0^2 - 2x_0 x_{00} + x_{00}^2} \quad (34)$$

Substituting the coefficients  $a_0$ ,  $a_1$  and  $a_2$  from equations (32) to (34) in equation (28) and multiplying the integral by electronic charge,  $q$  yields the drain current in equation (26) as

$$I_D = qZ \frac{l_{\text{tunnel}}}{6} \left[ G_{BTB}(x_0) + 4G_{BTB}\left(\frac{x_0 + x_{00}}{2}\right) + G_{BTB}(x_{00}) \right] \quad (35)$$

Here  $x_0$  and  $x_{00}$  are boundaries of tunneling region [17].

$$x_0 = L_S - L_1 \quad (36)$$

$$x_{00} = L_S + L_{d1} \cosh^{-1}((\psi_{s1} - \psi_G - E_g/q) - (\psi_C - \psi_G)) \quad (37)$$

$$l_{\text{tunnel}} = x_{00} - x_0 \quad (38)$$

$Z$  is given by

$$Z = \frac{A t_{\text{inversion}}}{\sqrt{E_g}}$$

where  $t_{\text{inversion}}$  is the inversion layer thickness  $A$  is the BTBT parameter given by (25). This analytical model provides a closed form equation for drain current which is suitable for circuit simulations.

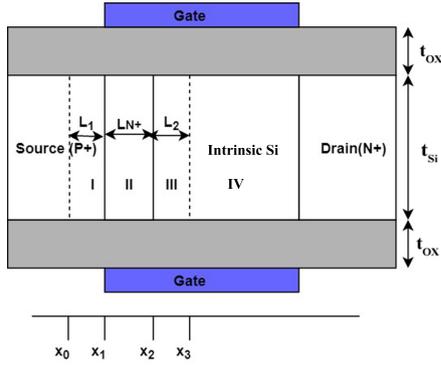


Fig. 4 Schematic of the double-gate pnpn TFET structure

### 2.5.1 Model using Simpson's 3/8 Rule

Simpson's 3/8 rule for integration is derived by approximating the given function with the third order (cubic) polynomial.

$$G_{BTB}(x) = a_0 + a_1x + a_2x^2 + a_3x^3 \quad (39)$$

To evaluate the polynomial coefficients  $a_0$ ,  $a_1$ ,  $a_2$  and  $a_3$ , choose four points in the  $x$  axis of the graph shown in Fig.3. The four points are  $x_0$ ,  $x_{01}$ ,  $x_{02}$ ,  $x_{00}$ . Where  $x_{01}$  and  $x_{02}$  are given by

$$x_{01} = x_0 + \frac{l_{tunnel}}{3} \quad (40)$$

$$x_{02} = x_0 + \frac{2l_{tunnel}}{3} \quad (41)$$

$$G_{BTB}(x_0) = a_0 + a_1x_0 + a_2x_0^2 + a_3x_0^3 \quad (42)$$

$$G_{BTB}(x_{01}) = a_0 + a_1x_{01} + a_2x_{01}^2 + a_3x_{01}^3 \quad (43)$$

$$G_{BTB}(x_{02}) = a_0 + a_1x_{02} + a_2x_{02}^2 + a_3x_{02}^3 \quad (44)$$

$$G_{BTB}(x_{00}) = a_0 + a_1x_{00} + a_2x_{00}^2 + a_3x_{00}^3 \quad (45)$$

Solving for  $a_0$ ,  $a_1$ ,  $a_2$  and  $a_3$  and substituting in  $G_{BTB}(x)$ , the drain current computed with Simpson's 3/8 rule is obtained as

$$I_D = qZ \frac{l_{tunnel}}{8} [G_{BTB}(x_0) + 3G_{BTB}(x_{01}) + 3G_{BTB}(x_{02}) + G_{BTB}(x_{00})] \quad (46)$$

This analytical model provides a closed form equation for drain current.

## 2.6 Drain Current Model for pnpn TFET

In comparison with the p-i-n TFET, the pnpn TFET structure is more promising for low-power circuit design [32]. Fig. 4 shows the cross section of the device considered in the analysis with gate length ( $L_G$ ) = 60 nm, body doping ( $N_3 = N_4$ ) =  $10^{15}/\text{cm}^3$ , source and drain doping ( $N_S$  and  $N_{Dr}$ ) =  $10^{20}/\text{cm}^3$ , length of source/drain regions ( $L_S/L_{Dr}$ ) = 70 nm, pocket length ( $L_{N+}$ ) = 6nm, pocket doping ( $N_{N+}$ ) =  $2 \times 10^{19}/\text{cm}^3$ , thickness of oxide layer ( $t_{ox}$ ) = 2 nm, thickness silicon film ( $t_{si}$ ) = 10 nm, and work function of gate-metal  $\phi = 4.33$  eV [33].

Using parabolic approximation the surface potential of the device[26] is found out to be

$$\psi_{Sj}(x) = C_j e^{u(x-x_{j-2})} + D_j e^{-u(x-x_{j-2})} + \psi_{dj} \quad (47)$$

where  $1/u$  is the characteristic length and  $j = 2-4$  is applicable for regions II – IV respectively.

In region I the potential is given by

$$\psi_{s1}(x) = \frac{qN_{eff}}{2\epsilon_{Si}}(x + L_1)^2 - \psi_{src} \quad (48)$$

where

$$N_{eff} = N_{src} - \frac{2C_f}{qt_{Si}}(V_{GS} - V_{FB} - \psi_{src}) \quad (49)$$

$$\psi_{src} = -\frac{kT}{q} \ln \frac{N_S}{n_i} \quad (50)$$

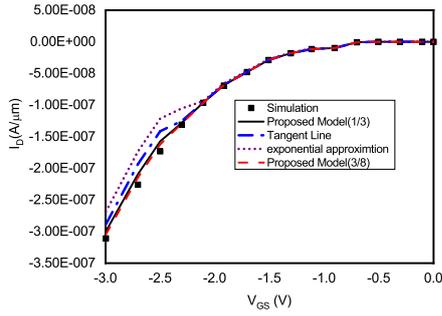
Expression for  $x_0$  remains the same as in equation (36) and the value of  $x_k$  [26] changes to

$$x_k = L_S + \frac{1}{u_3} \cosh^{-1}((\psi_{s2} - \psi_G - E_g/q) - (\psi_C - \psi_G)) \quad (51)$$

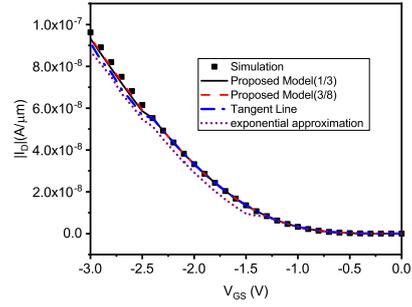
Electric field is obtained as the derivative of surface potential and is applied in generation rate. Drain current is modeled using Simpson's 1/3 and 3/8 rule by applying generation rate in equation (35) and (46) respectively.

## 3 Model Validation

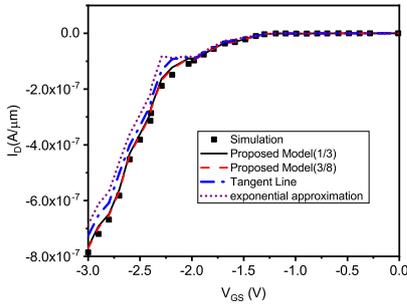
Even after the availability of an accurate surface potential model, it is difficult to obtain a drain current model by direct integration due to the reason specified in section II. In this paper, a novel method of drain current formulation using a numerical integration method called Simpson's 1/3 rule and Simpson's 3/8 rule is proposed. To evaluate the suitability of the model, the proposed drain current model is compared with the device simulations. While performing the device simulations, the



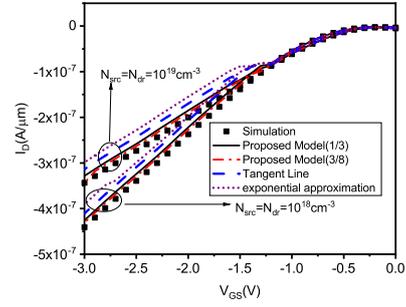
**Fig. 5** Comparison of  $I_D$  vs  $V_{GS}$  given by the proposed model, existing model [17] and device simulation for P channel TFET with  $V_{DS} = -0.05V$



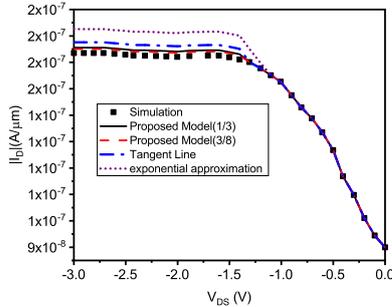
**Fig. 8** Comparison of  $I_D$  vs  $V_{GS}$  given by the proposed model, existing model [17] and device simulation for P channel TFET with  $V_{DS} = -0.05V$  with 20nm channel length



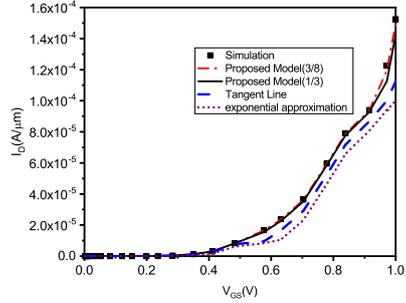
**Fig. 6** Comparison of  $I_D$  vs  $V_{GS}$  given by the proposed model, existing model [17] and device simulation for P channel TFET with  $V_{DS} = -2V$



**Fig. 9** Comparison of  $I_D$  vs  $V_{GS}$  given by the proposed model, existing model [17] and device simulation for P channel TFET with  $V_{DS} = -0.05V$  for different source and drain doping



**Fig. 7** Comparison of  $I_D$  vs  $V_{DS}$  curve given by the proposed model, existing model [17] and device simulation for P channel TFET with  $V_{GS} = -2V$

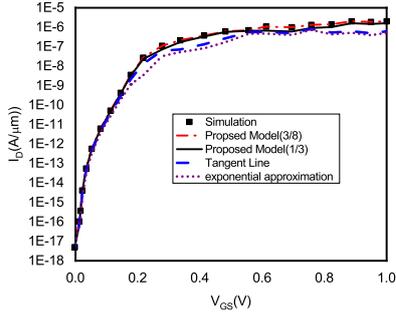


**Fig. 10** Comparison of  $|I_D|$  vs  $V_{GS}$  given by the proposed model, existing models and device simulation for  $V_{DS} = 1V$  for npn TFET

models used are concentration dependent mobility, electric field dependent mobility, Shockley-Read-Hall recombination, Auger recombination, bandgap narrowing and Kane's band-to-band tunneling. The constants in Kane's band-to-band tunneling model is fixed as  $A_{Kane} = 4 \times 10^{19}$  and  $B_{Kane} = 41$  [20] so that they resemble experimental results [25]. The proposed models are also compared with the existing drain current models derived by applying tangent line approxima-

tion [17] and by neglecting the polynomial term in the band to band tunneling generation rate [15].

Fig. 5 and Fig. 6 shows the validation of models with device simulation when  $V_{DS}$  is  $-0.05V$  and  $-2V$  respectively. The proposed models show excellent agreement with the device simulations for the entire range of  $V_{GS}$ . Model With Simpson's 3/8 rule (equation (44)) is slightly more accurate than that with Simpson's 1/3 rule (equation 35). However, the computational time



**Fig. 11** Comparison of  $I_D$  vs  $V_{GS}$  in log scale given by the proposed model, existing models and device simulation for  $V_{DS} = 0.2V$  for pnpn TFET

associated with Simpson's 3/8 rule, because of its third order polynomial approximation is significantly higher than the one associated with Simpson's 1/3 rule which uses only second order polynomial approximation. Fig. 7 shows the output characteristics ( $I_D$ - $V_{DS}$ ) for  $V_{GS} = -2V$ . The proposed models has a slight error in the saturation region. This is due to the inaccuracy of surface potential model at high drain voltages.

A short-channel TFET with channel length of 20 nm is also used in th analysis and compared with the models in Fig. 8. The proposed models are in good agreement with the simulation results and hence the model is suitable upto a channel length of 20 nm.

In the existing method [17], drain current is calculated by integration of generation rate using tangent line approximation. Integration is done by dividing the tunneling generation rate shown in Fig. 3 into linear segments and calculating the area under the graph using triangular approximation. On the other hand, Simpson's rule approximates the graph with sequence of quadratic parabolic segments instead of straight lines. This makes the model more accurate which closely portrays the device behavior in the entire operating range.

In the existing model, the tangent line is drawn to the generation rate function  $y = G_{btb}(x)$  at a particular point  $x = a$  and the value of  $y$  is then linearly approximated. Now the linear approximation to  $G_{btb}(x)$  is written as

$$L(x) = G_{btb}(a) + G'_{btb}(a)(x - a) \quad (52)$$

If the possible error in  $x$  is  $x_e$ , the possible error in  $y$  is given by

$$y_e = x_e \left[ \frac{dy}{dx} \right]_{x=a} \quad (53)$$

Here  $x_e$  depicts the error in surface potential and  $y_e$  is the total error in drain current. This demonstrates the mismatch of the existing drain current model with the

actual device behavior in saturation region as shown in Fig. 7. The model is also validated with different source and drain dopings as shown in Fig. 9. The proposed model is accurate with different doping concentrations.

The proposed drain current models for pnpn TFET is validated against numerical device simulations. So far, no published models are there for the drain current of pnpn TFET. Fig. 10 and Fig. 11 shows the  $I_D$  vs  $V_{GS}$  plot for  $V_{DS} = 1V$  and  $V_{DS} = 0.2V$  respectively. The plots show excellent match between the models and simulation results for different device parameters.

## 4 Conclusion

In this paper, a compact analytical models for the drain current of a planar TFET and pnpn TFET are reported. Investigations on the drain current modeling approaches indicate the need for an accurate method for integration of tunneling generation rate in the source body junction. The proposed modeling approach is based on integration of the tunneling generation rate by Simpson's rule. Both 1/3 and 3/8 rule are used for numerical integration of tunnelling generation rate function. The band to band tunneling generation function is approximated by sequence of quadratic parabolic segments in both the proposed models, whereas in the existing model with tangent line approximation, it is done by straight line segments. While developing the model the source side depletion region is also taken into account. The results demonstrate excellent agreement of the model with device simulations. The accuracy is proved in both ON state and subthreshold region for different device dimensions.

## Declarations

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### Conflict of Interest

The authors declare that they have no conflict of interest

## Author Contributions

- 1 **Arun A V**: Conceptualization, formal analysis, investigation methodology, device simulation, mathematical modeling, validation, writing- original draft.
- 2 **Minu K K**: Mathematical Analysis, modeling methodology, writing - review and editing.
- 3 **Sreelekshmi P S**: Formal analysis, device simulation, validation
- 4 **Jobymol Jacob**: Conceptualization, formal analysis, investigation methodology, device simulation, mathematical modeling, validation, writing- review and editing, supervision.

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Not applicable

Compliance with ethical standards

Not applicable

Consent to participate

Not applicable

Consent for publication

Not applicable

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## References

1. Datta S, Liu H, Narayanan V. Tunnel FET technology: A reliability perspective. *Microelectronics Reliability* 2014;54(5):861–874. doi.org/10.1016/j.microrel.2014.02.002
2. Wang H, Chang S, Hu Y, He H, He J, Huang Q, et al. A novel barrier controlled tunnel FET. *IEEE electron device letters* 2014;35(7):798–800. doi.org/10.1109/LED.2014.2325058
3. Asra R, Shrivastava M, Murali KV, Pandey RK, Gossner H, Rao VR. A tunnel FET for  $V_{DD}$  scaling below 0.6 V with a CMOS-comparable performance. *IEEE Transactions on Electron Devices* 2011;58(7):1855–1863. doi.org/10.1109/TED.2011.2140322
4. Ionescu AM, Riel H. Tunnel field-effect transistors as energy-efficient electronic switches. *nature* 2011;479(7373):329–337. doi.org/10.1038/nature10679
5. Schenk A, et al. Rigorous theory and simplified model of the band-to-band tunneling in silicon. *Solid-State Electronics* 1993;36(1):19–34. doi.org/10.1016/0038-1101(93)90065-X
6. You KF, Wu CY. A new quasi-2-D model for hot-carrier band-to-band tunneling current. *IEEE Transactions on Electron Devices* 1999;46(6):1174–1179. doi.org/10.1109/16.766880
7. Shen C, Yang LT, Samudra G, Yeo YC. A new robust non-local algorithm for band-to-band tunneling simulation and its application to Tunnel-FET. *Solid-State Electronics* 2011;57(1):23–30. doi.org/10.1016/j.sse.2010.10.005
8. Abdi, Dawit Burusie, and Mamidala Jagadesh Kumar. "In-built N+ pocket pnpn tunnel field-effect transistor." *IEEE Electron Device Letters* 35.12 (2014): 1170-1172. https://doi.org/10.1109/LED.2014.2362926
9. Cui N, Liang R, Wang J, Xu J. Si-based hetero-material-gate tunnel field effect transistor: Analytical model and simulation. In: 2012 12th IEEE International Conference on Nanotechnology (IEEE-NANO) IEEE; 2012. p. 1–5. doi.org/10.1109/NANO.2012.6321906
10. Cui N, Liang R, Wang J, Xu J. Two-dimensional analytical model of hetero strained Ge/strained Si TFET. In: 2012 International Silicon-Germanium Technology and Device Meeting (ISTDM) IEEE; 2012. p. 1–2. doi.org/10.1109/ISTDM.2012.6222412
11. Lee MJ, Choi WY. Analytical model of single-gate silicon-on-insulator (SOI) tunneling field-effect transistors (TFETs). *Solid-State Electronics* 2011;63(1):110–114. doi.org/10.1016/j.sse.2011.05.008
12. Liu L, Mohata D, Datta S. Scaling length theory of double-gate interband tunnel field-effect transistors. *IEEE Transactions on Electron Devices* 2012;59(4):902–908. doi.org/10.1109/TED.2012.2183875
13. Mohammadi, Saeed, and Danial Keighobadi. "A universal analytical potential model for double-gate Heterostructure tunnel FETs." *IEEE Transactions on Electron Devices* 66.3 (2019): 1605-1612. doi.org/10.1109/TED.2019.2895277
14. Keighobadi, D., and S. Mohammadi. "Physical and analytical modeling of drain current of double-gate heterostructure tunnel FETs." *Semiconductor Science and Technology* 34.1 (2018): 015009. doi.org/10.1088/1361-6641/aaeeeb
15. Mohammadi, Saeed, and Hamid Reza Tajik Khaveh. "An analytical model for double-gate tunnel FETs considering the junctions depletion regions and the channel mobile charge carriers." *IEEE Transactions on Electron Devices* 64.3 (2017): 1276-1284. doi.org/10.1109/TED.2017.2655102
16. Verhulst AS, Sorée B, Leonelli D, Vandenberghe WG, Groeseneken G. Modeling the single-gate, double-gate, and gate-all-around tunnel field-effect transistor. *Journal of Applied Physics* 2010;107(2):024518. doi.org/10.1063/1.3277044
17. Vishnoi R, Kumar MJ. An accurate compact analytical model for the drain current of a TFET from subthreshold

- to strong inversion. *IEEE Transactions on Electron Devices* 2015;62(2):478–484. doi.org/10.1109/TED.2014.2381560
18. Mahfouf JF. Influence of physical processes on the tangent-linear approximation. *Tellus A: Dynamic Meteorology and Oceanography* 1999;51(2):147–166. doi.org/10.3402/tellusa.v51i2.12312
  19. Park SK, Droegemeier KK. Validity of the tangent linear approximation in a moist convective cloud model. *Monthly weather review* 1997;125(12):3320–3340. doi.org/10.1175/1520-0493(1997)125
  20. Int S, Santa Clara C, et al. ATLAS device simulation software. Santa Clara, CA, USA 2014;.
  21. Bhushan B, Nayak K, Rao VR. DC compact model for SOI tunnel field-effect transistors. *IEEE transactions on electron devices* 2012;59(10):2635–2642. doi.org/10.1109/TED.2012.2209180
  22. Kane E. Zener tunneling in semiconductors. *Journal of Physics and Chemistry of Solids* 1960;12(2):181–188. doi.org/10.1016/0022-3697(60)90035-4
  23. Young KK. Short-channel effect in fully depleted SOI MOSFETs. *IEEE Transactions on Electron Devices* 1989;36(2):399–402. doi.org/10.1109/16.19942
  24. Kumar MJ, Chaudhry A. Two-dimensional analytical modeling of fully depleted DMG SOI MOSFET and evidence for diminished SCEs. *IEEE Transactions on Electron Devices* 2004;51(4):569–574. doi.org/10.1109/TED.2004.823803
  25. Vishnoi R, Kumar MJ. Compact analytical model of dual material gate tunneling field-effect transistor using interband tunneling and channel transport. *IEEE Transactions on Electron Devices* 2014;61(6):1936–1942. doi.org/10.1109/TED.2014.2315294
  26. Wan J, Le Royer C, Zaslavsky A, Cristoloveanu S. A tunneling field effect transistor model combining interband tunneling with channel transport. *Journal of Applied Physics* 2011;110(10):104503. doi.org/10.1063/1.3658871
  27. Vandenberghe W, Verhulst AS, Groeseneken G, Soree B, Magnus W. Analytical model for point and line tunneling in a tunnel field-effect transistor. In: 2008 International Conference on Simulation of Semiconductor Processes and Devices IEEE; 2008. p. 137–140. doi.org/10.1109/SISPAD.2008.4648256
  28. Verhulst AS, Leonelli D, Rooyackers R, Groeseneken G. Drain voltage dependent analytical model of tunnel field-effect transistors. *Journal of Applied Physics* 2011;110(2):024510. doi.org/10.1063/1.3609064
  29. Zhang, Lining, et al. "An analytical charge model for double-gate tunnel FETs." *IEEE Transactions on Electron Devices* 59.12 (2012): 3217–3223. doi.org/10.1109/TED.2012.2217145
  30. Kane EO. Theory of tunneling. *Journal of applied Physics* 1961;32(1):83–91. doi.org/10.1063/1.1735965
  31. Zheltikov A. Keldysh parameter, photoionization adiabaticity, and the tunneling time. *Physical Review A* 2016;94(4):043412. doi.org/10.1103/PhysRevA.94.043412
  32. Ram, Mamidala Saketh, and Dawit Burusie Abdi. "Dopingless PNP tunnel FET with improved performance: design and analysis." *Superlattices and Microstructures* 82 (2015): 430–437. doi.org/10.1016/j.spmi.2015.02.024
  33. Abdi, Dawit Burusie, and Mamidala Jagadesh Kumar. "2-D threshold voltage model for the double-gate pnpn TFET with localized charges." *IEEE Transactions on Electron Devices* 63.9 (2016): 3663–3668. doi.org/10.1109/TED.2016.2589927