Comprehensive Analysis of SRAM Cell Architectures With 18nm FinFET for Low Power Applications

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Research Article

Keywords: SRAM, Low Power, leakage current, FinFET, Power reduction techniques, SRAM cell layout etc.

Posted Date: June 29th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-620247/v1

Version of Record: A version of this preprint was published at Silicon on August 10th, 2021. See the published version at https://doi.org/10.1007/s12633-021-01290-2.

Abstract

The SRAM cells are used in many applications where power consumption will be the main constraint. The Conventional 6T SRAM cell has reduced stability and more power consumption when technology is scaled resulting in supply voltage scaling, so other alternative SRAM cells from 7T to 12T have been proposed which can address these problems. Here a low power 7T SRAM cell is suggested which has low power consumption and condensed leakage currents and power dissipation. The projected design has a leakage power of 5.31nW and leakage current of 7.58nA which is 84.9% less than the 7T SRAM cell without using the proposed leakage reduction technique and it is 22.4% better than 6T SRAM and 22.1% better than 8T SRAM cell when both use the same leakage reduction technique. The cell area of the 7T SRAM cell is 1.25μM^2, 6T SRAM is 1.079μM^2 and that of 8T SRAM is 1.28μM^2all the results are simulated in cadence virtuoso using 18nm technology.

1. Introduction

The present day 5G networks require high data rate for transmission of signal which consumes a lot of power, even the 5G network introduces IOT concept through which all the devices are connected with mobile networks.Inorder to achieve this wireless sensor networks are used which are low power consuming and cost effective and also in miniature size. For the data transmission in such a way wireless sensor networks are established by spacing all the networks close to each other in large numbers. These networks have to work with low power consumption for which routing protocols are built which uses SRAM for data storage. [1]

SRAMs are an important embedded part of the memory in any portable device. The SRAMs have become an integral part of the present-day memories as the device size is decreasing. Specifically, in biomedical applications like wireless body area networks, the low power SRAMs are an emerging trend. Since it is required to have low power devices reduction in power is the main criterion for any kind of VLSI device and it can be done by reducing the size and also the supply voltages. There appears to be not at all feasible alternatives of remaining out using the conventional MOSFET with down scaling from 65nm to 45nm or further smaller nodes. Rigorous Short Channel Effects (SCE) like Drain Induced Barrier Lowering (DIBL), Vth roll off, rising leakage currents like sub-threshold S/D leakage, hot carrier effects and gate direct tunneling leakage that effect in device performance degradation are afflicting the industry [2].

Dropping the V_{DD} helps decrease hot carrier effects and power however deteriorates the performance, which can be enhanced by dropping Vth but it degrades Source/Drain leakage. To rise suitable channel control by the gate and decline DIBL, the oxide width can be reduced but this augments the gate leakage. Resolving one problem directs to another. The improving of high gate dielectric to lessen the gate leakage and sufficient channel control is to be found out. But unfortunately, this investigation has not been successful to be used. There are problems with the band alignment (w.r.t Si) and/or interface states (with Si) and/or thermal instability. The current uncertainty crisis has led the scientists to search for metal gate conductors instead of poly-silicon. But metal gates conductors with opposed work resolutions haven‘t

been initiated to be practical. Under this situation, poly-silicon remains to be used, where the work utility stresses that Vth be sited by high channel doping. This in turn leads to random dopant fluctuations (at small gate lengths) along with increased impurity scattering and ultimately condensed mobility. Definitely, it is felt that as a substitute of planar MOSFETs.The alternate way is to use a FinFET device when the technology is scaled beyond 65nm to have reduced leakage currents and remove short channel effect [3].

The most used conventional 6T SRAM cell has few drawbacks, to overcome these drawbacks different number of transistor SRAMs are proposed which reduce the problems of the conventional SRAM. The SRAMs with different transistor topologies reduce the bit interleaving problems and stability problems and power consumption problems up to a certain extent, still as the number of transistors are increasing the area of the design will increase which is another parameter to be considered. Keeping in view all the constraints a 7T SRAM is a better design to address the problems that a conventional design has, this is because the 7T SRAM has only one extra transistor which actually providing better stability to the design and also managing the power consumption by switching off the unused transistors [4]

2. Finfet Based 6t Sram Cell

Optimization of FinFET is required for better stability and condensed power feeding. This can be achieved by varying the supply, H_{fin} and also varying the threshold voltages. However, reducing the supply voltage (V_{DD}) below parametric variations has a robust harmful effect on the SRAM cell stability. Memories are essential to have low power dissipation and short access times, therefore FinFET based SRAM cells are used. The FinFET devices are having low power dissipation [5] so the SRAM with FinFET has different functionality unlike the conventional SRAM here as shown in Fig. 1 the SRAM has N3, N4 access transistors which have to be always ON for read and write process since they are the connectivity between the cross-coupled transistors acting as inverters and the Word, Bit and Bit_b line [6–7].

SRAM OPERATION

SRAM has three different modes of operations read, write and hold. The SRAM cell must have better performance to operate in read and write mode [8].

Read Operation

In this operation takes place only by using single transistor pair the read process takes place when both bit line and bit_b line are set and by setting P2 ON and N2 OFF the data falls and it rises when the condition is vice versa. This process takes place when word line is maintained by the access transistors N3 and N4.

Write Operation

In this the data is supplied to the bit line and bit_b, subject to the data to be written both the lines are assigned with data which is opposite in nature. The word line is then triggered so that the data written is stored. The write operation can be benefited by increasing the number of fingers of the FinFET, but not in all cases. [9–10].

Hold Operation

In this state there is no connectivity between the word line, bit line and bit_b with the cross-coupled devices as the transistors N3 and N4 are the OFF-inverter transistors support each other to maintain the data as long as possible [11–13].

3. Leakage Currents In 7t Sram

The fundamental goal of proposing the 7T SRAM cell is to device abundant Read Steadiness and SNMs. The proposed 7T SRAM cell is presented in Fig. 2. Here in the proposed design, it consists of 7 transistors of which 4 Transistors work similar to the conventional device but the remaining transistor controls the device in such a way that during read mode N4 and N5 will be On and N3 will be OFF and During Write mode N5 will be OFF, thus reducing the power consumption. [14–15]

As 7T SRAM Cell utilizes just a single BL, in any mode of operation the power depletion is condensed to half of conventional device usage. [16–17]. The 7T SRAM cell has a leakage current of 50.26nA and Power dissipation of 35.22nW which can be seen in the Figs. 3(a) and 3(b) respectively.

The subthreshold leakage current of N type and P type FinFET devices is simulated and it is found to be 2.84pA and 2.04pA respectively and is shown in Figs. 4(a) and 4(b).

3.1 Techniques for reducing Leakage in 7T SRAM Cell

High-performance circuits design paths are prevented by high power dissipation. Since battery stores, an amount of energy and circuit designers require minimizing the power dissipation. In 7T based SRAM cell a single bit line will have low power consumption because of its functionality when it is compared with a 6T based SRAM and few other SRAMs. Still, the power consumption can be further decreased by reducing the leakage currents. In order to decrease the leakage currents, many techniques have been suggested like [18]

- Multi-threshold CMOS (MTCMOS) Technique
- Adaptive Voltage Level Technique (AVL)
- Drowsy-Cache Technique
- Proposed Self-Controllable Voltage Level Technique (SVL)

Multi-threshold CMOS (MTCMOS) Technique

In CMOS-based chip technology, its variation represents the multi-threshold that consists of transistors with dual-threshold voltage (Vth) for optimizing the power and delay. In MOSFET transistor multiple threshold voltage is the voltage at the gate terminal at which this formation of an inversion layer at an interface between body and oxide layer. Hence devices with lower threshold voltage will switch fast and also minimize clock periods on critical delay paths. The disadvantage of a lower threshold voltage device is that it has a high leakage power. Therefore to overcome this limitation of leakage a higher threshold voltage device is used that has a less static power. Typically by using a higher threshold voltage device static leakage is reduced 10 times when compared to lower threshold voltage devices. [19].

In the multi-threshold CMOS technique, lower threshold voltage transistors are detached from the source by sleep transistor having a higher threshold voltage that is present at the top and bottom of the circuit. Figure 5 Illustrates a transistor that has a lower threshold voltage used for logic design. The sleep signal controls a sleep transistor. When the transistor is in active mode, a sleep signal will be distorted and results in switching ON the higher threshold voltage transistor and will supply power virtually and GND to the lower threshold voltage. When the designed circuit becomes inactive, a step signal will be asserted and force the transistor having the higher threshold voltage to move in a cutoff region that will disconnect its power to lower threshold voltage. It causes a lower current at the threshold region from power towards the GND.

Adaptive Voltage Level Technique (AVL)

Adaptive Voltage Level based technique is another approach for minimizing a leakage current and leakage power on a shorted gate DG FinFET SRAM cell. As seen in Fig. 6, an approach is to combine the technique of adaptive voltage level scaling done at supply voltage for reducing the supply provided to a circuit in static mode and Adaptive voltage level scaling done at the ground when the circuit is at inactive mode. [20] By a reduction in power source and an growth in ground potential, a reduction in leakage power is achieved. In AVLS, during active mode, we apply a full voltage supply i.e., VDD to the SRAM cell. Whereas, during the inactive mode, we apply a reduced amount of supply voltage. This consequences in leakage current decrease by the access transistors that makes bit lines to float. In AVLG, increased voltage is provided during the standby mode while, during the active mode, a 0V is provided at the GND mode. [21].

Here above scheme is related to the diode cache scheme that is used to regulate the SRAM leakages, and here the design has a diode that has a higher threshold transistor for increasing the ground level to reserve mode.

Drowsy-Cache Technique

In this method we apply a lower supply voltage to SRAM cell during hold operation. For present memory we use dual supply voltages. When transistor is in active mode we apply a higher supply voltage for read/write operations. Since by decreasing VDD there will be decrease in leakage current, and lower VDD will be used. In case of standby mode and higher supply voltage for reducing the SRAM leakage [22].

Hence simultaneous reduction of leakages will decrease the leakage power quadratic ally and there will be improvement in performance of designed circuit. Waveform of leakage current implemented by DCT is shown below in figure.7

Proposed Self-Controllable Voltage Level Technique (SVL)

Various methods are used for reducing the power and to maintain the device performance at high speed. A self-controllable voltage level design circuit is used for declining the power and for refining the device performance. Here we generate a minimum or maximum voltage supply, and minimum or maximum ground voltage for increasing the speed of operation. When there is a switching among standby mode and active mode here the circuit has three levels of design such as lower SVL, upper SVL and a mixture of both lower and upper SVL [23–24].

As shown in Fig. 8 the design consists of transistors N6, P3 and P4 linked in series amongst the 7T SRAM and the ground and these transistors are controlled by a control signal CSB which actually maintains a virtual ground when the device is in idle mode. And similarly the transistors P5, N7 and N8 operated with CSB provide V_{DD} when the device is in idle mode and maintains the transistors in 7T SRAM such that the subthreshold leakage through transistorsP1 and N1 is reduced.

4. Results Discussion Of The Proposed Design

The different leakage reduction techniques such as MTCMOS, AVL, and Drowsy–cache and the proposed SVL are implemented and the leakage current and leakage power are calculated for the proposed design of 7T SRAM, the simulation graphs are shown in Fig. 9,10,11,12 respectively. Using MTCMOS technique the leakage current is reduced by 75.9%, with AVL technique the leakage current is reduced by 77.5%, by using Drowsy-cache technique the leakage current is reduced by 82.6% and it is found that the SVL technique provides the better performance than the other techniques where it has reduced the leakage current by 84.9% when compared with the leakage currents of the 7T SRAM without applying any leakage reduction technique.

The proposed technique of SVL is also implemented for other 6T, 7T, 8T, 9T, 10T, 12T SRAMs and found to have better power dissipation and leakage current. All the results were implemented with 18nm FinFET technology. Table 1 and Table 2 give the comparison of leakage current and power for different transistor topologies with leakage reduction techniques. Table 3 shows the power consumption and power dissipation proposed 7T SRAM and other published works.

Table 1
Comparison of Leakage current and leakage power of 7T SRAM with different techniques

Leakage reduction Techniques	Leakage Current Without technique	Leakage current with technique	Leakage Power Without Technique	Leakage Power With Technique
MTCMOS	50.26nA	12.1nA	35.22nW	8.47nW
AVL		11.3nA		7.91nW
Drowsy-cache		8.7nA		6.12nW
SVL		7.58nA		5.31nW

Table 2
Comparison of the leakage power and leakage current with proposed SVL technique applied to different transistor SRAM

SRAM Cells	Leakage Current Without technique (nA)	Leakage current with leakage reduction technique (nA)	Leakage Power Without leakage reduction technique (nW)	Leakage Power With leakage reduction Technique (nW)
6T	51.31	9.78	35.91	6.85
8T	52.63	9.72	36.84	6.81
9T	52.87	9.88	37.1	6.92
10T	53.32	9.22	37.32	6.46
12T	54.12	9.01	37.88	6.31

Figure 13 shows the total power consumption of the 7T SRAM cell with SVL technique where it is found that the total power consumed by the circuit is 7.52 nW which is 36.8% less than the power consumed by 7T SRAM without using SVL technique where it is 11.9 nW.

Table 3
Comparison of 7T SRAM with other Published Papers

OFF-State Leakage Power of 7T SRAM cell				Total Power Consumption (ON + OFF state Power consumption)	
Ensan et.al [25]	Kushwah et.al [26]	Vandana et.al [27]	Proposed 7T SRAM	Proposed 7T SRAM without technique	Proposed 7T SRAM with technique
69.1nW	26.63nW	20.95nW	5.3nW	11.9nW	7.52nW

Cell Area and Layout

The two most significant properties of a memory collection are its functionality and density. Functionality is certain for bulky memory groupings provided that adequately enormous design limitations, which are decided by the supply voltage, device sizing and slightly, by the assortment of transistor threshold voltages. Even though upsizing the transistors upsurges the noise limits, it surges the cell area thus sinking the density.

Here the layout of 7T, 6T, 8T SRAM with the final design along with the leakage reduction circuit is drawn using cadence virtuoso layout editor and DRC check is done. The layouts are shown in Figs. 14(a), 14(b), 14(c) respectively. The area is calculated according to the design rules where the area of 6T SRAM is 1.079 μM ^{2,} area of 7T SRAM cell is 1.25 μM^2 and the area of 8T SRAM cell is 1.28 μM^2 as shown in Table 4.

Table 4: Area of SRAM cells

S.No	SRAM	Area(μM^2)
1	6T	0.83*1.3
2	7T	0.83*1.51
3	8T	0.83*1.55

5. Conclusion

In this paper, the leakage reduction techniques have been applied to the proposed 7T SRAM cell and it is set up that by relating the SVL technique the leakage current is reduced by 84.9% in comparison to the 7T SRAM without applying the technique .whereas by applying MTCMOS method it is detected that leakage current is reduced by 75.9% by using AVL technique the leakage current by 77.5% and another technique drowsy cache has brought down the leakage current by 82.6% in comparison to 7T SRAM based on FinFET without applying the technique. It is evident that of all the techniques SVL technique is better. Then the same SVL technique is applied to the SRAM cells with other transistor topologies where it is found that the 6T SRAM has 80.9% reduction, 8T SRAM has 51.5% reduction, 9T SRAM has 81.3% reduction, 10T SRAM has 82.75% reduction and the 12 T SRAM has 83.3% reduction in leakage current compared to their designs without technique. The 7T SRAM cell has the least leakage power of 5.3nW which and total power consumption of 7.52nW which makes it the preferred SRAM of all the compared circuits.

Declarations

Funding

There is no funding received for this work.

Conflicts of interest/Competing interests

There is no conflict of interest at any stage.

Availability of data and material

The associated data will be made available on request.

Code availability

The simulation work has been carried out Cadence virtuso

Authors' contributions (optional): NA

Additional declarations

Ethics approval: NA

It is a simulation-based design and analysis. So, it does not produce any environmental hazards.

Consent to participate

Yes, we are ready to participate.

Consent for publication

We are ready for publication with your journal.

Acknowledgement

We acknowledge for the support and lab facility provided by department of VLSI design , School of Electronics and Electrical Engineering, Lovely Professional University, Punjab India.

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Figures

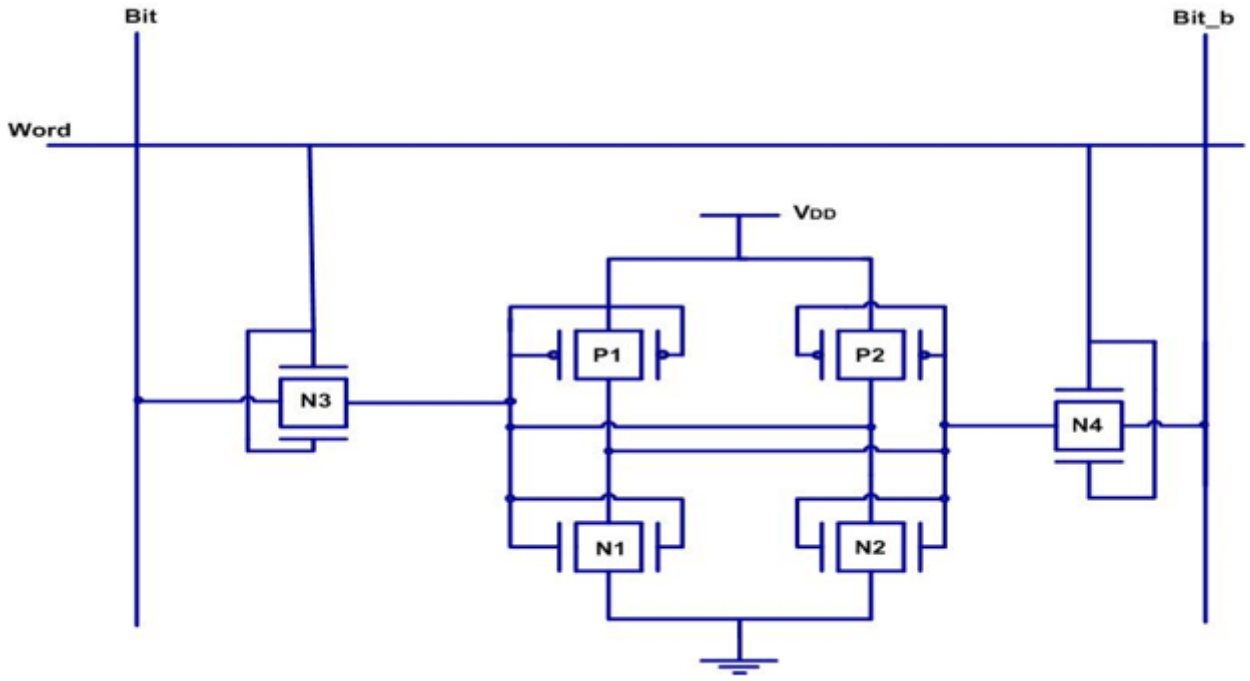

Figure 1

FinFET based 6T SRAM

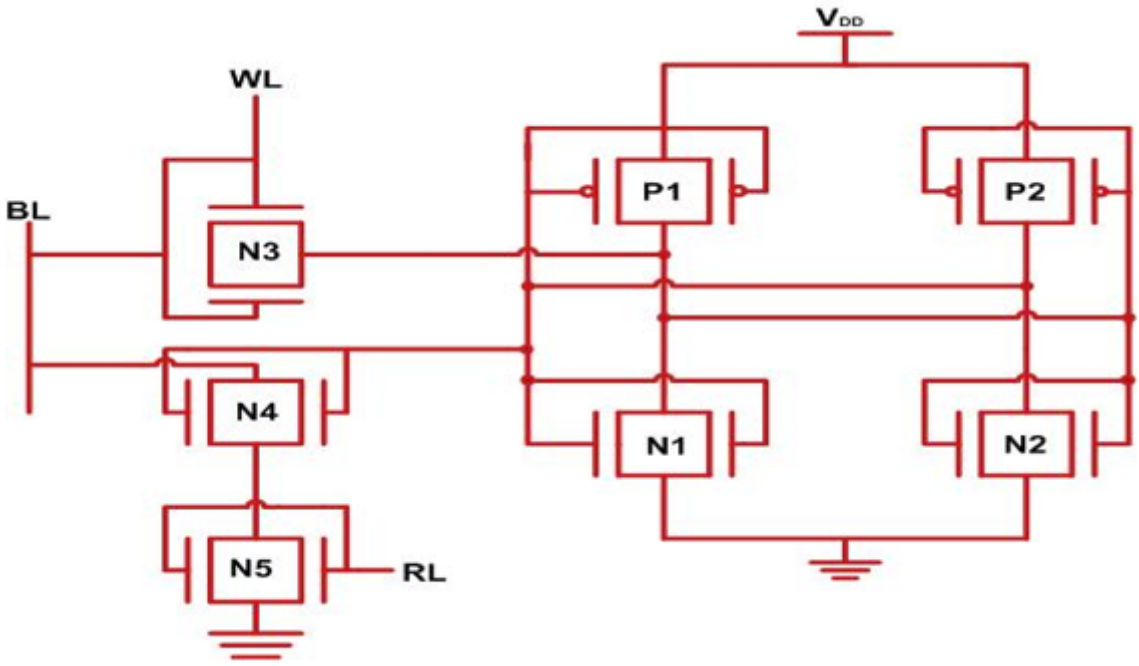

Figure 2

FinFET based 7T SRAM

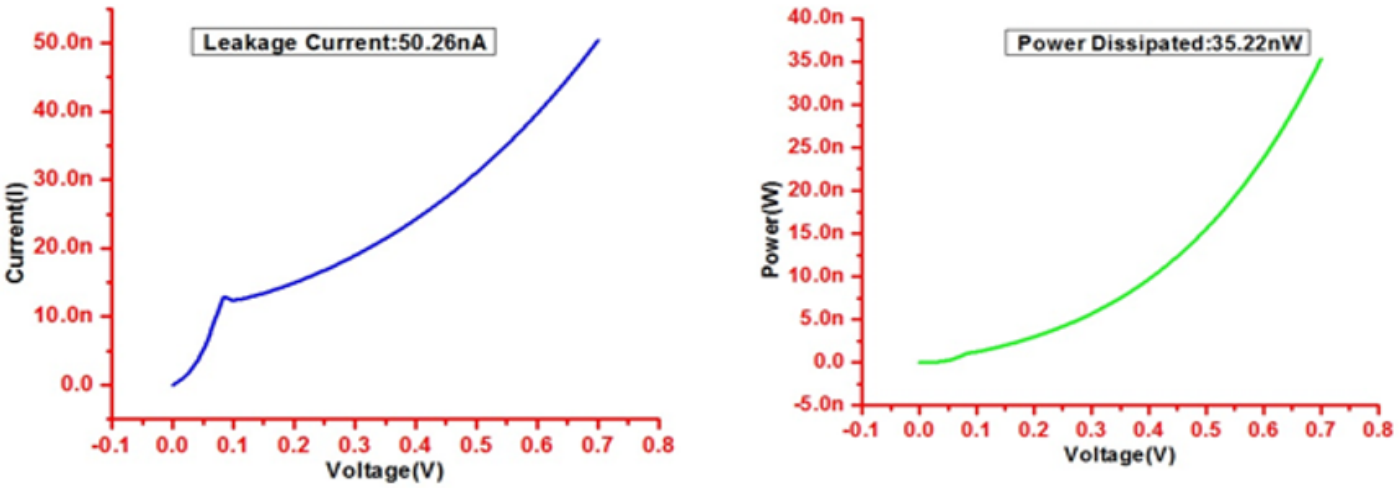

Figure 3

(a) Leakage Current of 7T SRAM, (b) Leakage Power of 7T SRAM

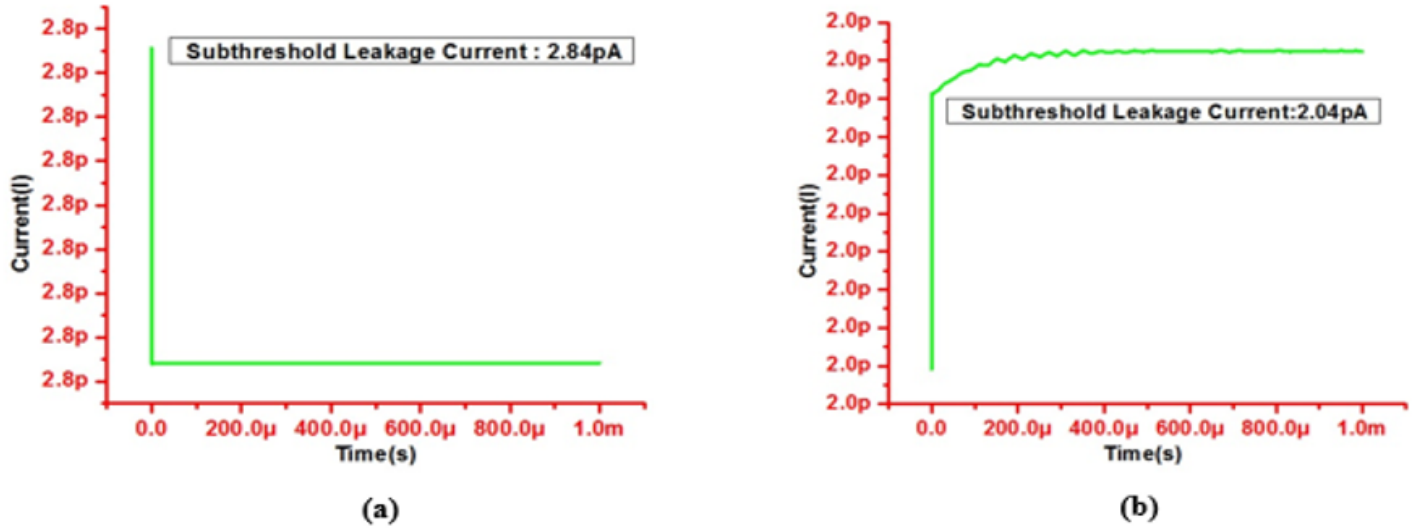

Figure 4

Subthreshold Leakage Current of (a) N-Type FinFET (b) P Type FinFET

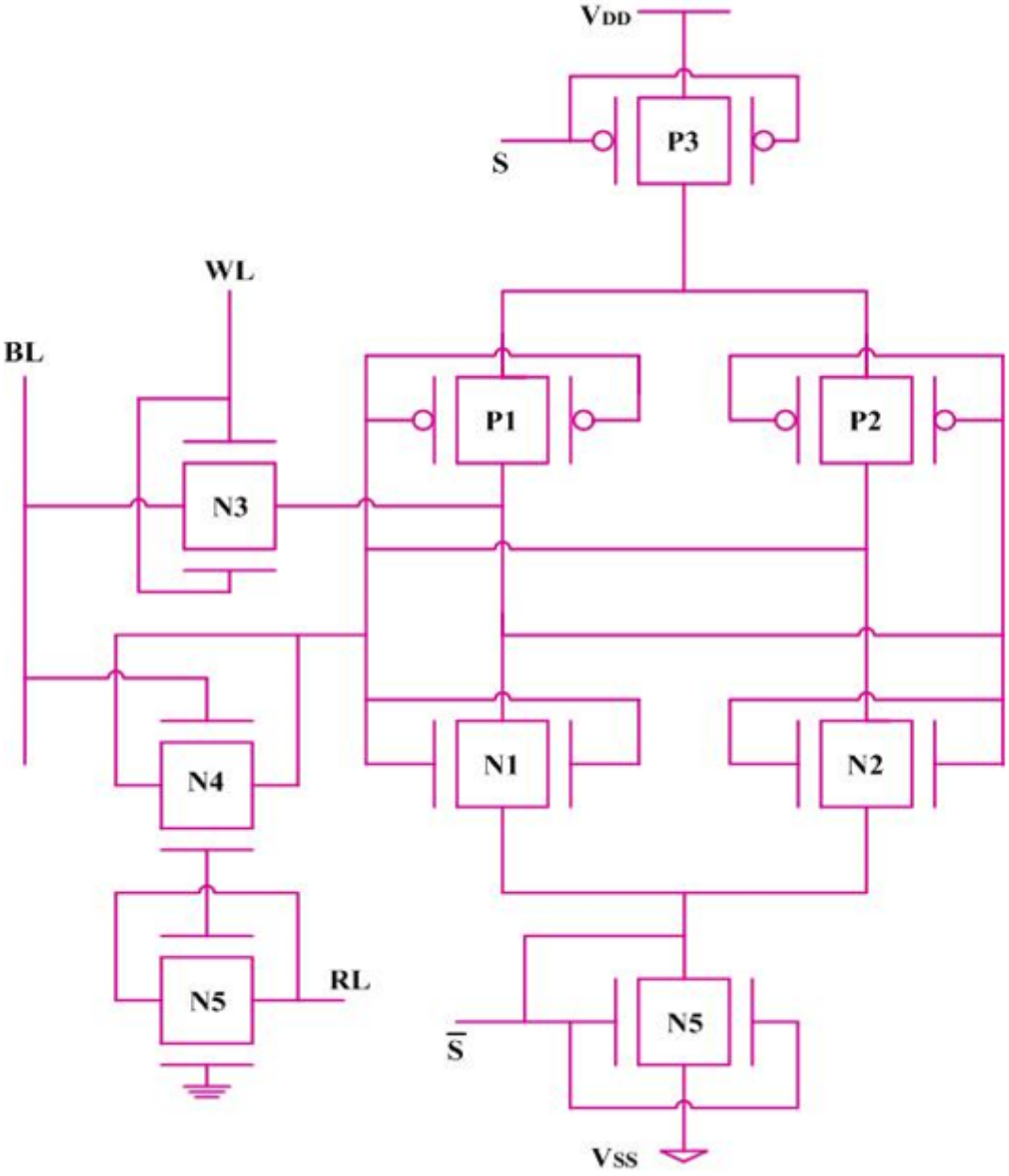

Figure 5

7T SRAM with MTCMOS Technique

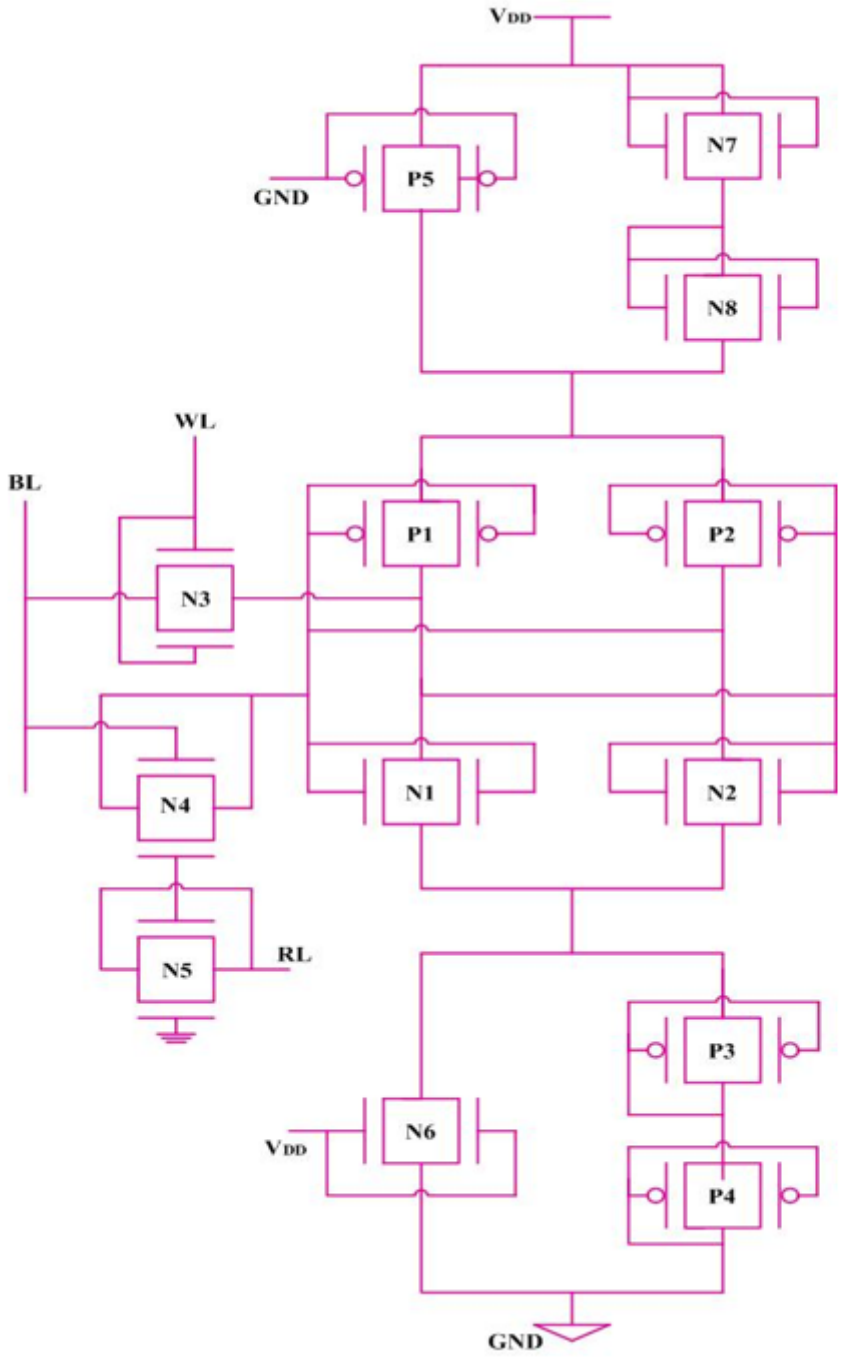

Figure 6

7T SRAM with AVL technique

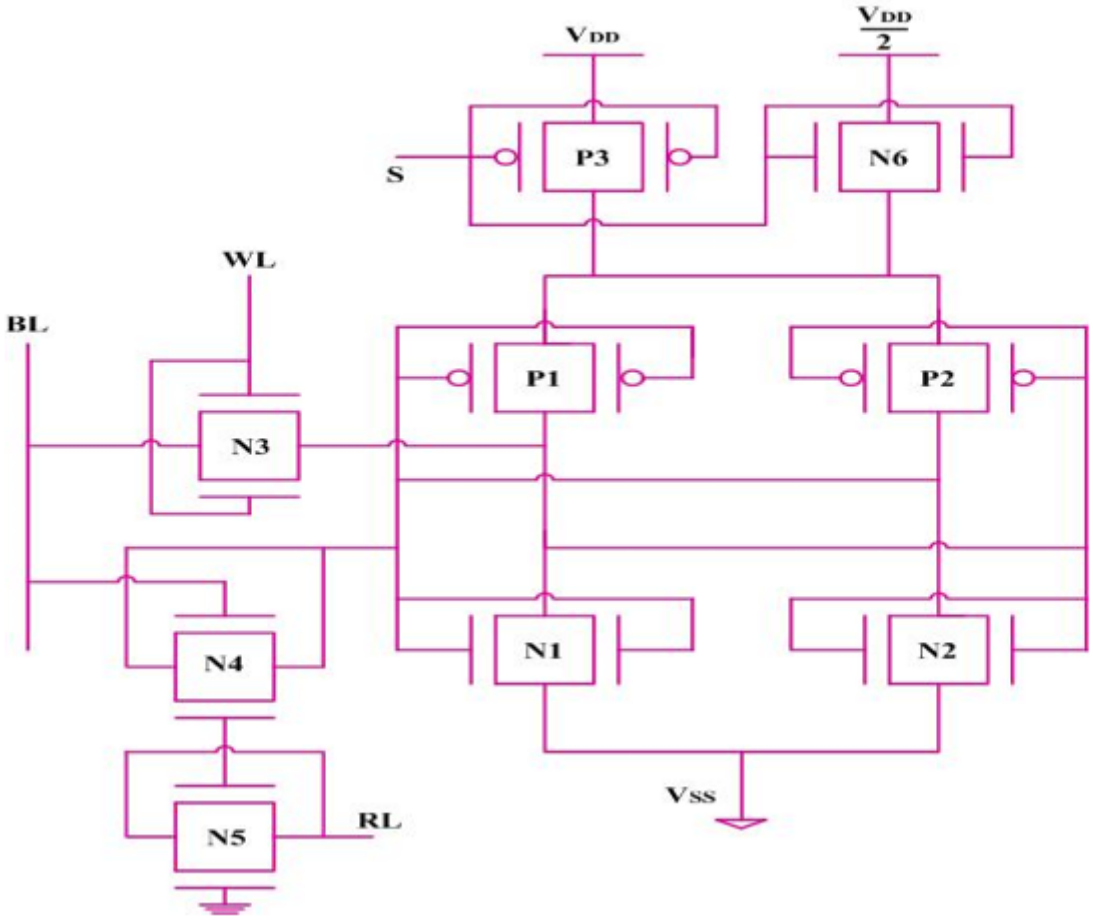

Figure 7

7T SRAM in Drowsy-Cache Technique

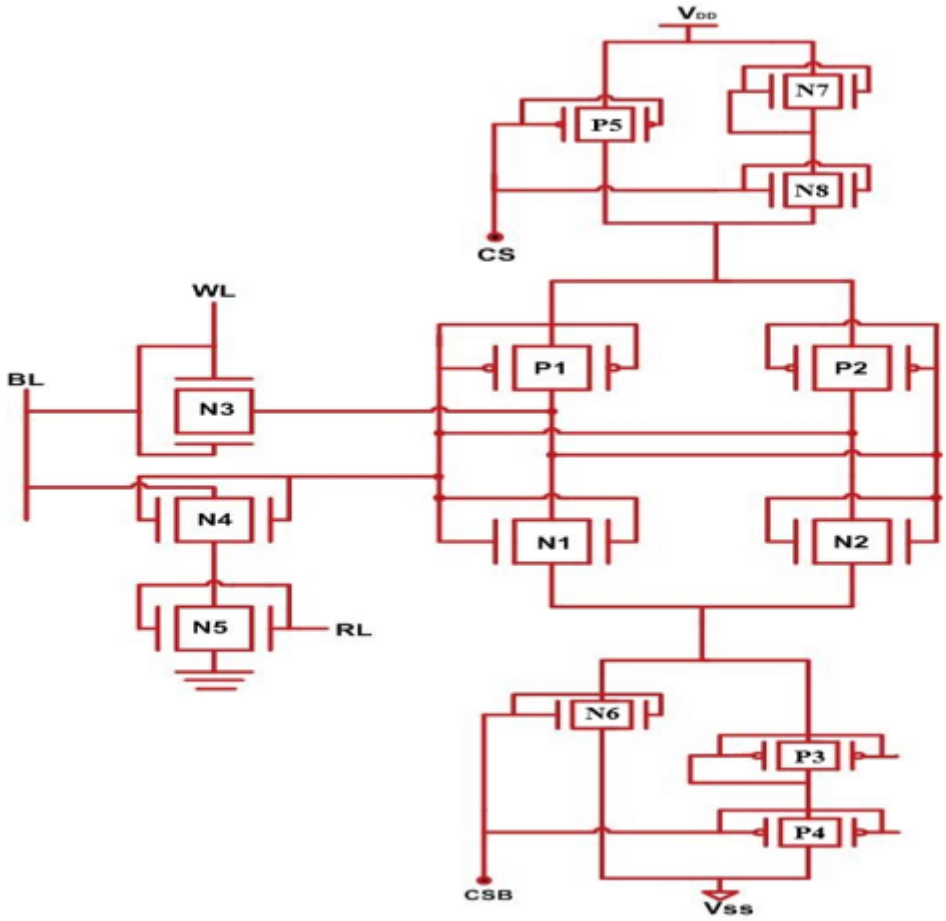

Figure 8

7T SRAM with SVL Technique

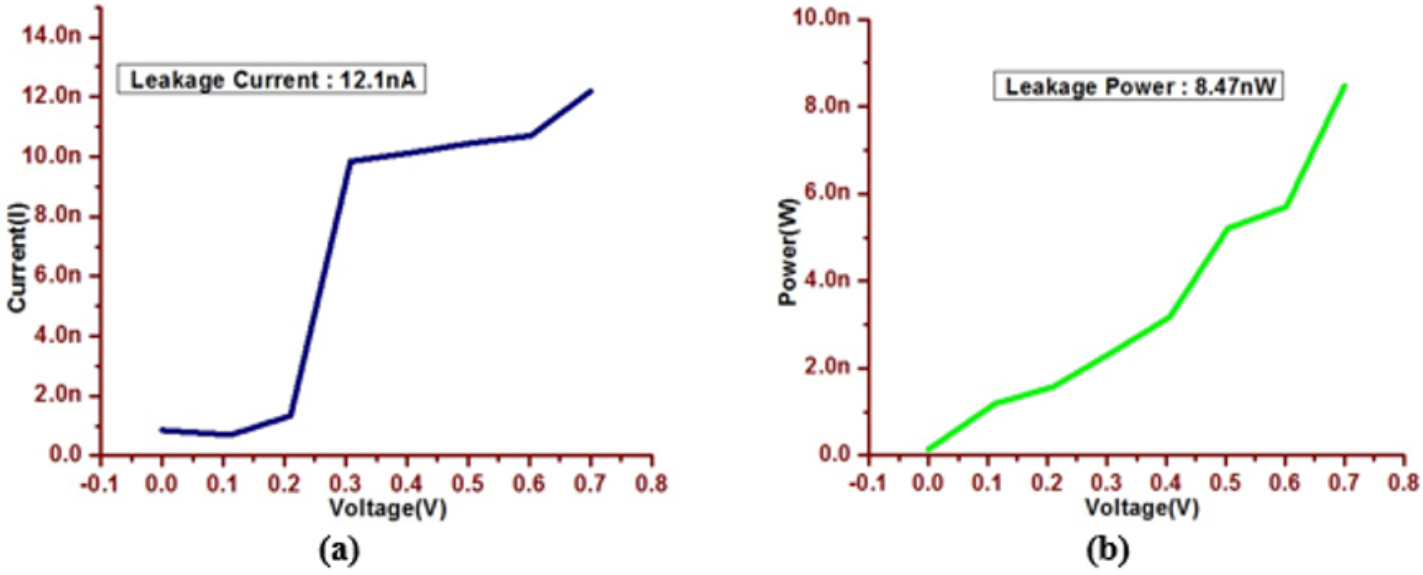

Figure 9

7T SRAM with MTCMOS Technique (a) Leakage Current (b) Leakage Power

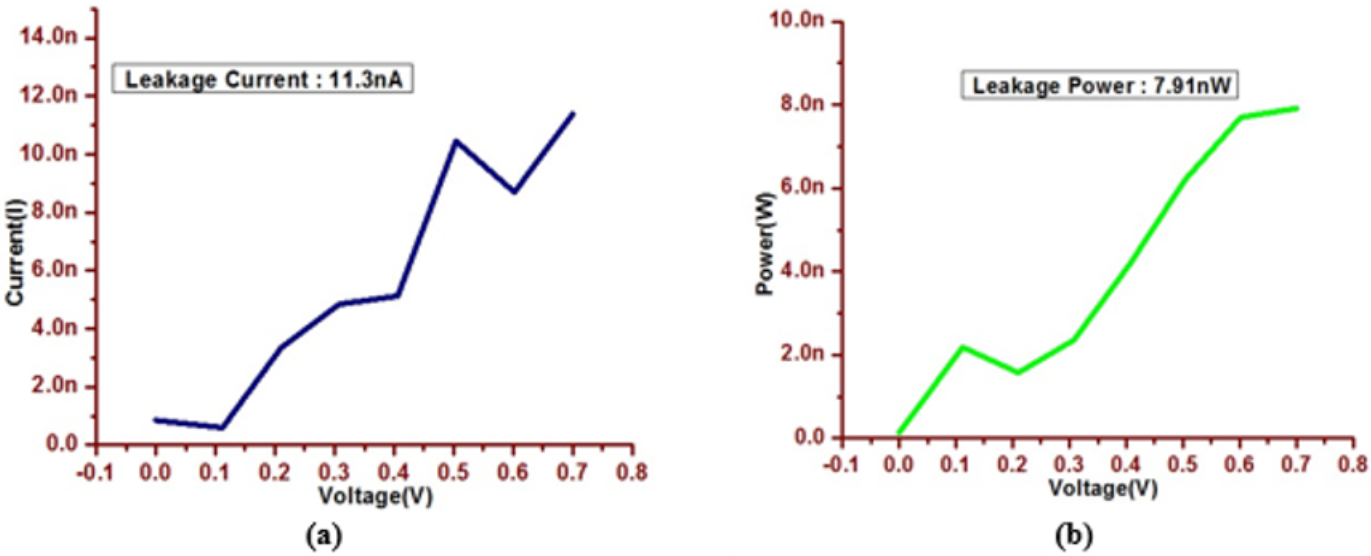

Figure 10

7T SRAM using AVL Technique (a)Leakage Current (b)Leakage Power

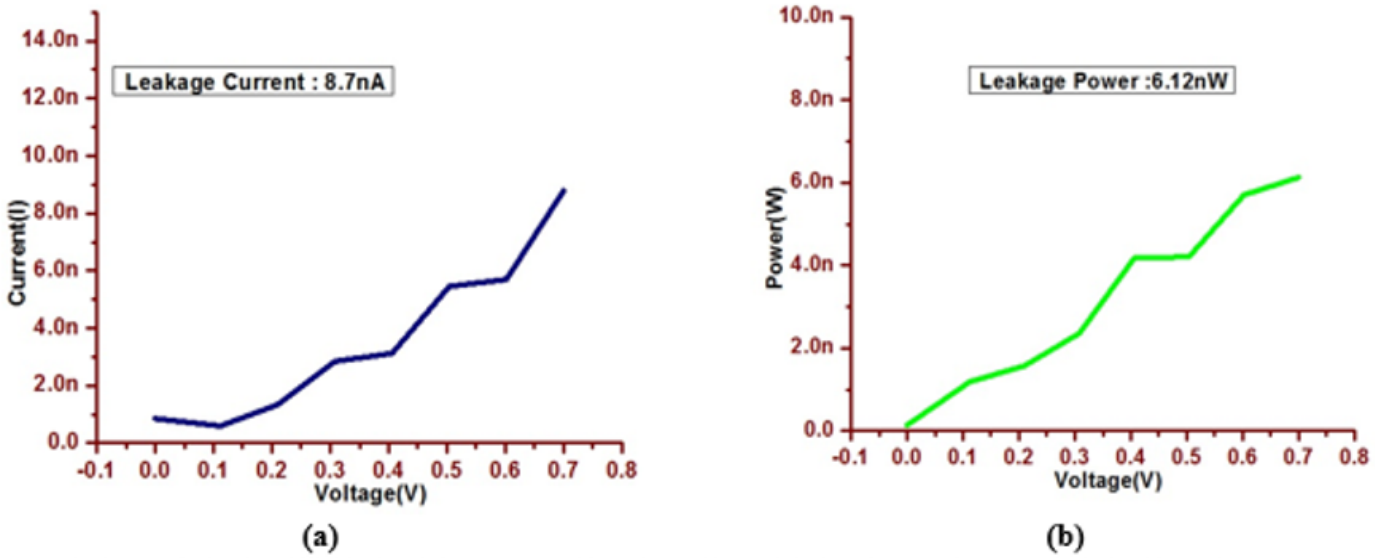

Figure 11

7T SRAM with Drowsy cache Technique (a)Leakage Current (b)Leakage Power

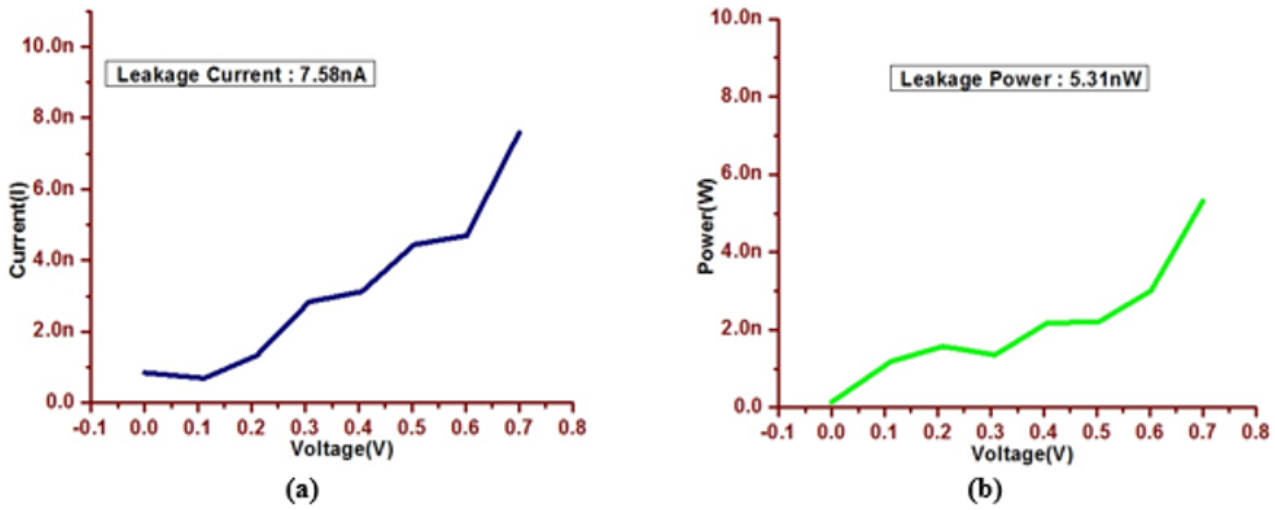

Figure 12

7T SRAM using SVL Technique (a)Leakage Current (b)Leakage Power

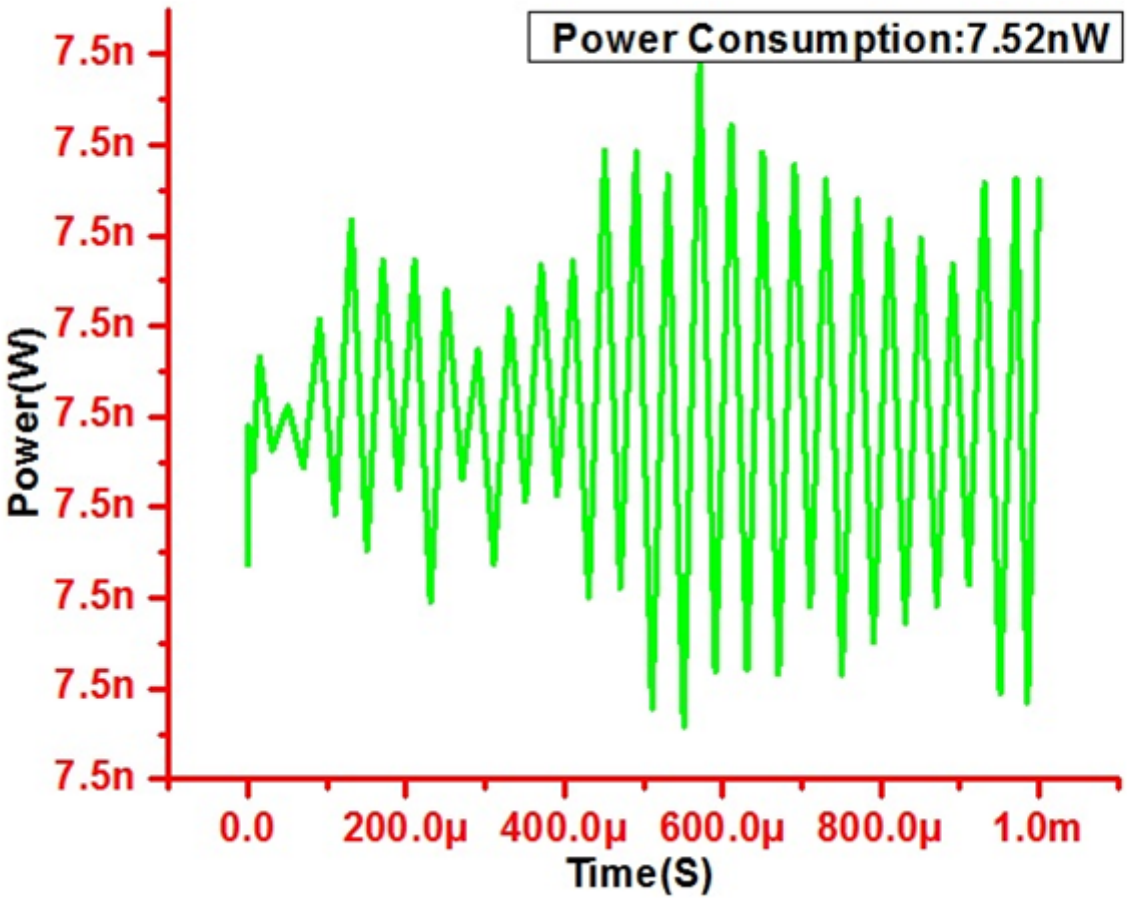

Figure 13

Total Power Consumption of 7T SRAM cell

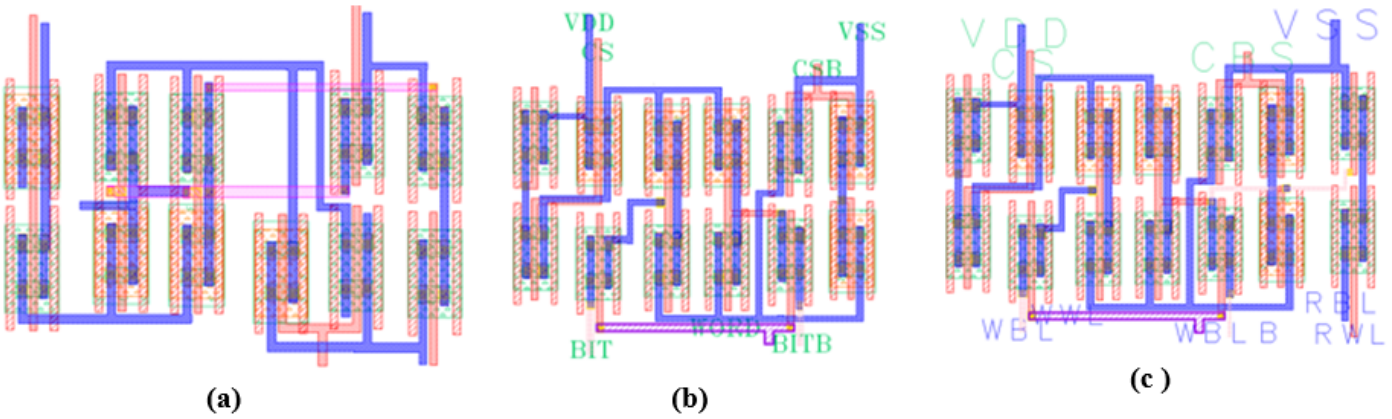

Figure 14

Layout of (a) Proposed 7T SRAM Cell (b)6T SRAM (c) 8T SRAM