Study of Analog/Rf and Stability Investigation of Surrounded Gate Junctionless Graded Channel MOSFET(SJLGC MOSFET)

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Research Article

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Study of Analog/Rf and Stability investigation of Surrounded gate Junctionless Graded Channel MOSFET(SJLGC MOSFET)

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Abstract: This paper explores the potential advantage of surrounded gate junctionless graded channel (SJLGC) MOSFET in the view of its Analog, RF performances using ATLAS TCAD device simulator. The impact of graded channel in the lateral direction on the potential, electric field, and velocity of carriers, energy band along the channel is investigated systematically. The present work mainly emphasises on the superior performance of SJLGC MOSFET by showing higher drain current (I_D) , transconductance (g_m) ,cut off frequency (f_T) , maximum frequency of oscillation (f_{max}) , critical frequency (f_K) .The drain current is improved by 10.03 % in SJLGC MOSFET due to the impact of grading the channel. There is an improvement in f_T, f_{max}, f_K by 45%, 29% and 18% respectively in SJLGC MOSFET showing better RF Performance. The dominance of the SJLGC MOSFET over SJL MOSFET is further elucidated by showing 74% improvement in intrinsic voltage gain (g_m / g_{ds}) indicating its better applications in sub threshold region. But the transconductance generation factor of SJLGC MOSFET is less than SJL MOSFET in the subthreshold region. The intrinsic gate delay (ζ_D) of SJLGC MOSFET is less in comparison to SJL MOSFET due to the impact of lower gate to gate capacitance (C_{GG}) suggesting better digital switching applications. The simulation results reveal that SJLGC MOSFET can be a competitive contender for the coming generation of RF circuits covering a broad range of operating frequencies in RF spectrum.

Keywords: Transconductance generation factor, Intrinsic gain, unity gain cut off frequency , maximum frequency of oscillation, critical frequency (f_k), energy band diagram, intrinsic gate delay .

SECTION-I

HIGHLIGHTS

- The proposed device exhibits the potential advantage of having surrounded gate, ,junctionless , graded channel architecture.

- Comparison of center potential, electric field , average velocity ,energy band diagram of surrounded gate junctionless graded channel (SJLGC) MOSFET (SJLGC) with surrounded gate junctionless (SJL) MOSFET .

- Systematic Comparison of Analog/RF performances of SJLGC MOSFET and SJL MOSFET .

INTRODUCTION

The development of metal oxide semiconductor large scale integration is closely associated with the regular downscaling of its basic element i.e. MOSFET from the starting of 1970s. The downsizing of MOSFETs is the ultimate and efficient way to enhance the performance, increase the packaging density, increase the number of functionality in a given chip area, decrease the power consumption if at all the area of the chip is constant [1]. Smaller sized MOSFETs possess electrical characteristics which differ from its bigger size counterpart due to the presence of short channel effects. Hence there is a demand of introducing advanced technologies, novel structures and new materials to fulfil the demand of today's electronic industry and make the MOSFETs suitable for ultra-large-scale integration. Multigate FET (MUGFET) has been proposed in literature where the channel is more electro statically controlled by the gates [2-6]. A junctionless transistor has been proposed in literature as an alternative candidate to overcome the problem associated with thermal budget in the formation of steep S/D junction [7-8].Mobility degradation in heaviliy doped channel of JL MOSFET results in lower ON state current and transconductance [9,10]. JL MOSFET relies on bulk conduction and requires gate metal of higher work function to completely deplete the channel during its off state [11].

In the last decades many researchers have put their effort to bring improvement in the Analog/RF performance of conventional MOSFETs using source/drain end engineering [12, 13] and gate engineering [14, 15] .To mitigate the challenges of SCEs and to achieve high speed performance in wireless RF communications systems, many advanced channel engineered structures have been addressed in literature [16, 17, 18, 19]. Y.Chen et al. had investigated the Analog / RF performance of graded channel junctionless MOSFET having gate length of 30nm [20]. A.Kranti et al. had put their effort in highlighting the analog performances of SOI DG MOSFET by applying asymmetric channel engineering [21]. The lateral grading of channel shows noticeable enhancement in analog performance of the device due to increase in g_m and decrease in drain conductance [22, 23].

Many reports are available in literature dealing with the designing problem of RFIC in analysing the high frequency and noise performance [24, 25]. All though reports are available in literature showing the analog and RF analysis of different CMOS devices [26-31] but a systematic comparison of analog /RF performance analysis in between graded and ungraded channel architecture in surrounded gate junctionless structure is still unexplored.

In this work, we propose Surrounded gate junctionless graded channel (SJLGC) MOSFET as a strong contender for system on chip applications and wireless communication networks. The

novelty in present work lies in the architecture of the proposed device as it takes in to account simultaneously the advantages of three architectures such as junctionless architecture (lower thermal budget, easy of fabrication), surrounded gate (channel is more electro statically controlled by the warping of gates and drain current is optimized), graded channel (reduced short channel effect and improved transconductance). Graded channel design in junctionless surrounded gate architecture has not been investigated till now to the best of our knowledge. The fast growing wireless electronic industry need modern technologies in CMOS devices so that these devices can well be applicable for radio frequency/analog/mixed signal applications.

. The manuscript is planned as under: introduction related to different reports from literature is presented in section-I. We outline the device description and physical models used during the numerical simulations in section II. In section III, IV we compare the static characteristics, Analog / RF performance of the proposed device with the conventional one. Finally conclusion of this comparison is drawn in the section V.

SECTION II

Device Description and Simulation Model

The 3-D and 2-D cross sectional view of our proposed structure are shown in Fig.1. (a) and Fig.1. (b). The device structural parameters, drain and gate supply sources are chosen as per the guidelines ITRS [32]. The source /drain is heavily doped n type region with doping concentration of 10^{19} cm^{-3} for both of the devices. This proposed device has a lateral graded doping distribution profile along the channel in the z -direction.

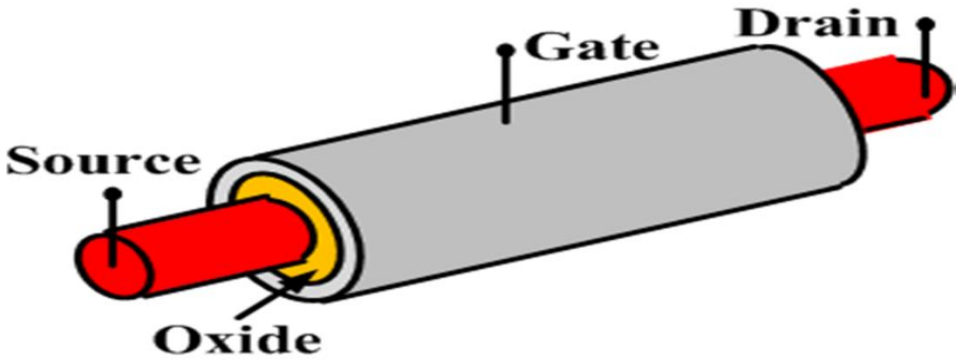

Fig. 1 (a): A 3 Dimensional view of SJLGC MOSFET

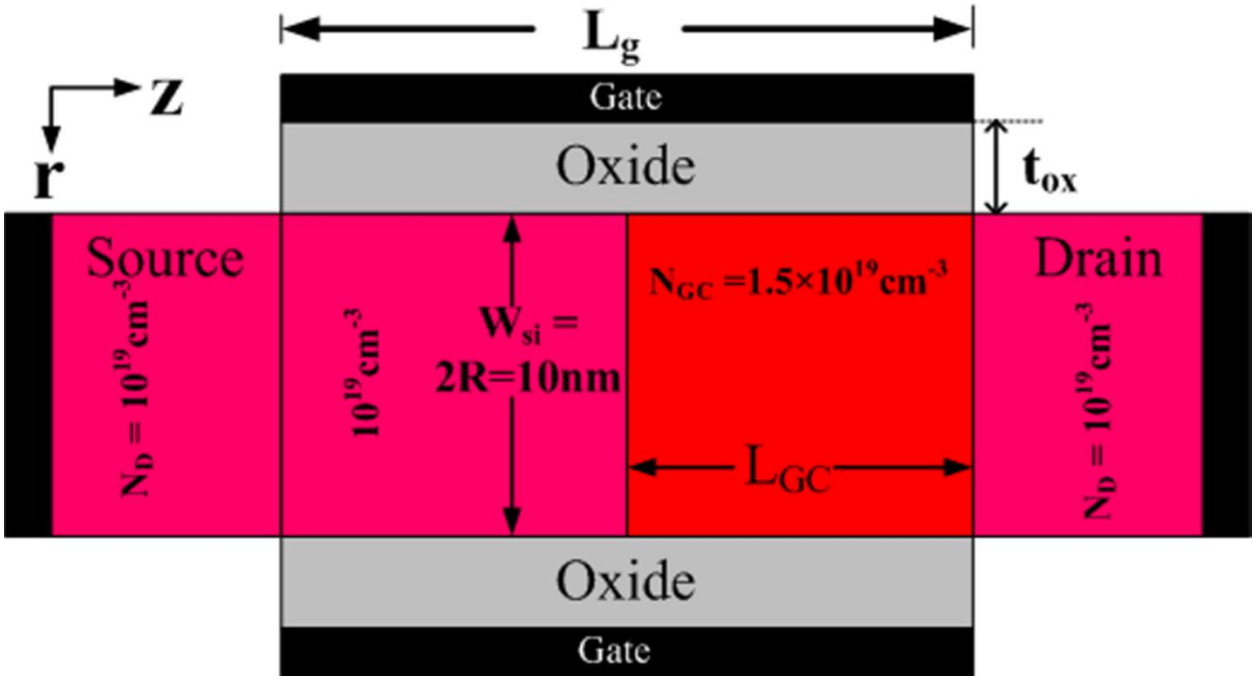

Fig.1 (b) : .Schematic two dimensional view of SJLGC MOSFET.

The entire channel length of SJLGC MOSFET is equally divided into two regions where the region towards the source is doped with same doping concentration as the source region (N_D =$10^{19}cm^{-3}$) and region towards the drain end is heavily doped with a doping concentration(N_{GC}) of 1.5 x $10^{19}cm^{-3}$ having length L_{GC}. The length of graded channel region (L_{GC}) is exactly half of total channel length (L_g) .The SiO_2 is used as the gate oxide material having thickness (t_{OX}) 1nm. The gate length (L_g) in the cylindrical structure is 30nm. The diameter (2R) of the cylindrical Si body is 10nm which is the width (W_{si}) of the Si body. The length of source and drain ($L_{S/D}$) regions are 20nm.The structural dimension of the conventional SJL MOSFET is exactly same as SJLGC MOSFET except the fact that the source, drain, channel are uniformly doped with n type dopant with a doping concentration of $N_D = 10^{19}$ cm^{-3}.In this work, during our simulation we have chosen the optimized value of the graded channel length i.e. $L_{GC} = (L_g / 2)$ [33]. It is the concentration gradient ($G = N_{GC} - N_D$) at the graded channel region which is responsible for improved performance of SJLGC MOSFET supported by the use of optimized value L_{GC}. But higher concentration gradient leads to reliability issues in fabricating the devices in practical scenario [34].

The structural parameters of the devices are summarized in Table-1.

Table -1

DIMENTIONS OF THE STRUCTURAL PARAMETERS OF THE DEVICES.

Parameters	**SJL MOSFET**	**SJLGC MOSFET**

Gate length (L_g)	30nm	30nm
Radius of silicon body (R)	5nm	5nm
Width of silicon body (W_{si})	10nm	10nm
Doping concentration of Source/ Drain	$1x10^{19}$ cm^{-3}	$1x10^{19}$ cm^{-3}
Doping Concentration of channel	$1x10^{19}$ cm^{-3}	$1x10^{19}$ cm^{-3} for 15nm from source side
Length of graded channel (L_{GC})	Channel is not graded	15nm from the centre of the channel
Doping concentration of Graded channel (N_{GC})	Channel is not graded	$1.5x10^{9}$ cm^{-3} for 15nm towards drain side
Thickness of Oxide layer (t_{OX})	1nm	1nm
Work function of polysilicon metal (ϕ_m)	5.0 eV	5.0 Ev

ATLAS TCAD 3-D Device simulator is used for performing simulation in this paper [35]. The current densities for electron and holes in drift-diffusion model are given by

$$\vec{J}_n = \mu_n(n\nabla E_C - 1.5nKT\nabla \ln m_n) + D_n(\nabla_n - n\nabla \ln \gamma_n) \quad (1)$$

$$\vec{J}_p = \mu_p(p\nabla E_V + 1.5pKT\nabla \ln m_p) - D_p(\nabla_p - p\nabla \ln \gamma_p) \quad (2)$$

Where J_P and J_n denote current densities for hole and electrons. μ_n and μ_p are the mobilities of electron and hole. n and p are the electron and hole densities. Fermi statistics constants for electron and holes are denoted by γ_n and γ_p. The spatial effective masses for electron and hole are m_p and m_n. The conduction and valence energy bands are denoted by E_C and E_V. T is the temperature and K is the Boltzmann constants. D_n and D_p are diffusion constants.The models used during our simulations are specified in Table-2 along with their description.

Table-2

SIMULATION MODELS

S.NO	Physical model	Description
1	Carrier transport model	• Drift Diffusion models (DD) is the basic model that considers carrier transportation mechanism in semiconductor devices.
2	Carrier statistics Model	• Boltzmann Transport model. • Conduction band density at 300 K (nc 300),Valence band density at 300 K(nv 300) parameters are defined in the MATERIAL statement and are set at their default values as $2.8x10^{19}$ cm^{-3} and $1.04x10^{19}$ cm^{-3} respectively.

3	Mobility Model	• Lombardi CVT model and Concentration dependent mobility model (CONMOB) are used for inversion layer mobility and low field mobility respectively. • Parallel electric field dependent mobility model (FLDMOB) takes in to account the velocity saturation of carriers in high field. • The parameter β_n in the MOBILITY statement is set at its default value at 2.0 to take in to account the high electric field dependent mobility.. • α_n. fld , θ_n. fld , tnomn . fld parameters are specified in MOBILITY statements to consider the velocity saturation for electron.
4	Recombination Models	• Shockley Read Hall (SRH) and Auger model take in to account the recombination of minority charge carriers with their life time at 1 x 10^7 sec.
5	Bandgap narrowing model	• BGN model is used in the present work as the devices are heavily doped i.e. greater than $10^{18}cm^{-3}$. • bgn.e, bgn.n, bgn.c parameters specified in MATERIAL statements and are set at their default values as 6.92 x 10^{-3} V, 1.3 x 10^{17} cm^3, 0.5 respectively.
6	Impact Ionization and tunnelling model	• Hot carrier performances are not studied in present work, so no such model is considered here.
7	Quantum mechanical model	• No such model is used in the present work to take in to account the quantum mechanical effects as the thickness of the device is greater than 7nm [36].

As the silicon body is heavily doped, a p type polysilicon gate metal having higher work function is used to fully deplete the channel during the off state for both of the device [37]. The threshold voltages of SJLGC MOSFET and SJL MOSFET are at 0.569 Volt and 0.571 Volt respectively as obtained from the result of simulation where p^+ polysilicon is used as the gate metal for both of the devices having work function (ϕ_m) 5.0eV. Hence, we have approximated the threshold voltage of both of the devices at 0.57 Volt for fair comparison of performances between both of the devices. In the present work thickness of the device is 10nm, hence quantum correction is not required[38-42] . To solve the set of differential equations and current density equations of charge carriers, Gummel-Newton numerical iteration techniques are used. For result validation, certain parameters of the physical model of our ATLAS TCAD simulator are calibrated with the results obtained from the experiment [43] for n type Si Nanowire to obtain the transfer characteristics. To validate our results, we have kept the gate length, oxide thickness, width of the device, doping concentration of S / D /Channel are at 1µm, 10 nm, 30 nm , 2 × 10^{19} cm^{-3} respectively as per the experimental data. A close agreement between simulated results and experimental results are observed in Fig.2. Once the matching is done, we have used the same model for our present work to analyse the Analog and RF performances.

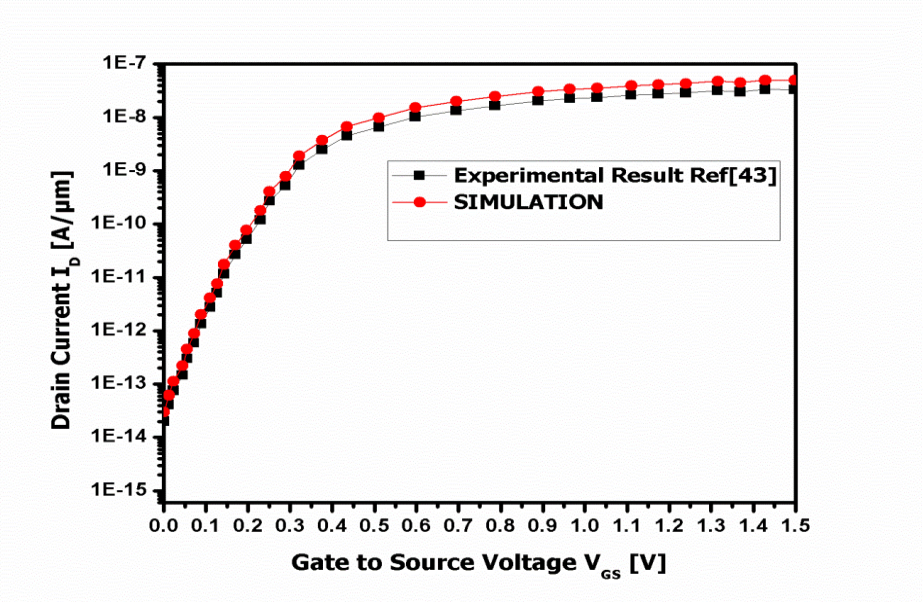

Fig. 2 : Experimental and Simulated plot of I_D v/s V_{GS} in log scale at V_{DS} = 0.05 Volt after calibrating the simulator, showing a fair agreement between experiment and simulation output.

SECTION III

STATIC ANALYSIS

Fig.3. (a) illustrates the transfer characteristics (I_D V_s V_{GS}) of traditional SJL and SJLGC MOSFETs.

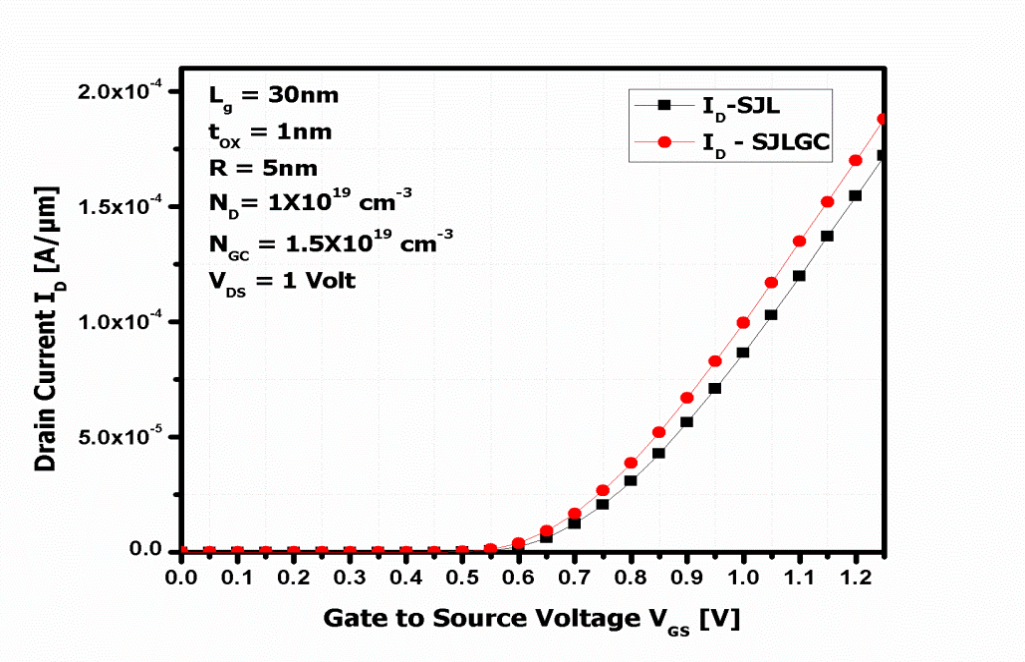

Fig.3 (a) : Transfer characteristics of the proposed SJLGC MOSFET and the conventional SJL MOSFET at ϕ_m = 5.0 eV , Wsi = 10 nm, L_{GC} = 15 nm.

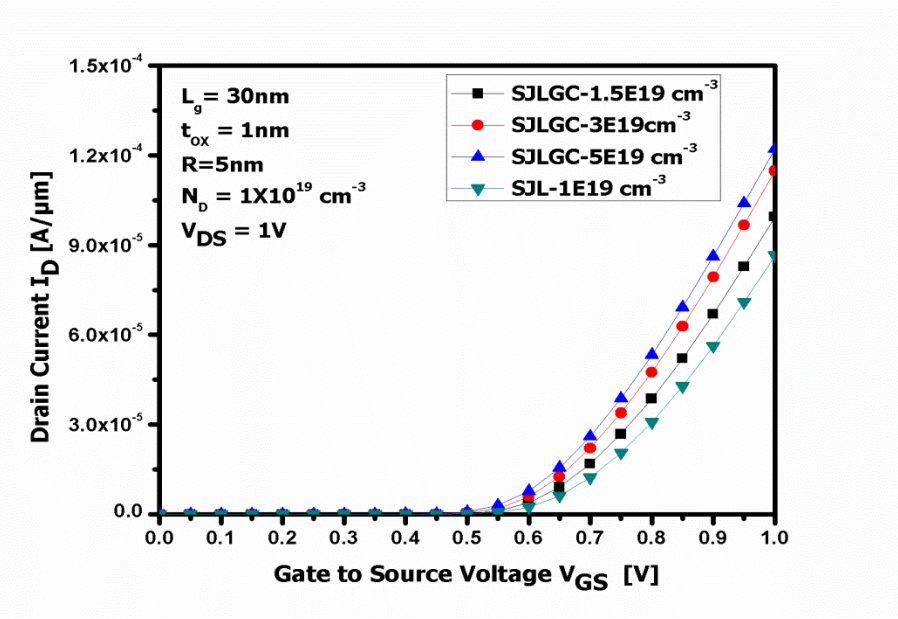

Fig. 3 (b): Transfer characteristics of the proposed SJLGC MOSFET and the conventional SJL MOSFET at ϕ_m= 5.0 eV, W_{si} =10 nm, L_{GC} =15 nm with respect to different doping concentration in the graded channel region.

The enhancement of ON current I_D in SJLGC in comparison to SJL as shown in fig.3 (a) depends on the variation of electron concentration and velocity of electron from source towards drain. Fig. 3(b) illustrates the improvement in drain current in SJLGC MOSFET with respect to increased graded channel doping concentration which is due to the increase in the height of concentration gradient but this increased height of gradient imposes burden in fabrication process

from reliability point of view [37]. The height of concentration gradient increases when the doping concentration of the graded channel region changes from $1.5x10^{19}$ cm^{-3} to $5x10^{19}$ cm^{-3} , resulting in 22.72% enhancement in drain current as shown in fig.3 (b).

To clarify the reason in the increase of I_D in SJLGC MOSFET, we have plotted the potential, electric field, velocity of electron, energy band along the channel in figures (4-6) for both of the devices for their fair comparison. These graphs are plotted by taking cut lines at Wsi / 2.

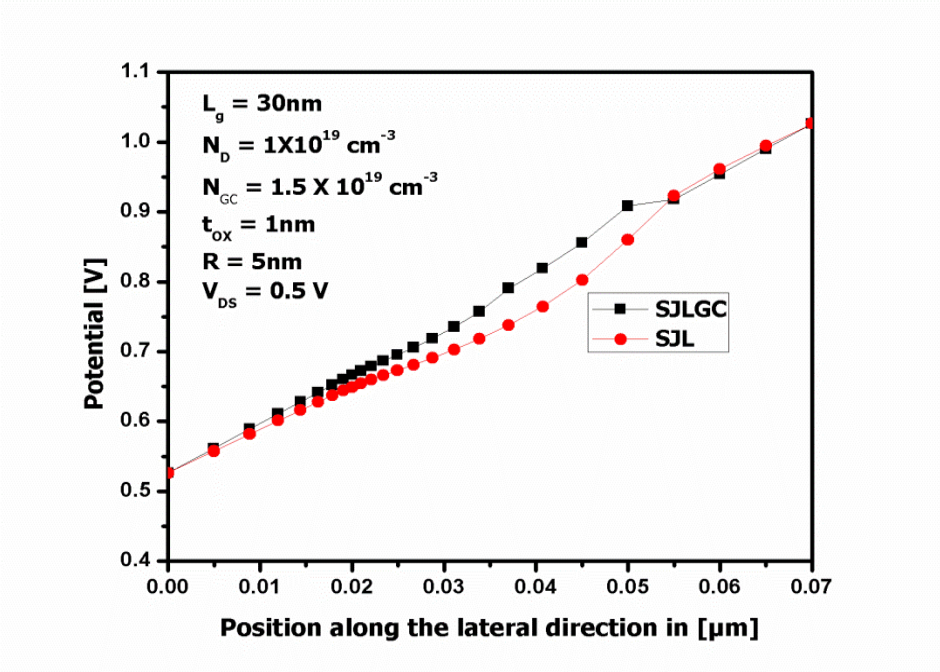

Fig.4 : Potential along the channel in the lateral (z) direction at V_{GS} = 1.0 V, $L_{S/D}$ = 20 nm, L_{GC} = 15 nm, ϕ_m= 5.0 eV for SJLGC and SJL MOSFETs . The channel is located from x = 0.020 µm to x = 0.050 µm.

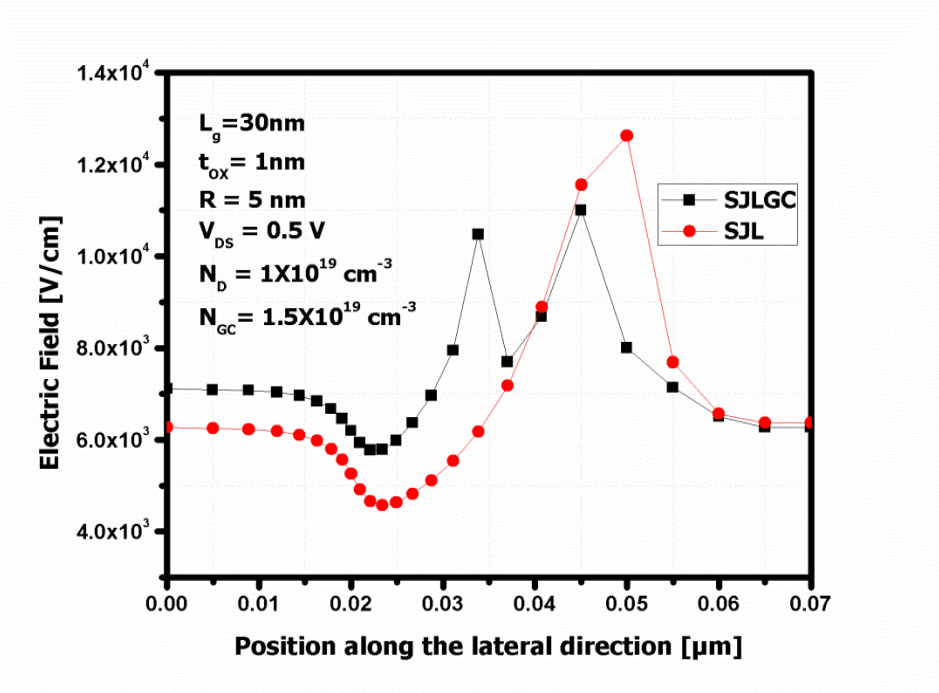

Fig.5 (a) : Electric field along the channel in the lateral (z) direction at V_{GS} = 1.0 V, $L_{S/D}$ = 20 nm, L_{GC} = 30 nm, ϕ_m= 5.0 eV for SJLGC and SJL MOSFETs . The channel is located from x = 0.020 μm to x = 0.050 μm.

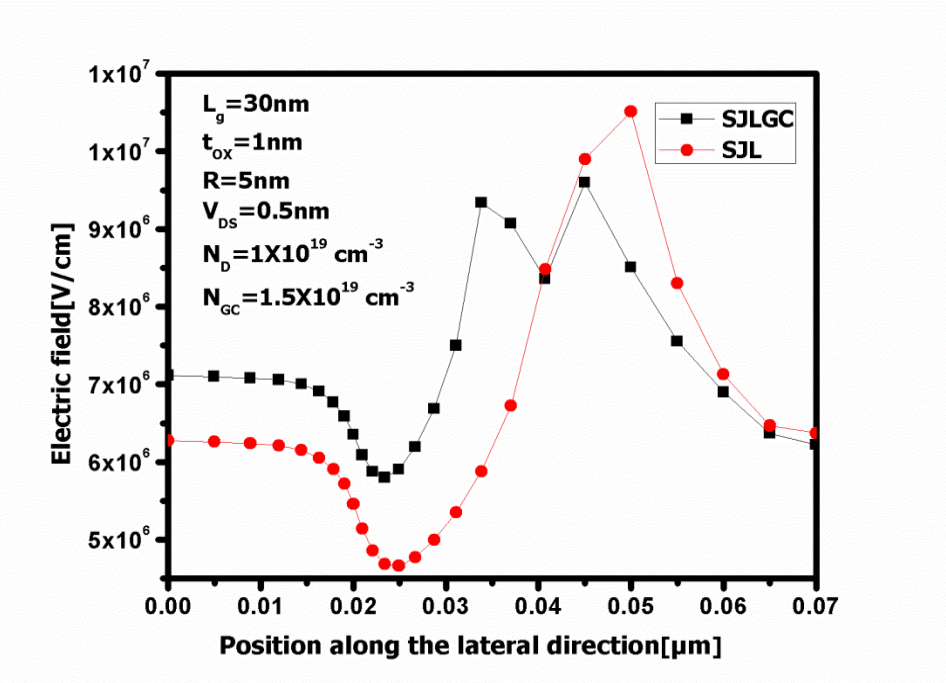

Fig.5 (b) : Average velocity of electrons along the channel in the lateral (z) direction at V_{GS} = 1.0 V, $L_{S/D}$ = 20 nm, L_{GC} = 15 nm, ϕ_m = 5.0 eV for SJLGC and SJL MOSFETs. The channel is located from x = 0.020 μm to x = 0.050 μm.

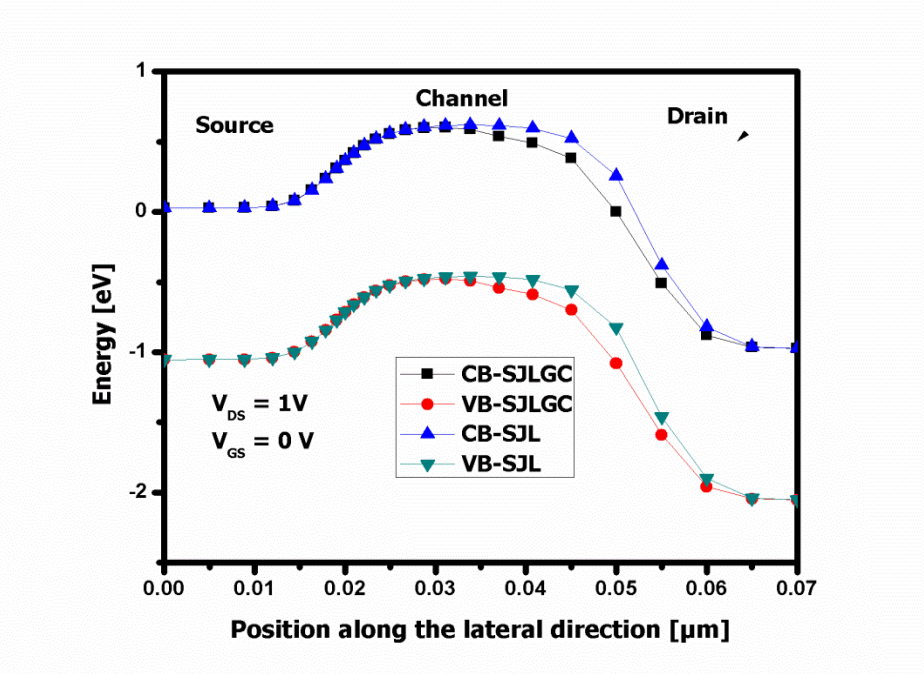

Fig.6 : Energy band SJLGC and SJL MOFETs along the channel in the lateral (z) direction at V_{GS} = 0 V, V_{DS} =1 V $L_{S/D}$ = 20 nm, L_{GC} = 15 nm, ϕ_m= 5.0 eV for SJLGC and SJL MOSFETs. The channel is located from x = 0.020 µm to x = 0.050 µm.

The centre potential of SJLGC MOSFET increases faster than the SJLMOSFET along the channel from x = 0.020 µm to x = 0.050 µm shown in Fig. 4. This is due to the higher transportation of carriers towards the drain end. There is a small change in potential as shown in Fig.4 from x=0.015 µm to x=0.025 µm. This is due to the absence of concentration gradient as these two points are maintained at a constant doping concentration of $1X10^{19}$ cm^{-3} .The potential towards the source region is the built in potential Vbi i,e Vbi= $(K.T/q)\ln(N_D/ ni)$ where *ni* is the intrinsic carrier concentration in silicon and the potential at the drain region is $V_{bi} + V_{DS}$[44,42]. The potential at the source region is 0.528 volt as depicted in Fig.4 which is the built-in potential (V_{bi}). The potential towards the drain region is at 1.028 volt as shown in Fig.4 which is $V_{bi} + V_{DS}$ and V_{DS} is kept at 0.5volt during simulation. A discontinuity in lateral electric field is observed in the channel region creating two different peaks for the proposed device whereas the traditional SJL MOSFET is said to have a single peak of electric field towards drain end as shown in Fig.5 (a). The extra peak of electric field developed in the middle of the channel lowers the impact of electric field created at the drain end for SJLGC MOSFET. Due to lowering of electric field created at the drain, the electrons are strongly pulled from the source towards the channel region in SJLGC MOSFET in comparison to SJL MOSFET. This enhances the transportation efficiency of carrier[45].Improved carrier transportation results in enhancement of drain current (I_{ds}), transconductance (g_m),cut off frequency (f_T).This extra electric field increases the non-equilibrium transportation capability of carriers in terms of their velocity as shown in Fig.5 (b) near the source end. The magnitude of electric field is the gradient of the potential[46].In Fig.5(a) , a valley like shape is observed because from x=0.015 µm to x=0.025 µm, the change or gradient in potential in Fig.4 is very less which is clear from the readings of simulation

corresponding these particular values of x. Hence, the electric field decreases towards x=0.025 µm. From x=0.025 µm to x=0.030 µm, the change in potential increases in Fig.4, as a result the electric field increases. The electron velocity is proportionally related to its electric field. Hence electron velocity changes accordingly w.r.t electric field and same valley like shape is observed in Fig. 5(b) at x=0.025 µm. The energy band diagram of SJLGC MOSFET and SJL MOSFET is shown in fig.6. The energy band bends more in SJLGC MOSFET supporting easy flow of carriers from source to drain as the source to channel barrier height decreases [47-48] .This results in increase in drain current.

SECTION-IV

1. ANALOG PERFORMANCES

Higher value of I_D results in higher value of transconductance (g_m) as clear from Fig.7. The change in drain current is more at V_{GS}=1.1 Volt as depicted in Fig.3(a) which illustrates the plot of I_D Vs V_{GS}. Hence the transconductance is said to have its highest peak at V_{GS} =1.1 Volt as evident from Fig.7.

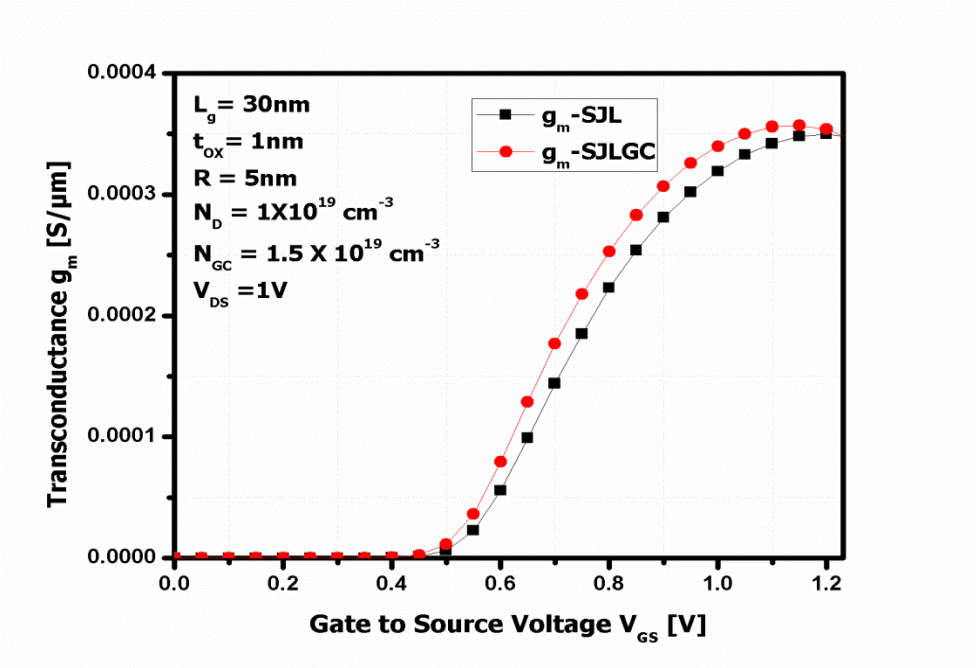

Fig.7: A plot of transconductance (g_m) w.r.t V_{GS} for SJLGC and SJL MOSFETs at ϕ_m = 5.0 eV, L_{GC} = 15 nm.

SJLGC MOSFET exhibits lower drain to source conductance (g_{ds}) as compared to SJL MOSFET as shown in Fig. 8. The cause behind this is the discontinuity in electric field at the position along the channel where the channel is graded with higher doping concentration which redistributes the electric field mainly towards the drain end .When V_{DS} increases in the region of saturation, the highly doped region of channel absorbs the extra drain voltage beyond saturation

and restricts the further punch through of electric field into the source end. This physical phenomenon is called screening effect which is the main cause of lowering the g_{ds} [49].

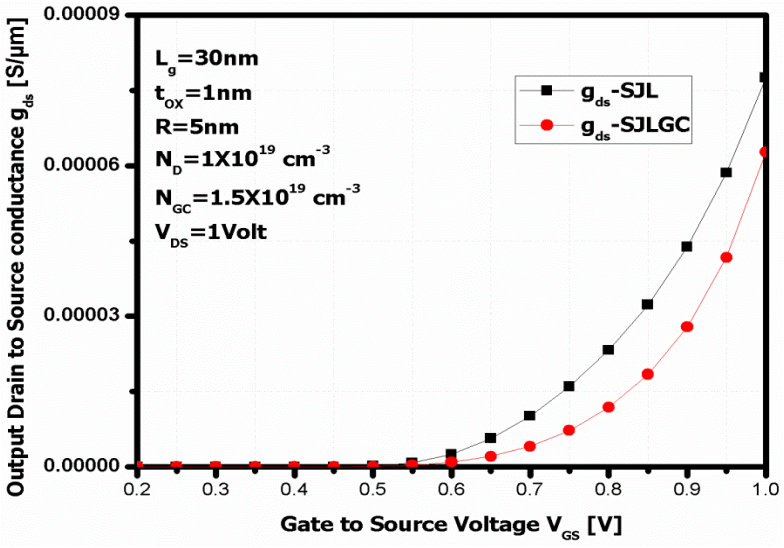

Fig.8: A plot of output conductance (g_{ds}) with respect to V_{GS} for SJLGC and SJL MOSFETs at L_{GC} = 15nm, ϕ_m = 5.0 eV.

Transconductance generation factor (TGF) is the ratio of transconductance (g_m) to the drain current (I_D). It is one of the key performance parameters considered in the design of subthreshold low power applications. The traditional SJL MOSFET possesses a slightly higher value of TGF in comparison to our proposed device as depicted in Fig. 9. This lower value of TGF for SJLGC MOSFET will not be regarded as its demerits as a very less power is consumed in the sub threshold region.

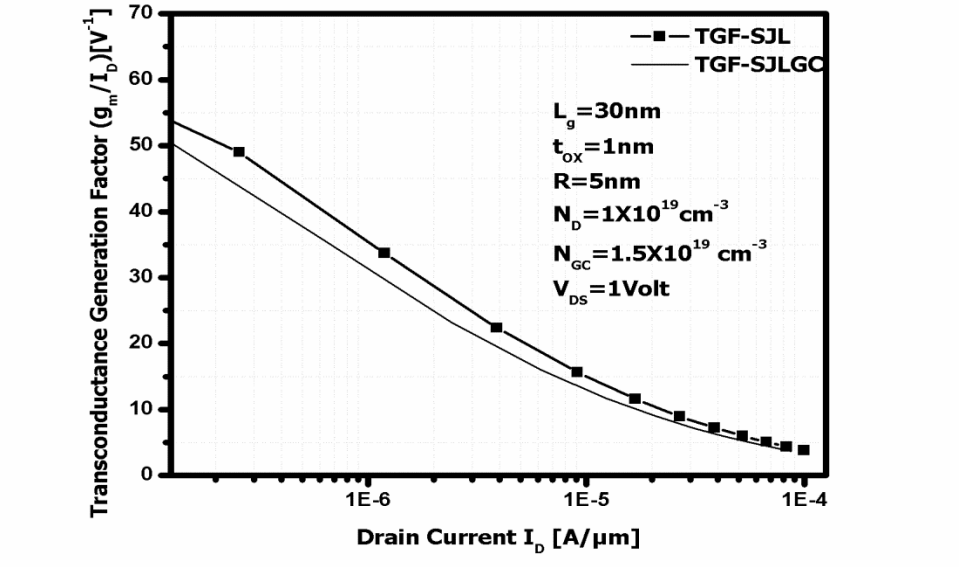

Fig. 9 : A plot of transconductance generation factor (TGF) with respect to V_{GS} for SJLGC and SJL MOSFETs at L_{GC} =15 nm, ϕ_m= 5.0 eV.

Intrinsic gain is referred as the ratio of transconductance to drain conductance (g_m / g_{ds}). SJLGC MOSFET outperforms the conventional SJL MOSFET device in terms of intrinsic gain as shown in Fig.10. This result is due to lower value of g_{ds} possessed by our proposed device.

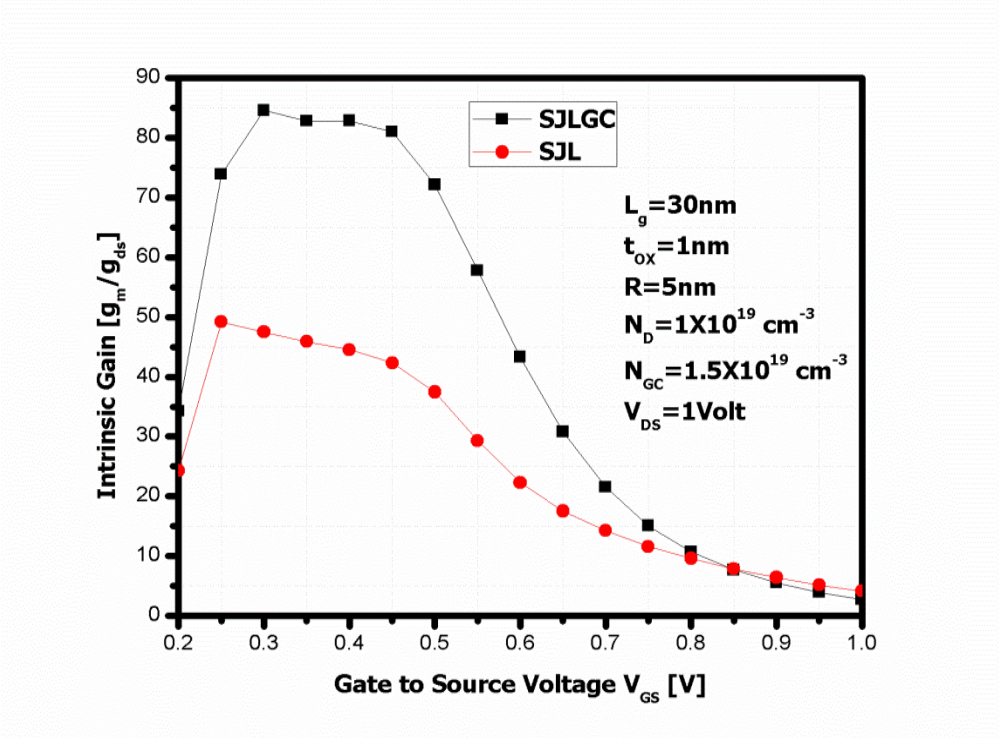

Fig.10: A plot of intrinsic gain with respect to V_{GS} for SJLGC and SJL MOSFETs at L_{GC}=15nm, ϕ_m= 5.0 eV.

2. *RF ANALYSIS*:

In fig (11-13), we have compared the inter electrode capacitances of the proposed device with the traditional one such as gate to drain capacitance (C_{GD}), gate to source capacitance (C_{GS}), gate to gate capacitance ($C_{GG} = C_{GS} + C_{GD}$).

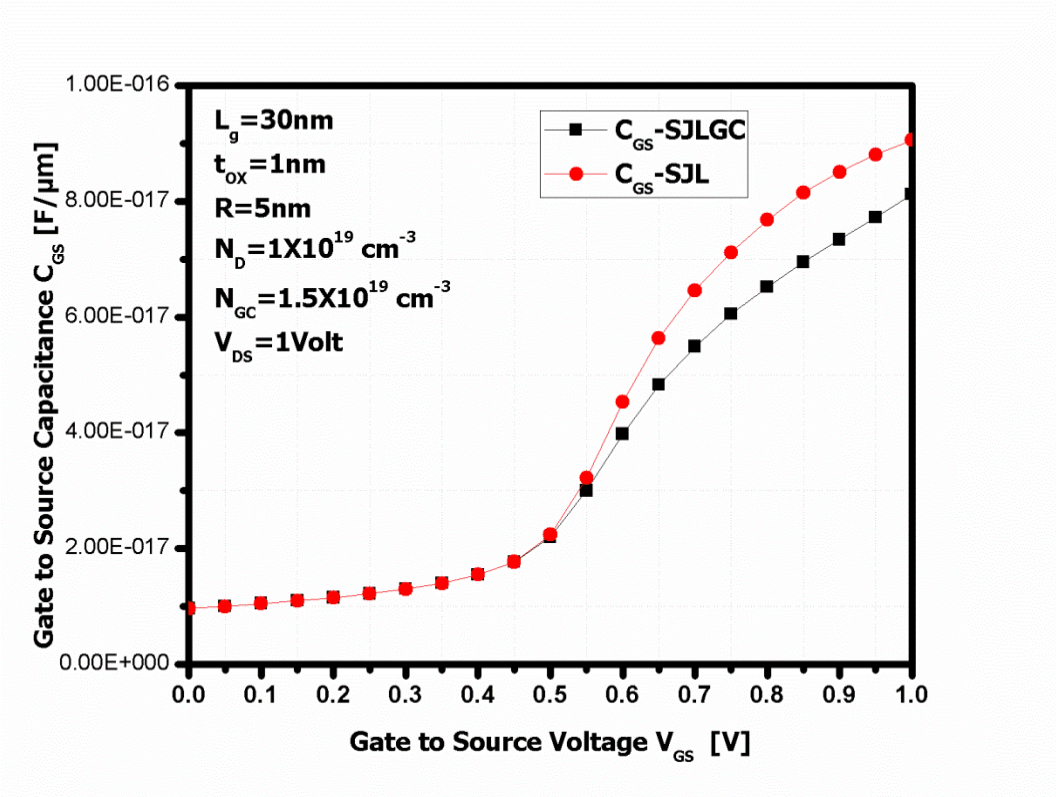

Fig .11: Variation of C_{GS} w.r.t V_{GS} for SJLGC MOSFET and SJL MOSFET at L_{GC}=15nm, ϕ_m=5.0 eV.

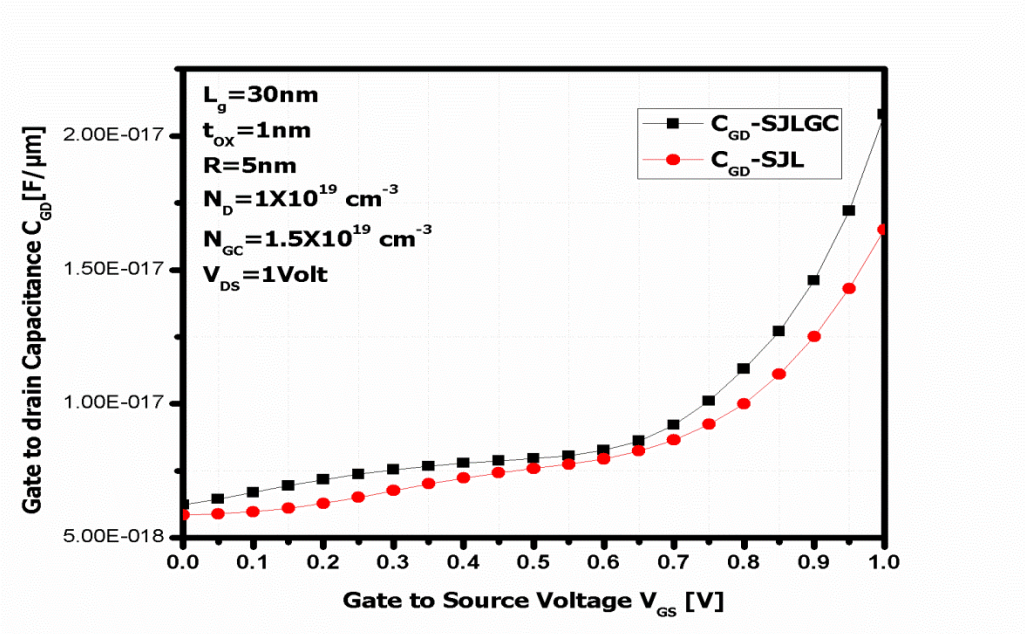

Fig.12 : Variation of C_{GD} w.r.t V_{GS} for SJLGC MOSFET and SJL MOSFET at L_{GC} =15 nm, ϕ_m = 5.0 eV.

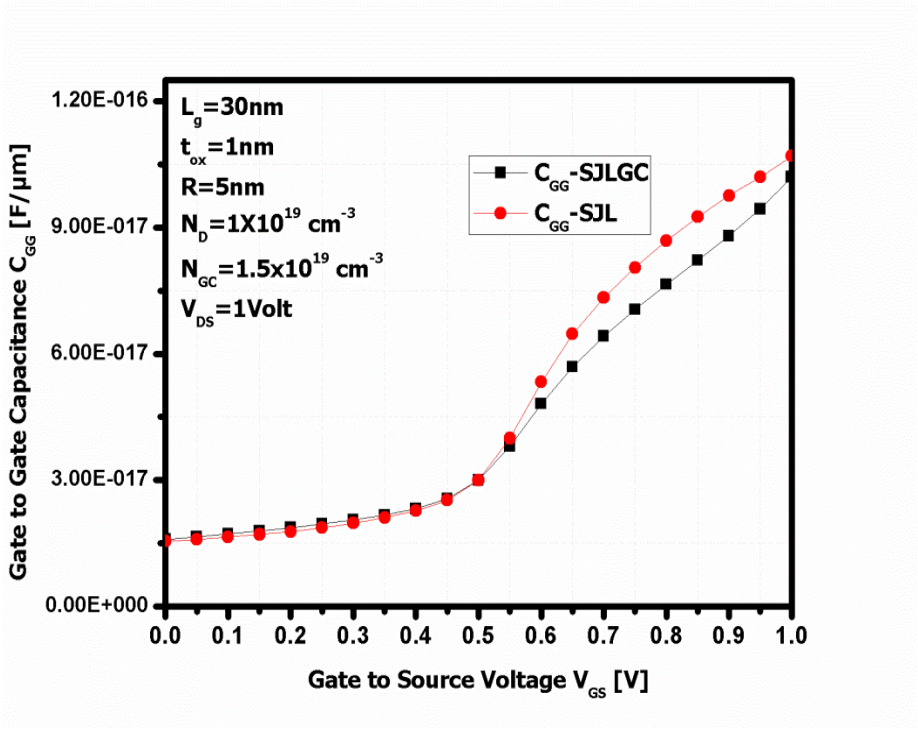

Fig.13: (a) Variation of C_{GG} with respect to V_{GS} for SJLGC MOSFET and SJL MOSFET at L_{GC} = 15 nm, ϕ_m = 5.0 eV.

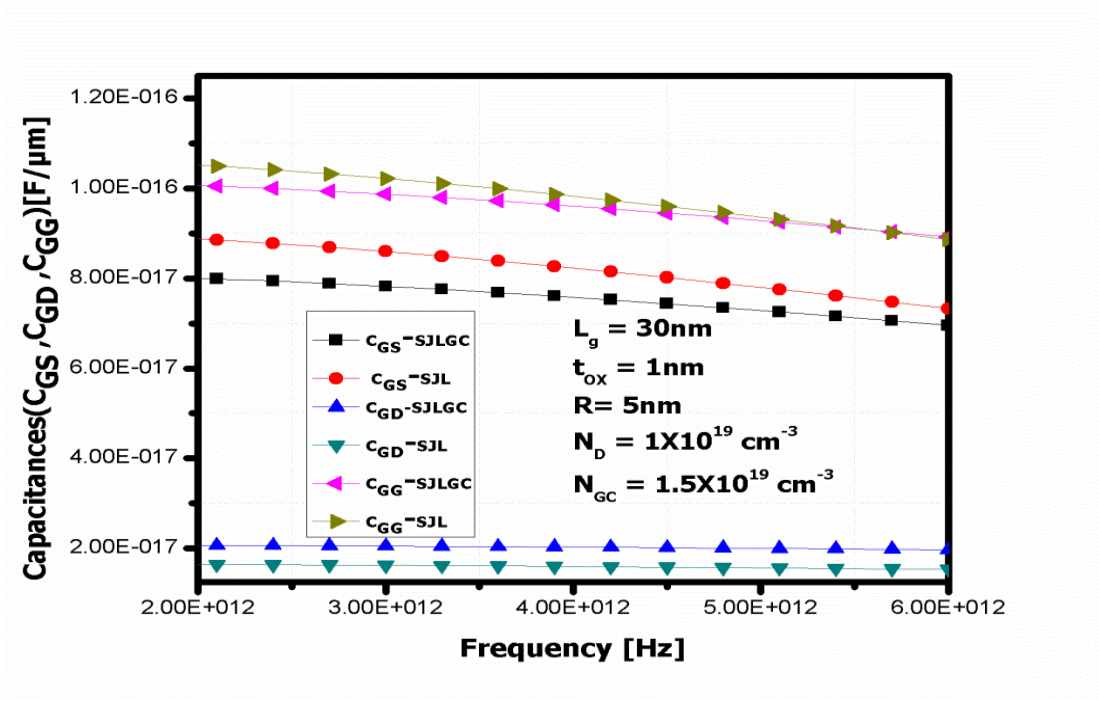

Fig.13: (b) Variation of inter electrode capacitances with respect to frequency for SJLGC MOSFET and SJL MOSFET at V_{GS} = 1 V, V_{DS} = 1V, L_{GC} =15 nm, ϕ_m = 5.0 eV.

The use of higher doping concentration at the middle of the channel results in lower value of C_{GS} and higher value of C_{GD} in SJLGC MOSFET in comparison to SJL MOSFET as shown in Fig.11 and Fig.12. C_{GD} of SJLGC MOSFET in the present work is higher than that of SJL MOSFET because the graded channel portion towards the drain end is doped with higher concentration (1.5 x $10^{19}cm^{-3}$) which results in creating different sheet charge densities along the direction of transportation [20].

The discontinuity in electric field profile in SJLGC MOSFET along the channel reduces the inversion charges towards the source end of the channel, thereby making the V_{GS} less effective for the inversion of channel near the source region. Due to this reason the value C_{GG} decreases in SJLGC MOSFET in comparison to SJL MOSFET as indicated in Fig.13. (a). The variation in all the inter electrode capacitances with respect to multiple frequencies are shown in fig.13. (b). The interelectrode capacitances are almost constant with a negligible variation with respect to frequency, representing themselves to be frequency independent terms [50-51].

In this section RF performance of the proposed device is compared with the conventional one with respect to different FOMs such as cut off frequency (f_t), maximum frequency of oscillations (f_{max}), intrinsic time delay, critical frequency (f_k).

The minimum frequency at which the current gain attains a value of unity is regarded as the cut off frequency (f_T). f_T is the key performance parameter for comparing the devices used in high speed digital switching operation. The frequency at which the maximum unilateral power gain falls to 0 dB (unity) is considered as the maximum frequency of oscillation (f_{max}). f_{max} is important for comparing the devices used in tuned radio frequency amplifiers. Intrinsic delay (ζ_D) is another performance metric for analyzing the devices applied in digital high speed applications. The evaluation of f_T, f_{max}, ζ_D are done using the following analytical expressions [52-54].

$$f_T = \frac{g_m}{2\pi(C_{GD}+C_{GS})} = \frac{g_m}{2\pi C_{GG}} \quad (3)$$

$$f_{\max} = \frac{f_T}{\sqrt{4R_G(g_{ds}+2\pi f_T C_{GD})}} \quad (4)$$

$$\varsigma_D = \frac{C_{GG}.V_{DS}}{I_{on}} \quad (5)$$

The incorporation of graded channel in the proposed device increases the electrons mobility by weakening the electric field in the drain end. This results in improvement of cut off frequency of the proposed device as depicted in Fig. 14. SJLGC MOSFET exhibits improvement in f_{max} as shown in Fig.15. More number of free charge carriers are accumulated in the channel region with the increase in V_{GS}, as a result drain current (I_D) and transconductance (g_m) increases. At higher value of V_{GS}, the electric field is maximized and the electron velocity is saturated resulting in

decrease in g_m [55]. Both cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}) are proportional to transconductance (g_m) as evident from equation (3) and (4). When V_{GS} increases from sub threshold regime, f_T rises due to higher g_m and lower gate to gate capacitance (C_{GG}). The fall in f_T at higher value of V_{GS} is due to the simultaneous impact of increasing C_{GG} and limiting transconductance (g_m) [56].The peak values of f_T for SJL and SJLGC MOSFETs are at 370 GHz and 536 GHz , resulting in a improvement in 45% . f_{max} shows the same behaviour as f_T with respect to V_{GS} . This is due to the compensation of increase in parasitic drain to source capacitance with decrease in g_{ds}. f_{max} is having its peak value at 1705 GHz and 2185 GHz for SJL MOSFET and SJLGC MOSFET respectively showing an improvement of 29%.The reduction in intrinsic delay of SJLGC MOSFET is shown in Fig.16. The decrease in C_{GG} and increase in I_{on} of SJLGC MOSFET lead to the reduction of intrinsic delay as compared to the conventional SJL MOSFET.

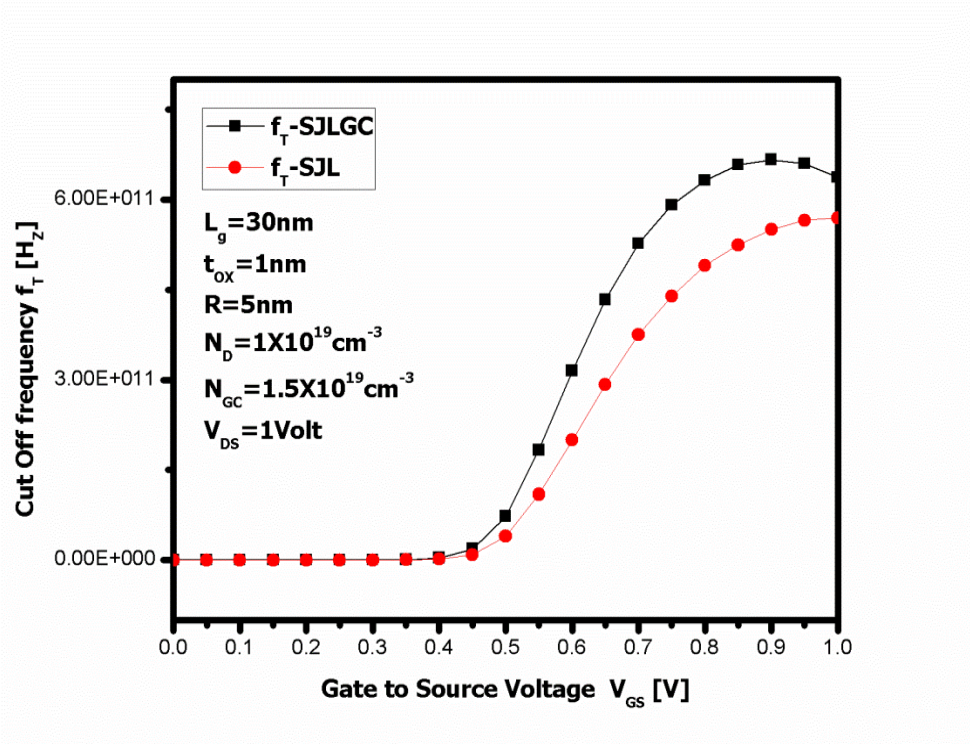

Fig.14: A plot of cut-off frequency (f_T) with respect to V_{GS} for SJLGC and SJL MOSFETs at L_{GC} = 15 nm, ϕ_m = 5.0 eV.

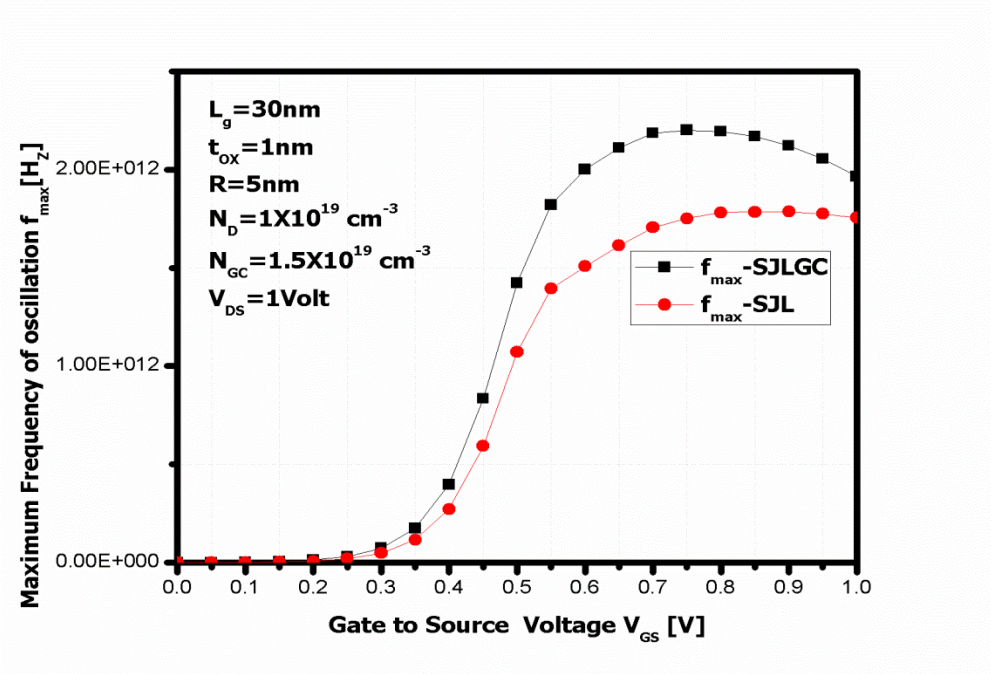

Fig.15: A plot of maximum frequency of oscillation (f_{max}) with respect to V_{GS} for SJLGC and SJL MOSFETs at ϕ_m = 5.0 eV, L_{GC} = 15 nm.

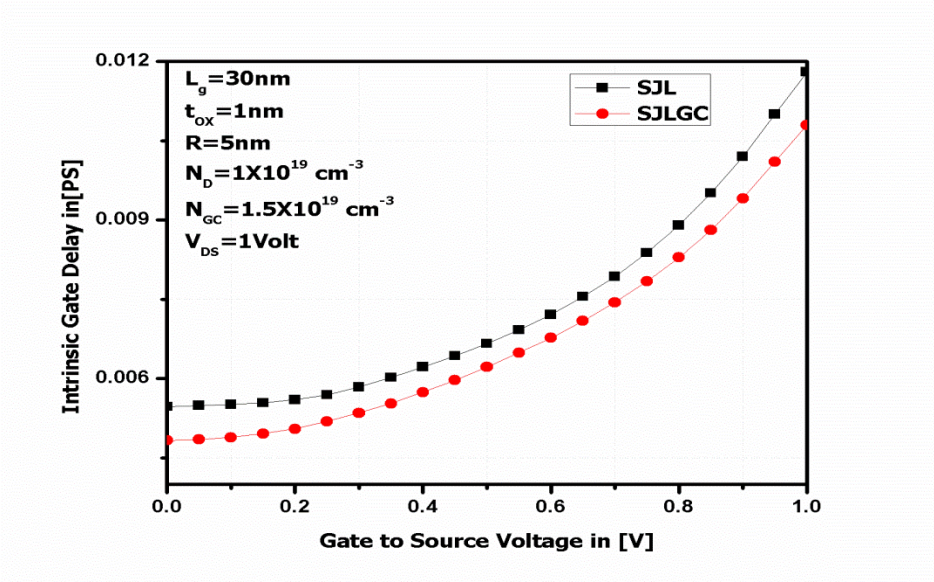

Fig.16: A Plot of intrinsic gate delay (ζ_D) w.r.t V_{GS} for SJLGC and SJL MOSFETs at ϕ_m = 5.0 eV, L_{GC} = 15 nm.

Stability of LNA should be investigated for the designing of RF and microwave amplifiers. The best possible way to inquiry the stability is to evaluate the stern's stability factor (K).The frequency at which K is exactly equal to 1 is the critical frequency (f_k) [57-58]. The expression for K is given by

$$K = \frac{1+|\Delta|^2-|s_{11}|^2-|s_{22}|^2}{2.|s_{12}.s_{21}|} \qquad (6)$$

Where S_{11}, S_{22} are reflection coefficients and S_{12}, S_{21} are transmission coefficients. Δ is the S matrix which is defined as: $\Delta = (S_{11} \times S_{22}) - (S_{12} \times S_{21})$.

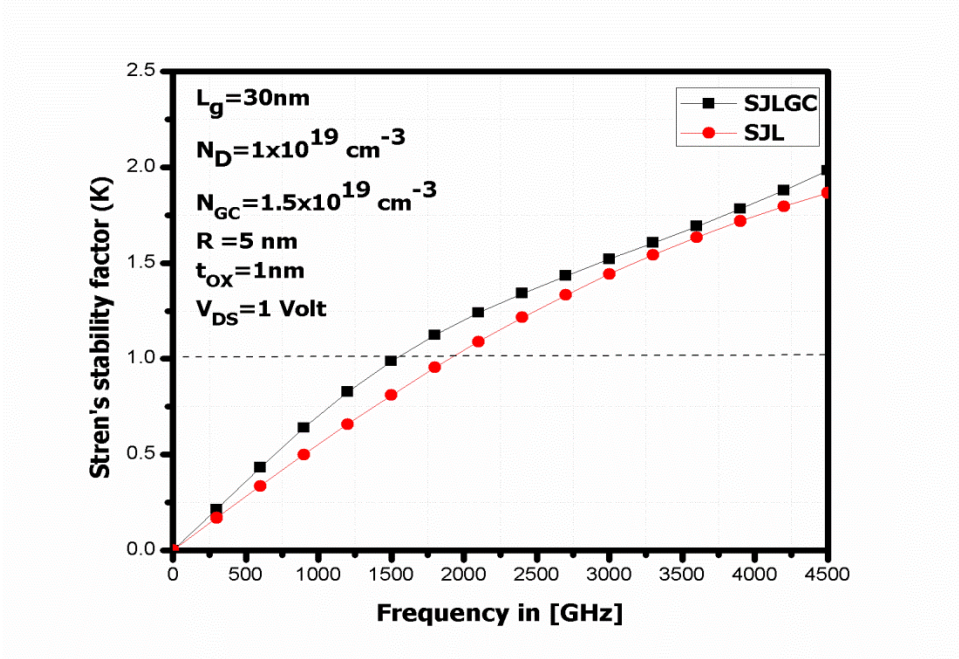

Fig.17: Stern's stability factor (K) for SJLGC and SJL MOSFETs for V_{DS}=1V, V_{GS}=1 V with respect to different frequencies.

The value of K is more for SJLGC MOSFET than for SJL MOSFET in higher frequencies as indicated in Fig.17. The critical frequency f_K for SJLGC and SJL MOSFETs are 1500 GHz and 1800 GHz respectively as evident from Fig.17 and shows an improvement of 18%. This result suggests that SJLGC MOSFET attains stability from 1500GHz without the need of any complex hardware circuitry for stabilization. The comparison of all the FOMs in between the two devices that we have discussed so far are summarised in Table-3 given below:

Table-3

COMPARISION OF ANALOG/RF FOMs FOR THE PROPOSED DEVICE AND CONVENTIONAL DEVICE AT V_{GS} = 0.7 V, V_{DS} =1.0V

Figure of Merits(FOMs)	**SJL**	**SJLGC**
Transconductance (g_m) [S / µm]	1.43803E-4	2.2675E-4
Output Conductance(g_{ds}) [S / µm]	1.01E-5	4.107E-6
Transconductance Generation Factor (TGF) [V^{-1}]	20.2	18.5
Intrinsic gain (g_m/g_{ds})	13	27
Gate to Gate Capacitance (C_{GG}) [F/ µm]	8.33E-17	6.12E-17
Cut off frequency (f_T) [GHz]	370	536
Maximum frequency of oscillation (f_{max}) [GHz]	1705	2185
Intrinsic gate delay (ζ_D) [ps]	0.00793	0.00664
Critical frequency (f_k) [GHz]	1800GHz	1500GHz

SECTION-V

Conclusion

This paper mainly focuses on the impact of graded channel in the surrounded gate junctionless architecture on the Analog and RF performances with respect to the key performance parameters such as TGF, intrinsic gain, cut-off frequency (f_T), maximum frequency of oscillation (f_{max}), stern's stability factor (K), Critical frequency (f_K). The result of performance comparison between SJLGC MOSFET and SJL MOSFET shows an enhancement in Analog and RF performances for the proposed device. The cause for this improvement is the existence of additional electric field peak at the position along the channel where the channel is graded. This additional peak speeds up the transportation capability of the charge carriers and the energy band bending is more resulting in higher drain current in SJLGC MOSFET. There is an improvement in drain current(I_D), f_T, f_{max}, and f_K by 10.03% , 45%, 29% and 18% respectively in SJLGC MOSFET showing better RF Performance. SJLGC MOSFET shows 74% improvement in intrinsic voltage gain (g_m/g_{ds}) than SJL MOSFET indicating its better applications in sub threshold region. Hence, in this paper, we conclude that SJLGC MOSFET is an attractive and competitive contender of the advanced structure MOSFETs for high speed RF applications with improved stability. SJLGC MOSFET is also a promising candidate for designing a stable LNA used in ultra-wide band RF amplifiers.

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Conflict of Interest

The authors declare that they have no conflict of interest.

Author contributions

Sarita Misra,Sudhansu Mohan Biswal - Conceptualization, methodology, simulation and investigation, Biswajit Baral,Sanjit Kumar Swain - Writing original draft preparation, reviewing and editing, Sudhansu Kumar Pati -Validation and overall correction.

Availability of data and material

The authors confirm that the data supporting the findings of this study are available within the article, its supplementary materials or below mentioned references.

Compliance with ethical standards

This article does not contain any studies with human participants or animals performed by any of the authors.

Consent to participate

All authors freely agreed and gave their consent to participate on this work.

Consent for Publication

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