Power Efficient Multichannel Discrete Time Based LTI System for DSP

Vivak Jain

Techno India Navdeep Jitendra Ranawat Institute of Technology: Techno India NJR Institute of Technology

Prasun Chakrabarti

Techno India Navdeep Jitendra Ranawat Institute of Technology: Techno India NJR Institute of Technology

Ananda Shankar Hati (✉ anandashati@iitism.ac.in)

Indian Institute of Technology (Indian School of Mines), Dhanbad <https://orcid.org/0000-0003-1414-3398>

Prince Kumar

Indian Institute of Technology (Indian School of Mines): Indian Institute of Technology

Research Article

Keywords: power-efficient, multichannel, particle swarm optimization, FPGA

Posted Date: June 25th, 2021

DOI: <https://doi.org/10.21203/rs.3.rs-638762/v1>

License: © ⓘ This work is licensed under a Creative Commons Attribution 4.0 International License.

[Read Full License](#)

Power Efficient Multichannel Discrete Time Based LTI System for DSP

Vivek Jain · Prasun Chakrabarti · Ananda Shankar Hati · Prince Kumar

Received: date / Accepted: date

Abstract This paper proposes a power-efficient multichannel discrete-time system based on a Cat swarm-based optimization algorithm for multi-signaling processing of the different signals from different musical instruments. The purpose is to provide an adjustable signalling rate to avoid aliasing. The multichannel discrete-time system can increase and decrease the sampling frequency by fraction value according to the incoming signal's maximum frequency from various musical instrument sources. Here, the multichannel discrete-time system introduces zeros and removes the samples uniformly according to requirements. To make it power efficient and reduce resource utilization by applying particle swarm optimization algorithm at the implementation time on FPGA.

Keywords power-efficient · multichannel · particle swarm optimization · FPGA

1 Introduction

In many applications such as digital communications, music industry, speech encoding, and decoding, MIMO system multi-rate signal processing is required. For that purpose, develop a multichannel discrete-time system for matching the required sampling rate for signals from different sources. We apply a practical swarm-based

optimization algorithm to make it power-efficient in terms of dynamic power and static power consumption. For that purpose, we use the different structures of discrete-time structure cascaded integrator comb(CIC), multiply accumulator (MAC) and cascaded multiply-accumulate CMFIR based design. CMFIR design developed by authors is the combination of CIC and MAC architecture. We apply a practical swarm-based optimization algorithm on CMFIR based architecture [1] [2].

The proposed LTI system is implemented using a CMFIR filter. CMFIR filter consumes less power and fewer resources consumption with significant bandwidth response due to anti-sinc function and optimized coefficient of CMFIR filter. The optimized coefficient required less space for storage and less switching from 0 to 1 and 1 to 0. The proposed LTI system is implemented up to 128 channels using time-division multiplexing. The novelty of this Proposed Model:

1. The proposed LTI system is implemented using the CMFIR structure with the cat-swarm optimization algorithm.
2. It contains 128 input channels.

Fig. 1 CMFIR Filter

2 Literature Survey

The length (order) of the direct form FIR filter structure-based sample rate converter linearly increases with the

F. Author and S. Author
Techno India NJR Institute of Technology, Udaipur, Rajasthan, India
E-mail: vivek.jain@technonjr.org of F. Author E-mail: drprasun.cse@gmail.com of S. Author

T. Author and Forth. Author
IIT (ISM) Dhanbad, India
E-mail: anandashati@iitism.ac.in of T. Author E-mail: ee.prince@ieee.org of Forth. Author

sampling rate. Consequently, it increases the utilization of register, flip flops, LUT, and power consumption by directly forming an FIR structure-based sample rate converter. In poly-phase decomposition FIR structure-based sample rate converter, the original length of the filter is divided into multiple stages. The problem with poly-phase FIR structure-based sample rate converter is that it does not work correctly when the sampling rate is changed significantly [3].

The anti-sinc function gives the output of the MAC filter with respect to frequency change. MAC FIR frequency response neutralizes the effect of sinc function. MAC architecture-based sample rate converter is efficiently used for significant bandwidth signal, but it increases resource utilization such as registers and flip-flops because of the large size of filter coefficients, leading to increased power consumption [4] [5].

FIR filter develops and design with respect to given specifications using the equi-ripple method but requires more memory to store filter coefficient. So, we need to reduce the storage requirement of the filter coefficient [6] [7].

So, we need to reduce power consumption, memory utilization, and resource utilization iteratively but keep the LTI system's frequency response within specification. The memory storage requirement of the filter coefficient is reduced by applying CAT Swarm-based optimization algorithm [8].

Jyothi, G.N., Sanapala, K. & Vijayalakshmi implement memoryless FIR filter. The filter input is MLDA form, and output is converted into a binary form using the Chinese theorem [9].

P. Kokil, S. Jogi, C. K. Ahn, and H. Kar improved the digital filter output stability by isolating the filter from external environmental interference and noise [10].

M. N. Kapetina, M. R. Rapaić uses an adaptive algorithm to measure the real-time parameter of the LTI system, such as propagation delay and system function [11].

T. Bindima and E. Elias implement a 2D filter using a farrow structure. 1D-poly phase 1D is the base for designing and developing of 2D-FIR filter [12].

A. Mitra and S. Sundaram developed an LTI system for sensors to measure the input from different structure nodes without any communication losses [13].

D. Ray, N. V. George, and P. K. Meher implement the FIR filter by using Single constant multiplication (SCM), and multiple constant multiplications (MCM) are among the most popular schemes [14].

J. Zheng and Z. Wei implement the FIR By combining FPGA and DSP technology features for increasing the speed of mathematical operation such as integration and differentiation [15].

MoorthiKiruban, Raja Jayamani implement FIR filter using BSCE algorithm. Multiple Constant Multiplication method consumes less power as compared to other implementation methods [16].

Bonetti, A. Teman, P. Flatresse and A. Burg implement the FIR filter in which power reduction is taken at run time without degrading the filter's performance [17].

J. Chen, J. Tan, C. Chang and F. Feng implement FIR filter by eliminating repeated expression without affecting the filter output [18].

3 Research Gap

From the literature review, limitations of existing models of LTI system find out:

1. CIC FIR structure-based LTI system has limited bandwidth. Its frequency response contains sinc function. Sinc function limited its output to small bandwidth.
2. Direct form FIR structure-based LTI system required many recourses such as flip flop and register for high order system.

The proposed LTI system is implemented using a CM-FIR filter. CMFIR design developed by which is a combination of CIC and MAC architecture. CMFIR filter large bandwidth response due to the antisinc function of MAC filter, and recourse optimisation is achieved by optimizing the coefficient size of the LTI system by applying a practical swarm-based optimisation algorithm. Optimised coefficient required less space for storage.

4 Cascaded Multiple-Accumulate Finite Impulse Response (CMFIR)

Our proposed Cascaded Multiple-Accumulate Finite Impulse Response (CMFIR) filter-based system may fulfil our requirement. CMFIR filter is the combination of CIC FIR and MAC FIR filter. CMFIR provides the features of both CIC and MAC FIR architecture. An essential additional function provided by the CMFIR is compensation for the passband drop introduced by the CIC filter. The structure of the CMFIR filter is shown in figure [1].

CIC filter is designed by a basic two-unit comb & integrator. In the design of the CIC filter, there is no need for a multiplier. The output of the MAC filter with respect to the frequency change is contained anti-sinc function. MAC FIR output eliminates the sinc response of CIC filter. MAC architecture-based sample rate converter is efficiently used for large bandwidth signal [19] [20]. Features of CMFIR:

1. Power consumed by the CMFIR LTI system is meagre.
2. CMFIR LTI system provides output for large bandwidth Due to the anti-sync feature.
3. Re-courses such as flip flop, LUT and Register requirement decreases.

5 Mathematical Modeling of the CAT SWARM based optimisation algorithm

The cat swarm optimisation is a continuous and single-objective algorithm. It is developed by monitoring the lifestyle of cats; cats spend their maximum time resting and tracing, but the consciousness of cat is maximum, and they are monitor what happened around them. When the cat identifies the target, then they move towards the target as soon as possible. Therefore, the CSO algorithm is designed by using such behaviour of the cat. CSO algorithm is operated in two modes tracing and seeking. Using that algorithm, we find out best solution or values coefficients for a discrete time sys-tem to best optimise power consumption and resource utilisation [21] [22]. Calculation of coefficients of LTI system with weight function.

1. A large number of coefficient enables greater global searchability.
2. The small number of coefficient enhances local searchability.

In our proposed design global search approach.

$$F(k) = \frac{f_{max} - (f_{max} - f_{min})i}{C_{max}} \quad (1)$$

where f_{max} is Largest value of existing coefficient array, f_{min} is smallest value of existing coefficient array, i is index of array, C_{max} is max no. of iterations.

Fig. 2 CMFIR Filter

Fig. 3 CMFIR Filter

Fig. 4 CMFIR Filter

Fig. 5 CMFIR Filter

Fig. 6 CMFIR Filter

6 Results

The figures 2-13 and tables 11-12 show efficiency of CMFIR Filter with Cat Swarm algorithm based multi-

Table 1 Total Power Efficiency of CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm with respect to other Fraction Sample Rate Converters

Number of Channel (s)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to MAC Filter Architecture Based Fraction Sample Rate Converter (%)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to CIC Filter Architecture Based Fraction Sample Rate Converter (%)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to CMFIR Architecture Based Fraction Sample Rate Converter Without Cat Swarm Algorithm (%)
1	85.78	3.17	1.61
2	87.31	2.86	1.45
4	88.58	4.40	2.25
8	85.29	8.53	7.09
16	80.59	16.18	12.76
32	74.04	24.37	17.18
64	67.02	17.59	13.33
128	62.08	14.29	7.38

Table 2 Dynamic Power Efficiency of CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm with respect to other Fraction Sample Rate Converters

Number of Channel (s)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to MAC Filter Architecture Based Fraction Sample Rate Converter (%)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to CIC Filter Architecture Based Fraction Sample Rate Converter (%)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to CMFIR Architecture Based Fraction Sample Rate Converter Without Cat Swarm Algorithm (%)
1	54.55	11.76	6.25
2	47.62	8.33	4.35
4	26.79	8.89	4.65
8	25.26	13.41	11.25
16	28.90	21.15	16.89
32	32.83	27.78	19.93
64	30.51	19.04	14.53
128	30.74	14.81	7.56

Table 3 Static Power Efficiency of CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm with respect to other Fraction Sample Rate Converters

Number of Channel (s)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to MAC Filter Architecture Based Fraction Sample Rate Converter (%)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to CIC Filter Architecture Based Fraction Sample Rate Converter (%)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to CMFIR Architecture Based Fraction Sample Rate Converter Without Cat Swarm Algorithm (%)
1	88.38	0.00	0.00
2	90.69	0.00	0.00
4	93.48	0.00	0.00
8	93.35	0.00	0.00
16	93.22	0.00	0.00
32	92.97	1.96	0.00
64	93.00	5.66	3.85
128	92.90	8.93	5.56

Table 4 Efficiency of CMFIR Filter with Cat Swarm Algorithm Based Multichannel Discrete Time System with respect to CIC Filter, MAC Filter and CMFIR Filter without Cat Swarm algorithm Based Multichannel Discrete Time System for Static Power Consumption.

Number of Channel (s)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to MAC Filter Architecture Based Fraction Sample Rate Converter (%)
2	76.80
4	76.55
8	76.77
16	76.77
32	76.74
64	76.44
128	76.79

Table 5 Efficiency Table of Register Utilization of CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm with respect to CIC Architecture Based Fraction Sample Rate Converter.

Number of Channel (s)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to CIC Filter Architecture Based Fraction Sample Rate Converter (%)
2	62.60
4	62.15
8	62.42
16	62.39
32	62.32
64	61.83

Table 6 Efficiency Table of Register Utilization of CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm with respect to CMFIR Architecture Based Fraction Sample Rate Converter without Cat Swarm Algorithm

Number of Channel (s)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to CMFIR Architecture Based Fraction Sample Rate Converter Without Cat Swarm Algorithm (%)
2	0.86
4	0.32
8	0.87
16	0.87
32	0.72
64	0.27
128	1.45

Table 7 Efficiency table of LUT utilisation of CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm with respect to MAC Architecture Based Fraction Sample Rate Converter

Number of Channel (s)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to MAC Filter Architecture Based Fraction Sample Rate Converter (%)
2	87.78
4	87.37
8	87.94
16	87.96
32	76.74
64	76.44
128	87.78

Table 8 Efficiency table of LUT utilisation of CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm with respect to CIC Architecture Based Fraction Sample Rate Converter

Number of Channel (s)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to to CIC Filter Architecture Based Fraction Sample Rate Converter (%)
2	77.54
4	76.71
8	77.72
16	77.75
32	62.32
64	61.83

Table 9 Efficiency Table of LUT Utilisation of CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm with respect to CMFIR Architecture Based Fraction Sample Rate Converter without Cat Swarm Algorithm

Number of Channel (s)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to MAC Filter Architecture Based Fraction Sample Rate Converter Without Cat Swarm Algorithm(%)
2	4.00
4	4.39
8	4.12
16	4.15
32	0.72
64	0.27
128	6.42

Table 10 Efficiency table of LUT –Flip Flop Pair Utilization of CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm with respect to MAC Architecture Based Fraction Sample Rate Converter

Number of Channel (s)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to MAC Filter Architecture Based Fraction Sample Rate Converter (%)
2	84.28
4	84.40
8	66.83
16	67.81
32	68.294
64	69.69
128	68.78

Table 11 Efficiency Table of LUT –Flip Flop Pair Utilization of CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm with respect to CIC Architecture Based Fraction Sample Rate Converter

Number of Channel (s)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to CIC Filter Architecture Based Fraction Sample Rate Converter (%)
2	70.25
4	70.20
8	46.31
16	46.78
32	46.98
64	47.39
128	47.26

Table 12 Efficiency table of LUT-Flip Flop Pair Utilization of CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm with respect to CMFIR Architecture Based Fraction Sample Rate Converter without Cat Swarm Algorithm

Number of Channel (s)	CMFIR Architecture Based Fraction Sample Rate Converter with Cat Swarm Algorithm efficiency with respect to MAC Filter Architecture Based Fraction Sample Rate Converter Without Cat Swarm Algorithm (%)
2	7.84
4	8.16
8	4.57
16	4.41
32	3.62
64	2.04
128	1.09

Fig. 7 CMFIR Filter

Fig. 8 CMFIR Filter

Fig. 9 CMFIR Filter

Fig. 10 CMFIR Filter

channel discrete-time system with respect to CIC Filter, MAC Filter and CMFIR Filter without Cat Swarm algorithm based multichannel discrete-time system for total power consumption, dynamic power consumption,

Fig. 11 CMFIR Filter

Fig. 12 CMFIR Filter

Fig. 13 CMFIR Filter

static power consumption and resource utilisation such as register, flip flop and LUT-Flip Flop pair.

$$\text{Power efficiency} = \left(\frac{P_{old} - P_{new}}{P_{old}} \right) \times 100 \quad (2)$$

where P_{old} is power consumed by the old or existing model, P_{new} is power consumed by the new or proposed model.

Power efficiency more means system is power consumption decreases.

$$\text{Resource utilization efficiency} = \left(\frac{R_{old} - R_{new}}{R_{old}} \right) \times 100 \quad (3)$$

where R_{old} is the power consumed by the old or existing model R_{new} is power consumed by the new or proposed model

7 Discussion

The multichannel discrete-time system with Cat Swarm algorithm-based architecture most efficient structure because it consumes less static power, dynamic power and implemented using less resource such as register, flip-flop and LUT-Flip-Flop Pair. Dynamic power, static power efficiency and power consumption efficiency increase whereas power consumption decreases. The advantages of less power consumption are the increase of battery life, less heat dissipation, and no heat sink requirement. It means the more power efficiency of the system, the more efficient system is. Similarly, when resources utilisation efficiency increases, resources utilisation decreases. It requires a less chip area. It means the more resource utilisation efficiency of the system is, the more efficient system is.

The paper entails the following:

1. The Multichannel CMFIR based system efficiency in term of power & resource utilisation has been improved.
2. The multichannel discrete-time system with Cat Swarm algorithm-based architecture efficiency in terms of the average total power reduction is 78.84 %.
3. The average dynamic power reduction is 34.65 %, and the average static power reduction is 92.25 % with respect to the MAC-based architectures.
4. The multichannel discrete-time system with Cat Swarm algorithm-based architecture efficiency in terms of the average total power reduction is 11.42 %. The average dynamic power reduction is 15.65 %, and the average static power reduction is 2.07 % with respect to the CIC based architectures.
5. The discrete multichannel system with Cat Swarm-algorithm-based architecture time efficiency in terms of the average total power reduction is 7.88 %. The average dynamic power reduction is 10.68 %, and the average static power reduction is 1.18 % with respect to the CMFIR without Cat Swarm algorithm-based architectures.
6. The CMFIR based LTI system with Cat swarm optimisation algorithm is the best architecture because it consumes less power and implements less resource utilisation.

The future work scope is to implement a 256 channel swarm algorithm-based power-efficient LTI system that can be used in digital image processing and speech processing applications.

References

1. E. Hogenauer, "An economical class of digital filters for decimation and interpolation," *IEEE transactions on acoustics, speech, and signal processing*, vol. 29, no. 2, pp. 155–162, 1981.
2. R. E. Crochiere and L. R. Rabiner, "Interpolation and decimation of digital signals—a tutorial review," *Proceedings of the IEEE*, vol. 69, no. 3, pp. 300–331, 1981.
3. L. Ming and Y. Chao, "The multiplexed structure of multi-channel fir filter and its resources evaluation," in *2012 International Conference on Computer Distributed Control and Intelligent Environmental Monitoring*. IEEE, 2012, pp. 764–768.
4. V. Jain and N. K. Agrawal, "Reconfigurable multichannel down convertor for on chip network in mri," in *ICT and Critical Infrastructure: Proceedings of the 48th Annual Convention of Computer Society of India-Vol I*. Springer, 2014, pp. 799–806.
5. S. Thakral, D. Goswami, R. Sharma, C. K. Prasanna, and A. M. Joshi, "Design and implementation of a high speed digital fir filter using unfolding," in *2016 IEEE 7th Power India International Conference (PIICON)*. IEEE, 2016, pp. 1–4.
6. D. Agarwal, K. S. Reddy, and S. Sahoo, "Fir filter design approach for reduced hardware with order optimization and coefficient quantization," in *2013 International Conference on Intelligent Systems and Signal Processing (ISSP)*. IEEE, 2013, pp. 293–296.
7. K. Grover, R. Mehra *et al.*, "Fpga based decimator using fully parallel technique for hearing aid applications," in *2017 3rd International Conference on Computational Intelligence & Communication Technology (CICCT)*. IEEE, 2017, pp. 1–6.
8. M. B. Trimale *et al.*, "A review: Fir filter implementation," in *2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*. IEEE, 2017, pp. 137–141.
9. G. N. Jyothi, K. Sanapala, and A. Vijayalakshmi, "Asic implementation of distributed arithmetic based fir filter using rns for high speed dsp systems," *International Journal of Speech Technology*, pp. 1–6, 2020.
10. P. Kokil, S. Jogi, C. K. Ahn, and H. Kar, "An improved local stability criterion for digital filters with interference and overflow nonlinearity," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 3, pp. 595–599, 2019.
11. M. N. Kapetina, M. R. Rapaić, A. Pisano, and Z. D. Jeličić, "Adaptive parameter estimation in lti systems," *IEEE Transactions on Automatic Control*, vol. 64, no. 10, pp. 4188–4195, 2019.
12. T. Bindima and E. Elias, "Low-complexity 2-d digital fir filters using polyphase decomposition and farrow structure," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 6, pp. 2298–2308, 2019.
13. A. Mitra and S. Sundaram, "Distributed observers for lti systems," *IEEE Transactions on Automatic Control*, vol. 63, no. 11, pp. 3689–3704, 2018.
14. D. Ray, N. V. George, and P. K. Meher, "Efficient shift-add implementation of fir filters using variable partition hybrid form structures," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 12, pp. 4247–4257, 2018.
15. J. Zheng and Z. Wei, "Fir filter design based on fpga," in *2018 10th International Conference on Measuring Technology and Mechatronics Automation (ICMTMA)*. IEEE, 2018, pp. 36–40.
16. M. Kiruban and R. Jayamani, "A comparative study on fir filters for reconfigurable applications," *International Journal of Information and Communication Sciences*, vol. 3, no. 1, p. 1, 2018.
17. A. Bonetti, A. Teman, P. Flatresse, and A. Burg, "Multipliers-driven perturbation of coefficients for low-power operation in reconfigurable fir filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 9, pp. 2388–2400, 2017.
18. J. Chen, J. Tan, C.-H. Chang, and F. Feng, "A new cost-aware sensitivity-driven algorithm for the design of fir filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 6, pp. 1588–1598, 2017.
19. V. Jain, N. Agarwal, and P. Chhawchharia, "Development of low power multi channel interpolator for system on chip in 4g application," in *2014 IEEE Microwaves, Radar and Remote Sensing Symposium (MRRS)*. IEEE, 2014, pp. 111–114.
20. M. Kadam, K. Sawarkar, and S. Mande, "Investigation of suitable dsp architecture for efficient fpga implementation of fir filter," in *2015 International Conference on Communication, Information & Computing Technology (ICCICT)*. IEEE, 2015, pp. 1–4.
21. J. G. Proakis, *Digital signal processing: principles algorithms and applications*. Pearson Education India, 2001.
22. S. Gavrilov, A. Glebov, S. Rusakov, D. Blaauw, L. Jones, and G. Vijayan, "Fast power loss calculation for digital static cmos circuits," in *Proceedings European Design and Test Conference. ED & TC 97*. IEEE, 1997, pp. 411–415.
23. X.-S. Yang, *Nature-inspired metaheuristic algorithms*. Luniver press, 2010.
24. R. Eberhart and J. Kennedy, "Particle swarm optimization," in *Proceedings of the IEEE international conference on neural networks*, vol. 4. Citeseer, 1995, pp. 1942–1948.