A Novel Method of Designing an all Optical 3-Bit Asynchronous Counter

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A novel method of designing an all optical 3-bit asynchronous Counter

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Abstract :

In digital signal processing and data communication system in optical domain it is paramount important to count the pulse number of any device or processor and hence optical counter for fast counting. In this letter the authors propose a new method to implement an all-optical 3- bit asynchronous binary counter comprising all-optical T flip flops which works based on the polarization switching characteristics of SOA, and frequency encoded data have been used for communication purpose. Use of Frequency encoding technique in the proposed scheme makes it attractive and effective one in various aspects in wave division multiplexing based communication network. Simulation aided results support the practicability of the proposed scheme.

Keywords: Optical Asynchronous Counter, All optical flip-flops, Frequency encoding, Polarisation switch.

1. Introduction:

Present day's communication demand fast and secure data processing. So, one of the important way-outs is to switch over our interest from electronic to optical communication. To implement our desired all optical communication we need optical logic gates, processors, memory unit, etc. Counter is such an important processor which is used to count number of pulses in case of data transmission. Counter is a one kind of registers which can go through a certain determined sequence of states. A Clock pulse, pulses originated from outside source maintaining a specific time interval or some random pulses can be used as input pulse. The

sequencing of the state follows binary pattern or any other kinds of sequence. Optical counter is considered as a key element because in optical packet switching it could be used as packet buffers, as frequency converter, and also finds potential applications in many more optical high speed data transfer networks.

Flip-flop is the basic element for designing any types of counter. Over a period of time various attempts have been made by many research groups to design optical flip flops, synchronous and asynchronous counters [1-11]. Optical flip-flop using two polarization switches has been demonstrated by Y. Liu [1]; Zhang et al. demonstrated the working of Multi -state flip flop using ring laser[2]]; S. Mandal et al. described a method to design AOFF using PSW[3,4]; T. Chattopadhyay et al. designed AOFF using TOAD[5,6] ,MZI-SOA based flip-flops[7], Micro-ring resonator based flip-flops[8]. All optical synchronous counter has been demonstrated by Tamer [9] based on two coupled polarisation switches(PSWs)flip flops; Asynchronous counter based on JK flip-flop memory has been described by T.A .Moniam[10]; Synchronous counter by exploiting Kerr nonlinearity has been reported also by Mitra et al.[11]. In this letter the authors proposed an all optical 3-bit asynchronous counter using T flip flop which works on the basis of frequency conversion and polarisation switching action(PSW)of semiconductor optical amplifier(SOA)with the help of frequency encoding technique. Several types of technique for encoding/decoding of optical data for example spatial encoding[12] , intensity encoding[13,14], polarization encoding[15], phase encoding[16] , etc. has been reported till date. But all these mentioned techniques have some own limitations. The frequency encoded data have been utilised here because of it's unique nature of constancy in case of absorption, refraction, reflection, etc, throughout the entire communication. Here binary '0' state has been encoded by the optical signal of ' ν_0 ' frequency and binary '1' state is encoded with the help of optical signal of ' ν_1 'frequency. **The article is organised as follows:**

Section-1 is the introduction of the proposed scheme. In section-2 switching and frequency conversion action of the SOA has been explained. Section-3 and Section-4 covers the design of the two input NOR gate and three input AND gate circuit and explains their operation of it supported by the simulation results. Section-5 deals

with the circuit design, its operation followed by the simulation results of the JK flip flop. In Section-6 the design and operation of the proposed asynchronous counter is explained, and lastly Section-7 contains discussion of the proposed scheme.

2. Working principle of polarisation switch :

The proposed optical circuit works on the principle of polarization switching action of SOA [17, 20-21]. A high intensity optical beam is injected to the SOA as the pump beam. Another beam of comparatively low intensity is used as the probe beam of SOA via an attenuator as shown in Fig-1. The function of polarization controller (PC) is to maintain the polarization state of the probe beam. The polarization beam splitter (PBS) splits the amplified probe beam into two components. When the pump beam is absent, the amplified power of the probe beam will appear at the output port-2, but in the presence of pump beam of sufficient intensity almost all the power will appear at output port-1. The mechanism of the nonlinear polarisation rotation of the probe beam in SOA is based on the works of Dorren, et al.[17]

Fig.1. SOA acting as the polarization switch (PSW)

The difference in phase between the TE and TM mode is given by equation

$$\Delta\Phi = \frac{1}{2} \left(\frac{\alpha^{TE} \Gamma^{TE} g^{TE}}{V_g^{TE}} - \frac{\alpha^{TM} \Gamma^{TM} g^{TM}}{V_g^{TM}} \right) L \quad [1]$$

Fig.2 shows how the phase difference between two modes varies with input pump beam power. In the presence of the pump beam of power about 0.5 mW , the phase

difference is $\Delta\Phi = 180^\circ$ between two modes[18]. The resultant output power can be calculated by

$$P_{out} = P_{out}^{TE} + P_{out}^{TM} + \sqrt{P^{TE} P^{TM}} \cos(\Delta\phi) \quad [2]$$

The power variation at port-1 and port-2 with the input pump power are shown in Fig.3.and Fig.4, respectively. The values of some useful parameters used for SOA simulation are: $\Gamma^{TE} = 0.2$, $\Gamma^{TM} = 0.14$, $\alpha^{TE} = \alpha^{TM} = 5$, $\xi^{TE} = 7.0 \times 10^{-9} \text{ ps}^{-1}$, $\xi^{TM} = 6.5 \times 10^{-9} \text{ ps}^{-1}$, $v_g^{TE} = v_g^{TM} = 100 \text{ } \mu\text{m} / \text{ps}$, $F=0.5$, $N_0 = 10^8$, $L = 800 \text{ } \mu\text{m}$, $T_1 = 500 \text{ ps}$, $\alpha_{int}^{TE/TM} = 0.27 \text{ ps}^{-1}$, $e = 1.6 \times 10^{-19} \text{ C}$.The optical power of the probe beam used here is 0.03 mW[19].

Fig.2. Phase difference at the output end of the PSW with the input power of the pump

Fig.3: Output power at port-1 of PSW with pump beam power

Fig.4: Output power at port-2 of PSW with pump beam power

3. Scheme of two-input NOR gate:

Fig.5 Schematic diagram of two-input NOR gate

The proposed optical two-input NOR gate is designed with three polarisation switches (PSW) P1, P2 and P3, two DMUXs (D1 and D2), and two MUXs (M1 and M2), as shown in Fig.5. Input beam 'A' is directly applied to D1 whereas the input beam 'B' is applied to P1 via attenuator. D1 routes the input beam 'A' in accordance to the frequency. Its channel -1 passes the frequency ν_0 , whereas channel-2 passes ν_1 frequency. Output port-1 of P1 is connected to the input of D2. Channel-1 and Channel-2 of D2 also carries the beam of frequency ν_0 and ν_1 , respectively. Channel-1 of D2 is connected to P2 and it serves as pump beam of P2. Channel-2 of both the DMUXs are connected by MUX (M1), and the output of M1 is injected as the pump

beam of P3. Probe beam of frequency ν_1 and ν_0 are applied to P2 and P3, respectively. In the presence of pump beam all port-1 of PSWs remain on, and port-2 of all PSWs remain off. Both the port-1 of P2 and P3 are connected through MUX (M2), which gives the final output. The truth table of the frequency encoded data based proposed NOR gate is given in Table 1.

Frequency of the input signals		Frequency of the output signal
Input signal A	Input signal B	
ν_0	ν_0	ν_1
ν_0	ν_0	ν_0
ν_0	ν_0	ν_0
ν_1	ν_1	ν_0

Table 1. Truth table of frequency encoded two-input NOR gate

Case-1: $A = B = \nu_0$

Here input A (ν_0) transmits through the channel-1 of D1 and works as the pump beam for P1. On the other hand input B (ν_0) acts as the probe beam of P1. As pump beam is available for P1, it switches the applied probe beam to its port-1 which is then reaches to P2 via channel-1 of D2. This beam works as the pump beam for P2 and it switches the probe beam (ν_1) at the port -1 of P2. Finally this ν_1 frequency beam passes through M2 and appears as the final output. Here P3 not getting any pump does not contribute to the final output.

Case-2: $A = v_0$, $B = v_1$

Input $A(v_0)$ similar to the previous case serves as pump beam for P1 via channel-1 of D1 and Input beam B (v_1) works as the probe beam of P1. In the existence of pump beam, probe beam appears at port-1 of P1, and after being channelized through channel-2 of D2 and through M1 is injected as pump beam for P3. As P3 gets the pump beam, it switches its probe beam (v_0) to port-1, which gives the final output via M2.

Case -3: $A = v_1$, $B = v_0$

Here input beam $A(v_1)$ works as the pump beam for P3 after passing through channel-2 of D1 and M1 respectively. Input beam B (v_0) is applied as the probe beam to P1, but not receiving any pump beam its port-1 remains off. Consequently P2 also remains off. In this case P3 receives pump beam, so it switches the probe beam (v_0) to its port-1, which gives the final output after passing through M2.

Case -4: $A = B = v_1$

Here function of both input beams is same as mentioned in the previous case. Input beam A and B works as the pump and probe beam of P3 and P1 respectively. But as P1 does not receive any pump beam, its port-1 remains off. P2 also remains off as it does not receive any pump beam from D2. On the other hand P3 receiving the pump beam, switches the probe beam (v_0) to its output port-1, which gives the final output via M2.

In Fig. 6 the simulated power spectrum of input and output beams of the proposed NOR gate is shown. Gaussian pulse with full width at half maximum (FWHM) of 0.4 nm is used here to represent the input and output beams. Here Binary bit '0' has been encoded with the optical signal of frequency 1.9317×10^{14} Hz (v_0) and the equivalent wavelength is 1552 nm. Similarly binary bit '1' has been encoded with optical signal of frequency 1.9255×10^{14} Hz (v_1) and the equivalent wavelength is 1557 nm.

Fig. 6. Simulation results of the two-input NOR gate (input A is at binary 1 state and input B is at binary 0 state, i.e., case-3) and (all the inputs are at binary 1 state, i.e., case-4)

4.Scheme of three input AND Gate:

Fig. 7 Schematic diagram of three-input AND gate

The proposed optical three-input AND gate is made up by four polarisation switches (PSW) P1, P2, P3 and P4; three DMUXs (D1, D2 and D3); and two MUXs (M1 and M2) as shown in the Fig.7. Input signal 'A' is applied to D1 while another input signal 'B' is applied to P1 via an attenuator. D1 channelizes the input beam A

in accordance to the frequency; its channel -1 carries frequency v_0 , whereas channel-2 carries v_1 frequency. Channel-2 of D1 deliveries the pump beam to P1. Output port-1 of PSW (P1) is connected to D2. Functions of both the channels in D2 are the same as that of D1. The beam passing through Channel-2 of D2 works as pump beam of P2. The third input signal C is applied as probe beam to P2 via an attenuator. Output port-1 of P2 is connected to D3. The output obtained from Channel-2 of D3 serves as the pump beam for P3. Channel-1 of all the DMUXs are connected by MUX (M1) . The output of M1 is applied as the pump beam of P4. Optical beam of frequency v_0 and v_1 are applied as the probe beam of P4 and P3, respectively. In the existence of pump beam ,port-1 of all PSWs remain on , and port-2 of all PSWs remain off. Port-1 of P3 and P4 are connected through MUX(M2),which gives the final output. The truth table of the proposed AND gate in frequency domain is given in Table-2 .

Input signals			Output signal
A	B	C	Y
v_0	v_0	v_0	v_0
v_0	v_0	v_1	v_0
v_0	v_1	v_0	v_0
v_0	v_1	v_1	v_0
v_1	v_0	v_0	v_0
v_1	v_0	v_1	v_0
v_1	v_1	v_0	v_0
v_1	v_1	v_1	v_1

Table 2. Truth table of frequency-encoded three-input AND gate

Now working of the proposed scheme of the AND logic gate is explained as below:

Case-1: $A = v_0, B = v_0, C = v_0 / v_1$

Input beam A being of frequency v_0 , it passes through channel-1 of D1 and acts as the pump beam of P4 via M1. Input beam B (v_0) and C (v_0 or v_1) are applied as the probe beams to P1 and P2, respectively. As both the PSW (P1 and P2) does not receive any pump beam, so they remain inactive. So P3 also remains inactive. While on getting the pump beam P4 switches the applied probe beam of frequency v_0 to its output port-1 which finally gives the output through M2. Therefore, whatever be the frequency of the input C, the output gives the beam of frequency v_0 for this case.

Case-2: $A = v_0, B = v_1, C = v_0 / v_1$

Similar to the previous case, the input signal A (v_0) after passing through the channel-1 of D1 serves as pump beam for P4 via M1. Input signal B (v_1) is applied as probe beam of P1. Similarly input beam C (v_0 or v_1) is applied as probe beam to P2. But both the PSW (P1 and P2) not receiving any pump beam remain inactive, consequently P3 also remains off. On the other hand P4 gets the pump beam. So it switches the probe beam of frequency v_0 to its output port-1, which is appeared as the final output via M2.

Case-3: $A = v_1, B = v_0, C = v_0 / v_1$

This time input A (v_1) passes through the channel-2 of D1 and acts as pump beam for P1. Input beam B (v_0) is used as probe beam to P1. On getting the pump beam, P1 transfer the probe beam to its port-1. As a result v_0 frequency arises at the port-1 of P1 which subsequently serves as pump beam for P4 via channel-1 of D2 and after that through M1. Input beam C (v_0 or v_1) is used as probe beam to P2. But P2 not getting any pump beam remains off. Consequently P3 also remains off. Now as P4 receives the pump beam, it switch the probe beam of frequency v_0 to its port-1 and that gives the final output through M2. Here also same situation happens in terms of the output beam frequency as the earlier two cases.

Case-4: $A = B = v_1, C = v_0$

Now input signal $A(v_1)$ is utilized as pump beam for P1 after it passes through the channel-2 of D1. Input beam B (v_1) serves as the probe beam for P1 and in the presence of pump signal it appears at port-1 of P1. It is then acts as pump beam for P2 via channel-2 of D2. Input beam C (v_0) serves as the probe beam for P2. As P2 gets the pump beam, it transfers the probe beam to its port-1. Thus at port-1 of P2, v_0 frequency appears which is then used as pump beam for P3 through D3. P3 switches the applied probe beam of frequency v_1 to it's output port-1 .Thus v_1 frequency is obtained as the final output through M2. Here P4 does not get any pump beam ,so it remains off.

Case -5 : $A=B = C = v_1$

Now we are interested to see what happens if all the three input beams are of frequency v_1 . Here input $A(v_1)$, after passing through channel -2 of D1 works as the pump beam of P1.Input $B(v_1)$ is applied as the probe signal to P1. On receiving the pump beam of sufficient intensity P1 transfer v_1 to it's port-1.Therefore at port-1 of P1, v_1 frequency arises, and it is used as the pump beam of P2 through channel-2 of D2.Now another input C(v_1) acts as the probe beam of P2. In presence of pump beam this probe beam (v_1) appears at port-1 of P2 and it serves as pump beam for P3 via channel-2 of D3. As a result P3 switches the probe beam (v_1) to it's port-1 .Thus v_1 frequency appears as the final output. In this case ,not getting any pump beam P4 contributes nothing towards the final output.

In **Fig 8** .the power spectrum of the simulated input and output signals are shown for the proposed AND gate.

Fig .8. Input-output spectrum of the three-input AND gate (Input A is at binary 0 state and both B and C are at binary 1 state, i.e., case-2) and (all the inputs are at binary 1 state, i.e., case-5)

5. Scheme of All optical clocked JK flip flop:

The proposed JK flip flop circuit comprises two 3-input all optical AND gates, two 2-input all optical NOR gates, two input named as 'J' and 'K' and a clocked pulse which is also given as the input to the both AND gates. We will discuss the whole operation of JK flip flop with clocked pulse in active 'HIGH' state (i.e. the frequency of clocked signal is taken as 'v₁' always.) The schematic diagram of the proposed all optical JK flip flop is shown in Fig.9. Earlier we have discussed the operational principle of all optical 3-input AND gate and 2-input NOR gate. So here the operation of JK flip flop will be explained on the basis of the early proposed gates. The frequency encoded input-output form of JK flip flop is shown in **Table 3**.

Fig.9. Scheme of all optical JK flip-flop

Frequency of the Input beam		Frequency of the output beam	
Input J	Input K	Output	Output $\bar{Q}$
v_0	v_0	Unchanged	Unchanged
v_0	v_1	v_0	v_1
v_1	v_0	v_1	v_0
v_1	v_1	Toggles	Toggles

Table 3 . Truth table of a JK flip- flop

Case 1 : $J = v_0, K = v_0$ (considering at this instant the previous output state $Q_n = v_0, \bar{Q}_n = v_1$)

In this case both the AND1, AND2 gives the beam of frequency v_0 at their respective outputs. Now as Q_n is of frequency v_0 and it is fed to NOR2, so it get both the inputs as the beam of frequency v_0 resulting ' v_1 ' frequency as output. Likewise $\bar{Q}_n$ is of frequency v_1 which is fed to NOR1. So on getting two different frequency signals as inputs, it gives the frequency ' v_0 ' as output. Finally we get Q_{n+1} as v_0 and $\bar{Q}_{n+1}$ as v_1 , which is same as the previous state outputs.

Case 2 : $J = v_0, K = v_0$ (considering at this instant the previous output state $Q_n = v_1, \overline{Q_n} = v_0$)

In this case AND1 gives v_0 frequency at the output but AND2, getting one of the inputs as v_0 frequency, gives v_0 frequency as its output. Now as Q_n is of frequency v_1 and it is fed to NOR2 resulting a frequency ' v_0 ' as output. Similarly NOR1 getting both the inputs as v_0 gives ' v_1 ' output. As a result we get $Q_{n+1} = v_1, \overline{Q_{n+1}} = v_0$, which is also same to its previous state.

Case 3 : $J = v_1, K = v_0$ (considering at this instant the previous output state $Q_n = v_0, \overline{Q_n} = v_1$)

Here as AND2 gets all its input beams of v_1 frequency, it gives output v_1 , but AND1 gives the frequency v_0 as outputs. Q_n which is the previous state output is of frequency v_0 and it is fed to NOR2 resulting a frequency ' v_0 ' as its output. Now this output is fed to NOR1 and it gives ' v_1 ' at the output. Finally we get Q_{n+1} as v_1 and $\overline{Q_{n+1}}$ as v_0 , i.e. output of the present state Q_{n+1} toggles to v_1 from v_0 , which is "SET" the flip-flop.

Case 4 : $J = v_1, K = v_0$ (considering at this instant the previous output state $Q_n = v_1, \overline{Q_n} = v_0$)

In this case AND2 gives v_0 output but AND1, getting one of the inputs as frequency v_0 gives the v_0 as its output. Now, as ' Q_n ' is of frequency v_1 and it is fed to NOR2, it gives frequency ' v_0 ' as output. Similarly NOR1 getting both the inputs as v_0 gives ' v_1 ' output. As a result we get $Q_{n+1} = v_1, \overline{Q_{n+1}} = v_0$ which is also same to its previous state.

Case 5 : $J = v_0, K = v_1$ (considering at this instant the previous output state $Q_n = v_0, \overline{Q_n} = v_1$)

Here as AND1 gets one of its input of v_0 frequency, it gives output v_0 . Similarly AND2 gives the frequency v_0 as outputs. Q_n which is the previous state output is of frequency v_0 and it is fed to NOR2, which getting both the inputs as v_0 frequency

gives 'v₁' as its output. When this v₁ frequency is fed to NOR1 which is getting the inputs of v₀ frequency gives 'v₀' frequency as output. Finally we get Q_{n+1} as v₀ and $\overline{Qn+1}$ as v₁, which are the previous state outputs.

Case 6 : J = v₀, K= v₁ (considering at this instant the previous output state Q_n = v₁, $\overline{Qn}$ = v₀)

In this case AND1 receives all of its input as v₁ frequency gives v₁ output but AND2 gives the v₀ as its output. Now as $\overline{Qn}$ is of frequency v₀ and it is fed to NOR1 gives frequency 'v₀' as output. This v₀ frequency along with the output of AND2 gives the NOR2 output 'v₁'. As a result we get Q_{n+1} = v₀, $\overline{Qn+1}$ = v₁, Thus the output of the present state Q_{n+1} toggles to v₀ from v₁, which "RESET" the flip flop.

Case 7 : J = K= v₁(considering at this instant the previous output state Q_n= v₀, $\overline{Qn}$ = v₁.)

In this situation AND2 gets all of its inputs of frequency v₁ gives output v₁, whereas AND1 gives output of frequency v₀. Q_n which in this case is taken as v₀ and fed to NOR2 gives frequency v₀ as its output. NOR1 is fed by $\overline{Qn+1}$ and AND1 (frequency v₀) also gives v₁ as output. so we get Q_{n+1} = v₁, $\overline{Qn+1}$ = v₀.

Case 8 : J = K= v₁(considering at this instant the previous output state Q_n = v₁, $\overline{Qn}$ = v₀)

Now we want to see what happens if Q_n = v₁ and $\overline{Qn}$ = v₀. In this condition AND1 after getting all its input of frequency v₁ also gives output of v₁ frequency, on other side AND2 gives v₀ as its output. Output of AND1 and $\overline{Qn}$ are fed to NOR1 gates and it results a frequency v₀ as its output. Whereas NOR2 being fed by AND2 and Q_{n+1} gives v₁ output. As a result we get Q_{n+1} = v₀, $\overline{Qn+1}$ = v₁.

Fig. 10 simulation results of clocked J K flip- flop

6. Design of the all optical 3-bit asynchronous Counter :

In a counter circuit on application of number of input pulses a set of unique combinations of output is produced and that number of unique outputs is called the mod number or modulus of the said counter. An n -bit binary counter comprising n number of flip-flops is able to count in binary from 0 to 2^n-1 number of pulses. Here in this paper authors have proposed a 3 bit asynchronous counter with frequency encoded bits. To design this we first have designed a T flip flop from a JK flip flop. The operational principle of frequency encoded clocked JK flip flop has already been

discussed in the previous section. Now to design a T flip flop we connect the J and K inputs as shown in Fig.11 below.

Fig.11. Design of T Flip flop from JK Flip flop

Input	Outputs	
T	Q_n	Q_{n+1}
V0	V1	V0
V1	V0	V1
V1	V1	V0
V0	V1	V1

Table 4: Excitation table of T flip-flop

In case of an asynchronous counter, the output transition from a flip-flop acts as a source to trigger other flip flops. The clock input of some of the flip flop or all the flip flops are generated by the transition that originates flip-flops outputs not by the common clock pulses. So to design a 3-bit asynchronous counter we need three such T flip-flops which are cascaded such that the output of the first flip flop is utilized as clock pulse for the subsequent flip flop. The schematic diagram of the said counter is shown in Fig.12.

Fig.12. Schematic diagram of a 3-bit asynchronous counter

Here all the T inputs are connected together and given a High input (Beam of frequency ν_1). The counting sequence of 3-bit asynchronous counter is given in the Table.5. The output waveform of the proposed counter is shown in Fig.13.

CLK	Q_2	Q_1	Q_0
0	ν_0	ν_0	ν_0
1	ν_0	ν_0	ν_1
2	ν_0	ν_1	ν_0
3	ν_0	ν_1	ν_1
4	ν_1	ν_0	ν_0
5	ν_1	ν_0	ν_1
6	ν_1	ν_1	ν_0
7	ν_1	ν_1	ν_1

Table 5. Counting sequence of a 3-bit counter

Fig.13. Output waveform of 3-bit asynchronous counter

Now following the excitation table of T flip-flop, when T input is of frequency signal v_1 then the output Q_{n+1} will be toggled and it depend on the previous state of the flip-flop. For example , when the output of the first flip-flop is of frequency v_1 ,only then the second flip-flop will toggle .Similarly the third flip-flop will toggle only when the outputs of both first and second flip-flop is of frequency v_1 .The entire operation starts working only when CLK pulse is present. The counter is first resets by making the outputs $Q_2Q_1Q_0$ at v_0 state .Now when first pulse is introduced LSB Q_0 becomes v_1 , Q_1 is in a condition to toggle if the next clock pulse has arrived. When the next pulse comes Q_1 and Q_0 simultaneously toggle. The final output taken from the consecutive $Q_2Q_1Q_0$ will be $v_0 v_0 v_1$ after the first pulse, $v_0 v_1 v_0$ after the second pulse, and after passing of the seventh pulse the counter will count $v_1 v_1 v_1$ as the final output.

7. Discussions:

In this paper authors have exploited the nonlinear rotation of the state of polarization(SOP) of the probe beam in semiconductor optical amplifier(SOA). Commercially available bulk JDS-uniphase SOA is used here to design the proposed circuits.[22-23]. In this SOA ,the required power of the pump beam is about 0.5 mW to the switch the probe beam from one port to another[24] . When pump beam is not present ,the SOA does not show any kind of nonlinearity. In this case the required probe beam power is restricted to 0.03 mW to have a faithful operation. To design 2-input NOR gate and 3-input AND gate at a time atleast two probe beam source is required. There are two AND gates, two NOR gates, in total four such gate is present in the proposed circuit of JK flipflop. So $2 \times 0.03 \times 4$ mW=0.24 mW optical power is required for the probe beams. Now in the circuit both the outputs Q_n and $\overline{Q_n}$ are feedback to the inputs. power of the both input is 0.5 mW each. So the power of the inputs J and K should not be greater than 0.03 mW. There is a clock inputs also. So power of the inputs = 0.03×3 =0.09 mW. Therefore the total optical power requied to operate a JK flip is = $0.24 + 0.09$ = 0.33 mW. Thus the requirement of power to operate 3-bit asynchronous counter is 3×0.33 =0.99mW, i.e., almost 1mW. For proper biasing of the PSW, 160mA current is required. So

according to our proposed circuit total $3 \times 14 \times 160 = 6.72$ A current is required. There must be some delay in any circuit. The delay due to feedback loop, and the duration of a clock pulse should be greater than the gain recovery time of SOA. The gain of the SOA remains constant in the C band. Thus it is best to select the frequencies for encoding data from this regime. We have chosen the frequency for encoding the data as 1.9317×10^{14} Hz (wave length 1552 nm.) for ν_0 and 1.9255×10^{14} Hz (wavelength 1557nm.) for ν_1 , respectively. The authors have considered a frequency encoded clock, which supplies optical beam of frequency 1.9255×10^{14} Hz (wavelength 1557nm.) and 1.9317×10^{14} Hz (wave length 1552 nm.)

8. Conclusion:

Our proposed JK flip flop can be applied in WDM based optical packet switching network. It can work as a memory unit to store a data packet temporally and then switch the data to different nodes according to the instruction of header signal. The counter can be used for up and down counting and can be comprehensively used for counting any number of pulses by extending the circuits with required number of optical flip flops. This scheme is designed using the flip flops and the propagation delay in case of optical flip flop is very small, however that can also be minimised in future by reducing the number of flip flops.

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