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## Research Article

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# “Thermal Eraser” to mitigate screening current by optimal control on spatial temperature distribution in a high temperature superconductor magnet

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## ABSTRACT

The so-called “screening current” in high temperature superconductor (HTS) is a well-known phenomenon that has detrimental effects on performance of an HTS magnet. To date, many research efforts have been devoted to suppressing *screening current* in an HTS magnet. Here we report a *customized* electric-heater, named “Thermal Eraser”, to mitigate the *screening current*. The key idea is to optimally control spatial temperature distribution in an HTS magnet using the customized heater and the consequent temperature-dependent local critical current of HTS wires of the magnet. To validate the idea, a Thermal Eraser was designed, constructed, and installed in an actual single-pancake HTS coil. And the Thermal Eraser plus test coil system was operated at temperatures ranging 7 - 40 K in our in-house conduction-cooling cryogenic facility. The feasibility of the Thermal Eraser was demonstrated in terms of two aspects: 1) creation of the designated spatial temperature distribution within the HTS test coil *as designed*; and 2) quantitative evaluation of its effectiveness to mitigate *screening current* using both experimental and numerical results. We confirmed that the *screening current induced field* in the test coil was reduced by 0.6 mT after activation of the Thermal Eraser, which implies 60% reduction of *screening current* in the HTS test coil. The results demonstrate that the Thermal Eraser is a viable option to effectively reduce the *screening current* in an HTS magnet.

## Introduction

Recent progress in high temperature superconductor (HTS) magnet technology is notable. Some laboratory HTS magnets reached magnetic fields far beyond 25 T<sup>1-6</sup>, a practical limit of conventional low temperature superconductor (LTS) magnets, including 45.5 T, the record high direct-current field. SuNAM and their collaborators built an 18 T 70 mm (RE)Ba<sub>2</sub>Cu<sub>3</sub>O<sub>7-x</sub> (REBCO, RE: rare earth) magnet that was *purchased* by the Institute for Basic Science (IBS) in Korea in October 2017<sup>7</sup> and has been continuously operated as a “user” magnet for axion detection experiment over 3 years. The IBS also purchased all-REBCO quadruple magnets from SuperGenics Co. Ltd., which are currently being installed in the IBS’s RAON accelerator site<sup>8</sup>. This may represent the first use of an HTS magnet for a large-scale national accelerator facility. In fact, applications of HTS magnet are rapidly expanding beyond laboratory magnets to fusion<sup>9-11</sup>, high energy physics<sup>12-15</sup>, biochemistry<sup>16-21</sup>, biomedical diagnosis<sup>22-27</sup>, renewable energy<sup>28-31</sup>, electric propulsion<sup>32-35</sup> and more<sup>36-41</sup>.

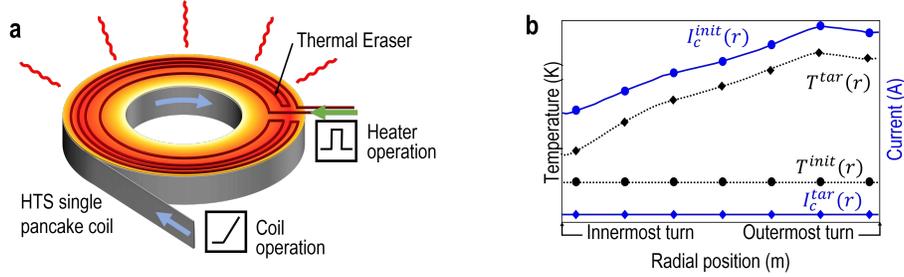
In every superconducting magnet, both HTS and LTS, it is well-known that “screening current” is always induced in nominal operation and even upon a quench. The *screening current* usually jeopardizes spatial uniformity and temporal stability of magnetic field due to the so-called *screening current induced field* (SCF)<sup>42</sup>. Recently, its detrimental impact on conductor mechanical damage was also reported and named as *screening current induced stress* (SCS)<sup>1</sup>. In general superconducting magnets wound with multi-filament superconducting wires experience marginal SCF and SCS, while an HTS magnet wound with essentially single filament conductor such as REBCO experiences substantially larger SCF and SCS, which often leads to failure in reaching the target field and/or permanent mechanical damage of the magnet. Thus, a technique to mitigate *screening current* is crucial for the development of the next generation high field HTS magnets.

To date, multiple techniques have been reported for mitigation of *screening current*<sup>43-47</sup>. Among them, there is an idea to temporarily increase the operating temperature of an HTS magnet “on purpose” in order to lower the overall critical current of the magnet. Motivated by this approach, we propose a more advanced technique, named “Thermal Eraser”, where *local* temperatures of individual turns of an HTS magnet are optimally controlled using a customized heater in a way to create a spatially designated temperature profile and consequently manipulate local critical currents of individual turns. In this paper, we first introduce the key concept of the Thermal Eraser. Then a test coil with a customized heater is designed, constructed, and

operated at temperatures ranging 7 - 40 K under a conduction cooling environment. Experimental results are compared with simulated ones, which validate the feasibility of our Thermal Eraser approach. Lastly, the discussion is followed with a focus on the discrepancy between experiment and simulation results. And some practical considerations to apply the Thermal Eraser to actual user magnets are also discussed.

## Key concept

Thermal Eraser is a customized heater for an HTS coil creating target (*designated*) spatial temperature distribution to manipulate local critical currents of individual turns. Figure 1a shows a key concept of Thermal Eraser. The basic mechanism in mitigation of *screening current* for a given HTS test coil is to: 1) design and construct a customized heater (Thermal Eraser, dark red heater wires in Fig. 1a) that creates a *designated* spatial temperature distribution (color gradient ranging red to yellow) in the coil (grey); and 2) install the customized heater in the test coil and operate in a way to reduce the local critical current of individual turns of the coil in a *pre-designed* pattern. Figure 1b presents an example of local temperature and critical current distributions at each turn of a coil, where  $T^{init}$  and  $I_c^{init}$  are, respectively, initial temperature and critical current distributions before activation of the Thermal Eraser and  $T^{tar}$  and  $I_c^{tar}$  are, respectively, target temperature and critical current distributions after activation of the Thermal Eraser. In most HTS magnets,  $T^{init}$  may be assumed to be spatially uniform during a nominal steady-state operation. The key design philosophy is to “control” the spatial distribution of  $T^{tar}$  in a way to make  $I_c^{tar}$  to be lower than  $I_c^{init}$  and spatially uniform in an ideal case. As a result, the spatial pattern of  $T^{tar}$  becomes similar to that of  $I_c^{init}$  but not completely identical, mainly because the field and temperature dependency of critical current of HTS must be also considered in design of Thermal Eraser.  $r$  in Fig. 1b is defined as the radial position of each turn in the coil.



**Figure 1.** (a) A schematic drawing to present the key concept of Thermal Eraser. A customized heater (dark red lines) is placed on top of an HTS single pancake coil (grey). When activated, it creates a *designated* temperature profile (red to yellow color gradient). Each rectangular icon indicates operation scenario for the HTS coil and the Thermal Eraser, respectively. Blue and green arrows stand for current flows in the HTS coil and the Thermal Eraser, respectively. (b) An example of local temperature and critical current distributions at each turn of a coil, where  $T^{init}$  and  $I_c^{init}$  are, respectively, initial temperature and critical current distributions before activation of the Thermal Eraser and  $T^{tar}$  and  $I_c^{tar}$  are, respectively, target temperature and critical current distributions after activation of the Thermal Eraser. The key design philosophy is to “control” the spatial distribution of  $T^{tar}$  in a way to make  $I_c^{tar}$  to be lower than  $I_c^{init}$  and spatially uniform in an ideal case.

## Design

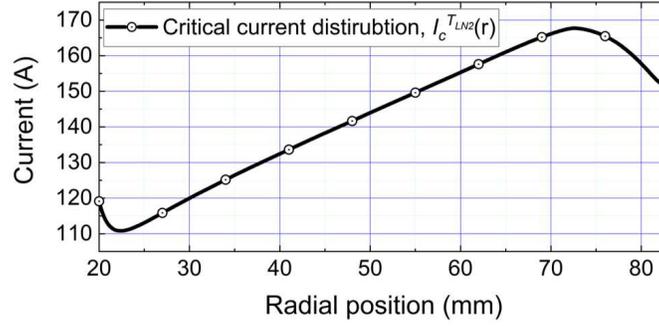
The first step in design of Thermal Eraser is to obtain  $I_c^{tar}(r)$  for a given HTS coil. Once the dimensions, operating current, and initial operating temperature of a target HTS coil are given, magnetic fields within the coil can be obtained in a numerical way, e.g., finite element method (FEM). In this paper, we consider: (1) dimensions of the given HTS coil provided in Table 1; (2) operating current of 50 A; and (3) the field and temperature-dependent critical current information,  $I_c(B, T)$ , obtained from a previous literature<sup>48</sup>. To avoid an unexpected quench, we aim at 50% reduction of *screening current induced field* (SCF) at the magnetic center of the coil and then consequently determine  $I_c^{tar}(r)$  of the coil with activation of the Thermal Eraser. Provided that the critical current is proportional to temperature at a given magnetic field<sup>43,49</sup>,  $T^{tar}(r)$  can be analytically calculated with:

$$T^{tar}(r) = T^{init}(r) + [I_c^{init}(r) - I_c^{tar}(r)] \cdot \left[ \frac{T_c - T_{LN2}}{I_c^{TLN2}(r) - I_c^{Tc}(r) \approx 0} \right], \quad (1)$$

where  $T_{LN2}$ ,  $T_c$ ,  $I_c^{TLN2}(r)$ , and  $I_c^{Tc}(r)$  stand for, respectively, liquid nitrogen temperature of 77 K, the critical temperature of 92 K, the critical current distribution in a given HTS coil at 77 K and a given magnetic field, and the critical current at the critical temperature (essentially zero). Measurement based  $I_c^{TLN2}(r)$  is provided in Fig. 2.

**Table 1.** Key parameters of test coil and Thermal Eraser

<b>NI HTS test coil</b>		
REBCO wire manufacturer		SuNAM
Tape width;thickness	[mm]	4.1;0.14
Inner and outer radii	[mm]	20;83
Total number of turns		450
Operating current	[A]	50
Self-inductance	[mH]	19.0
Characteristic resistance	[ $\mu\Omega$ ]	126
Time constant	[s]	150
Magnet constant	[mTA <sup>-1</sup> ]	6.4
<b>Thermal Eraser</b>		
Material		SUS310
Inner and outer radii	[mm]	61;80
Number of heating lines		10
Interval between two adjacent lines	[mm]	1
<b>NI HTS coil ↔ Thermal Eraser electromagnetic interaction</b>		
Mutual-inductance	[nH]	700

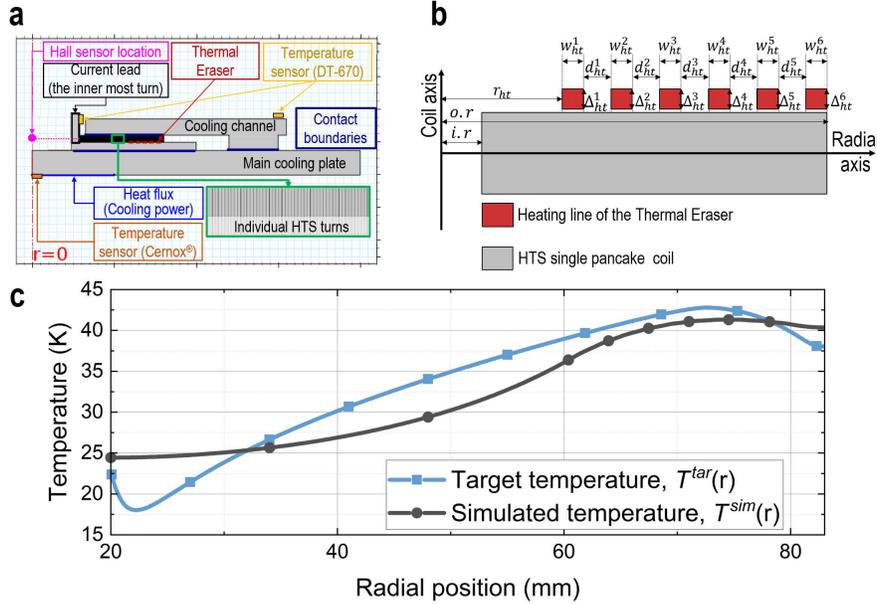
**Figure 2.** Critical current distribution in the given coil at liquid nitrogen temperature of 77 K considering the operating current of 50 A and measured  $I_c(B, T = 77K)$  data<sup>48</sup>.  $I_c^{init}(r)$  can be calculated with the provided critical current distribution by considering  $T^{init}(r)$  and the proportional relationship between temperature and critical current.

The second step is to build a time-dependent numerical simulation model for implementing the  $T^{tar}(r)$  in the given coil with multiple heating lines in a practical way. We use the COMSOL Multiphysics (thermal+electromagnetic) FEM tool to design and analyze the Thermal Eraser. The actual dimensions of our in-house conduction cooling facility are considered in the COMSOL model together with temperature-dependent material properties of key components. Figure 3a presents a to-scale 2D axisymmetric COMSOL model that includes the conduction cooling stage, the HTS test coil, Thermal Eraser and instrumentations. The well-known  $H$ -formulation with the domain homogenization technique<sup>50–52</sup> with the *power-law critical state* model for the  $E - J$  constitutive law of REBCO<sup>53</sup> is adopted for numerical simulation of *screening current* in the coil.

The last step is to optimize the Thermal Eraser design. As shown in Fig. 3b, key design variables are: (1) the number of heating lines (six in Fig. 3b); (2) the distance between adjacent heating lines ( $d_{ht}$ ); (3) width ( $w_{ht}$ ) and thickness ( $\delta_{ht}$ ) of each heating line; and (4) the radial position of the innermost heating line ( $r_{ht}$ ). The objective function to be minimized is defined as:

$$f^{obj} = \int |T^{sim}(r) - T^{tar}(r)| dr, \quad (2)$$

where  $T^{sim}(r)$  is the spatially distributed temperature within the coil, which is calculated during iteration of the COMSOL simulation. The genetic algorithm is adopted for optimization. For design simplicity, we adopt additional design constraints: (1)  $d_{ht}$  of the entire heating lines is identical; (2)  $w_{ht}$  and  $\delta_{ht}$  are set to be 1 mm and 0.1 mm, respectively; (3) the Thermal Eraser is activated for 1 minute with an operating current of 1 A; and (4) total resistance of the Thermal Eraser (material: stainless steel 310) is 25  $\Omega$  in consideration of our in-house power supply rating. The design optimization results are summarized in Table 1. Figure 3c presents a comparison between the final  $T^{sim}(r)$  and  $T^{tar}(r)$ , which shows reasonably good agreement. The average of  $|T^{sim}(r) - T^{tar}(r)|$  is  $\sim 3$  K.



**Figure 3.** (a) A to-scale 2D axisymmetric COMSOL model that includes the conduction cooling stage, the HTS testcoil, Thermal Eraser and instrumentations. (b) A schematic 2D axisymmetric drawing to show key design variables of Thermal Eraser. (c) Comparison between  $T^{tar}(r)$ , the analytic calculation results from (1), and  $T^{sim}(r)$ , the COMSOL simulation results.

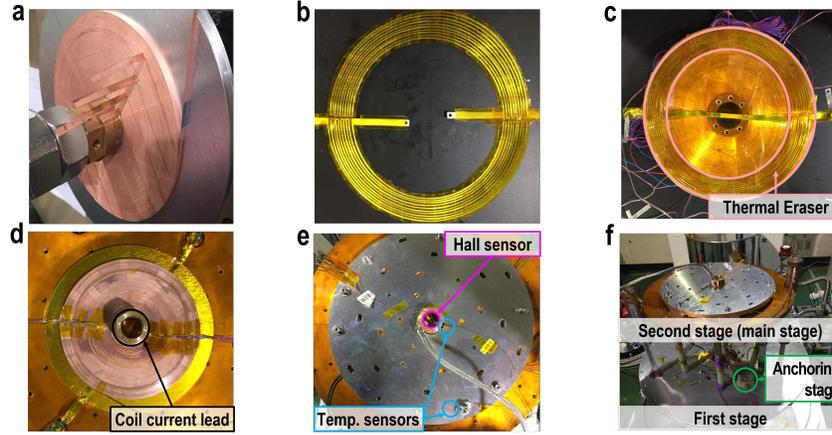
## Construction and instrumentation

In the construction phase, an HTS single pancake test coil was fabricated with the no-insulation (NI) winding technique incorporated<sup>54</sup>. To measure local voltages and temperatures of the coil, multiple short pieces of REBCO tapes were inserted as voltage taps at every 100 turn. After the test coil construction, key operation parameters including characteristic resistance of the coil (the sum of all contact resistances), time constant, and magnet constant (magnetic field at the coil center with operating current of 1 A) were measured in a liquid nitrogen bath at 77 K, and the results are summarized in Table 1. The Thermal Eraser was electrically insulated with the Kapton sheet of 100  $\mu\text{m}$  thick.

As for the instrumentation, Table 2 summarizes details of selected instruments, which include each device's resolution. Extra care was devoted to precisely estimating the range of each signal, as the magnitude of *screening current* in an HTS coil is often marginal. Figure 3a shows the locations of Cernox<sup>®</sup> and silicon diode (DT-670) temperature sensors, and Hall sensors (HGCA 3020). As the reference temperature point for thermocouple sensors, the first stage of our in-house conduction cooling system was used as an anchoring stage. Our data acquisition (DAQ) system consists of SCXI 1000, 1125, and 1305 of the National Instruments, while a nano-voltmeter was used to improve the measurement accuracy of magnetic fields. Two types of power supplies were used, one with a small current drift for the test coil operation and the other with a fast on-off switching speed (maximum 1.3 KHz) for the Thermal Eraser operation. Figures 4a–c show the construction process in detail, while Figs. 4d–f show the instrumentation process.

**Table 2.** Specifications of instruments for the feasibility test of Thermal Eraser

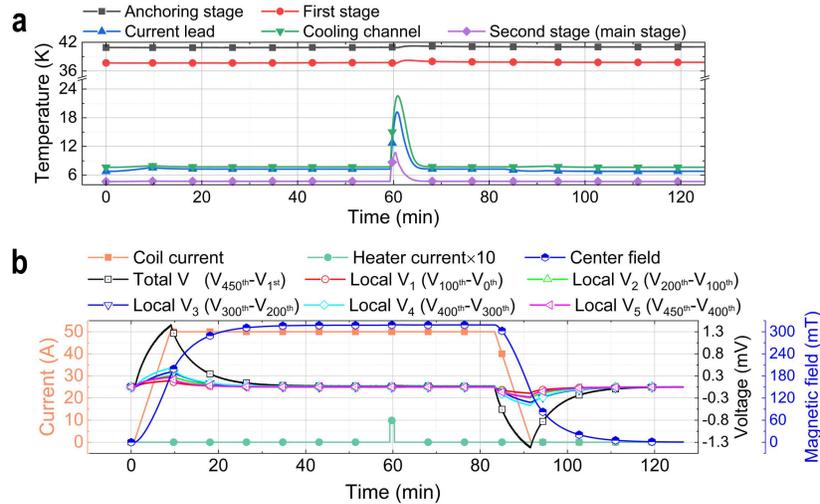
Name	Model	Range	Remarks
Temperature sensor I	Lake Shore Cernox <sup>®</sup>	0.10 – 325 K	$\pm 3$ mK at 4.2 K
Temperature sensor II	Lake Shore DT-670	1.4 – 500 K	$\pm 10$ mK at 77 K
Temperature sensor III	Lake Shore Thermocouple E type	3.0 – 475 K	$\pm 1$ K at 10 K
Magnetic field sensor	Lake Shore HGCA3020	$> 3$ T	$\sim 1.1$ G/ $\mu\text{V}$ at 4.2 K
Data acquisition	National Instruments SCXI system	-5 – 5 V	$\pm 10$ nV at range 100mV
Nano-voltmeter	KEITHELY 2182A	-100 – 100 mV	$\pm 10$ nV
Gaussmeter	Lake Shore Model 425	350 mG – 350 kG	$\pm 0.1$ G at 3.5 kG
Power supply I (NI HTS coil)	Oxford MercuryiPS	-10 – 10 V / -240 – 240 A	$\pm 2$ mA
Power supply II (Thermal Eraser)	PowerTM EX 300-12	0 – 300 V / 0 – 12 A	100 mV / 10 mA



**Figure 4.** (a) Winding an NI HTS test coil and inserting pieces of REBCO tapes for REBCO taps, (b) fabricating the customized heater, (c) assembling Thermal Eraser and coil, (d) installing heater current supply lines, thermocouple wires, and voltage signal lines, (e) locating a Hall sensor and temperature sensors, and (f) final assembly.

## Results and discussion

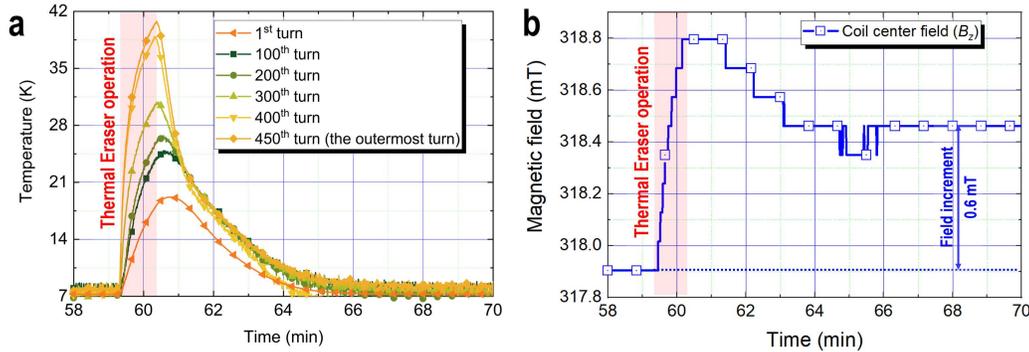
The test coil system including the HTS coil and the Thermal Eraser was tested at 7 K in our in-house conduction cooling system. The test coil was energized up to 50 A with the constant ramping-rate of  $0.1 \text{ As}^{-1}$ , and the Thermal Eraser was activated after sufficient time interval (typically more than 10 minutes) in consideration of the charging delay of an NI HTS coil<sup>54</sup>. Figure 5 shows experimental results. In Fig. 5a, the peak temperature variation during charging ( $0 < t < 60$  minutes, i.e., before activation of Thermal Eraser) was marginal (0.2 K), which may validate our assumption on the spatially uniform distribution of  $T^{init}$ . As shown in Fig. 5b, there is no discernible local voltage change during the Thermal Eraser operation as expected, mainly due to the marginal mutual inductance of 700 nH between the Thermal Eraser and the test coil.



**Figure 5.** Experimental results. (a) Temperatures measured by Cernox<sup>®</sup> and DT-670 sensors, and (b) currents, voltages, and the magnetic field at the coil center. The heater current represents ten times the actual operating current of the Thermal Eraser. Negligible temperature change of 0.2 K was observed before activation of the Thermal Eraser, while remarkable variation during the Thermal Eraser operation. The notable voltage variation by the Thermal Eraser was not measured due to weak mutual-coupling.  $V_n - V_m$  indicates the local voltage difference between  $n^{th}$  and  $m^{th}$  turns.

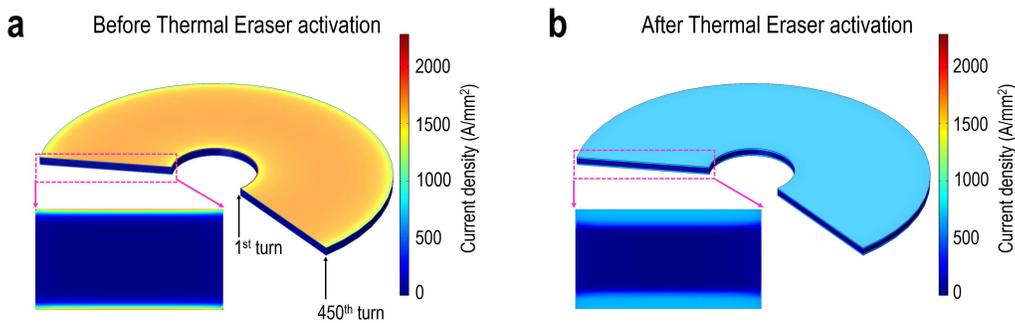
Figure 6 provides local temperatures at the radial location of selected turns and the coil center field under the operation of the Thermal Eraser. As shown in Fig. 6a, the local temperatures at 1<sup>st</sup>, 100<sup>th</sup>, 200<sup>th</sup>, 300<sup>th</sup>, 400<sup>th</sup>, and 450<sup>th</sup> turns (the outermost

turn), were initially uniform at 7 K. They rose to 18, 24, 26, 30, 39, and 40 K, respectively, at the time when the Thermal Eraser activation is terminated. Figure 6b shows the measured coil center fields ( $B_z$ ).  $B_z$  is 317.9 mT before activation of the Thermal Eraser and 318.5 mT after. To confirm that this field increment is not originated from the temperature-dependent measurement error of the Hall sensor,  $B_z$  was continuously measured until the temperature of the test coil returned back to its initial value of 7 K. Finally,  $B_z$  settled to 318.5 mT. The magnetic field increment by the *screening current induced field* (SCF) reduction of 0.6 mT was captured. Provided that the calculated SCF at the beginning of activation of the Thermal Eraser is 1 mT, it is concluded that our proposed Thermal Eraser reduces 60% of SCF.



**Figure 6.** (a) Spatially-distributed temperature in the NI HTS test coil. The local temperatures at 1<sup>st</sup>, 100<sup>th</sup>, 200<sup>th</sup>, 300<sup>th</sup>, 400<sup>th</sup>, and 450<sup>th</sup> turn (the outermost turn), were initially uniform at 7 K. They rose to 18, 24, 26, 30, 39, and 40 K, respectively, at the time when the Thermal Eraser activation is terminated. (b) Measured magnetic field at the coil center ( $B_z$ ).  $B_z$  is 317.9 mT at the beginning of activation of the Thermal Eraser and rises to 318.8 mT during the activation, but this field eventually saturated to 318.5 mT. Therefore, it is concluded that SCF reduction of 0.6 mT is captured by the Thermal Eraser activation.

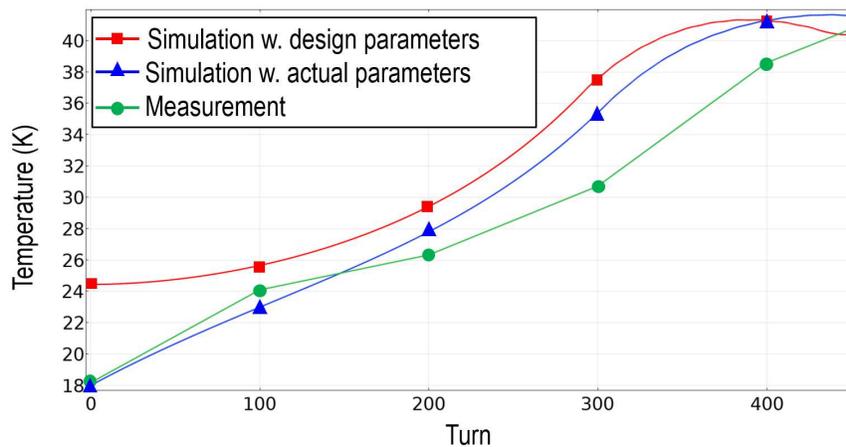
We performed COMSOL simulation with the actual parameters of the test coil and the Thermal Eraser. Figure 7 compares the spatial distribution of total current density (i.e., transport and screening): (a) before activation of the Thermal Eraser; and (b) after. The peak values of current density before and after activation of the Thermal Eraser are, respectively, 2200  $\text{Amm}^{-2}$  and 700  $\text{Amm}^{-2}$ . The coil center field,  $B_z$ , before the activation is calculated to be 317.8 mT, while it increased to 318.3 mT after the activation. When the *screening current* is not considered,  $B_z$  is calculated to be 318.8 mT. The measured SCF reduction of 0.6 mT agrees reasonably well with the calculated one of 0.5 mT, which may validate our simulation approach as well as the effectiveness of the Thermal Eraser to mitigate the *screening current* and the consequent SCF.



**Figure 7.** Spatial distribution of the total (transport + screening) current density in the given test coil: (a) before activation of the Thermal Eraser; (b) after. The maximum values of current density before and after activation are, respectively, 2200  $\text{Amm}^{-2}$  and 700  $\text{Amm}^{-2}$ . Due to the Thermal Eraser activation, the *screening current* and the consequent SCF are alleviated. And the calculated SCF reduction of 0.5 mT agrees reasonably well with the measured one of 0.6 mT.

Figure 8 shows temperature profiles along each turn of the test coil at the moment when the Thermal Eraser is turned off at  $t \approx 60$  min. Red squares represent simulated ones with the *designed* parameters of the Thermal Eraser, while green circles represent measured ones. The difference between the simulated and measured results is mainly due to: (1) the manufacturing errors of the Thermal Eraser; and (2) the different operating conditions from the ideal ones expected in the design stage. We

re-simulated the temperature profile with the *actual* dimensions and operating conditions of the Thermal Eraser considered in COMSOL: (1) the actual operating temperature of 7 K rather than 10 K assumed in the design stage; (2) the increment of the inner and outer radii of the Thermal Eraser by 2 mm (i.e., 61 and 80 mm in the design → 63 and 82 mm actual, respectively); and (3) the actual resistance of the Thermal Eraser of 20  $\Omega$ , while 25  $\Omega$  assumed in the design stage. Blue triangles in Figure 8 shows the simulated temperature profile with the *actual* parameters of the Thermal Eraser, which shows reasonable agreement with those measured ones (green circles). Note that the marginal difference between the designed and actual parameters of the Thermal Eraser rather largely impacts the performance of the Thermal Eraser.



**Figure 8.** Simulation and measurement results of local temperatures in the given HTS coil at the time when the Thermal eraser activation is terminated. As the actual parameters are considered, the average difference between simulation and measurement results is reduced from 3.5 K to 1.8 K.

## Conclusion

Here we introduced the “Thermal Eraser”, a customized heater that is dedicated to mitigating *screening currents* induced in a high-temperature superconductor (HTS) coil. The key idea of the Thermal Eraser is to create a (*designated*) spatial temperature distribution in a way to manipulate local critical currents of individual turns of the HTS coil. For the feasibility demonstration of the Thermal Eraser, we designed and constructed the Thermal Eraser and an HTS single pancake test coil. After the construction and instrumentation of the test coil system, Thermal Eraser and HTS test coil operated at temperatures ranging 7 - 40 K under a conduction cooling environment. After the test coil was energized up to its operating current of 50 A with a constant ramping-rate of  $0.1 \text{ As}^{-1}$ , the Thermal Eraser was activated for 1 minute with the operating current of 1 A. By activation of the Thermal Eraser, we measured spatial temperature distribution in the test coil at selected turns. Although there was a small difference between measured and designed temperature distribution, the measurements showed good agreement with the designed ones. The consequent magnetic field increment by the Thermal Eraser activation at the coil center was also measured. The magnetic field at the coil center was 317.9 mT at the beginning of activation of the Thermal Eraser and increased to 318.5 mT eventually. From the result, we concluded 0.6 mT increment of the magnetic field was captured which is due to the reduction of *screening current*. The measured SCF reduction value agreed reasonably well with the calculated value of 0.5 mT which is calculated using COMSOL Multiphysics, a commercial finite element method program. Finally, we discussed an issue regarding some practical considerations of the Thermal Eraser by providing comparison results between calculation and measurement results in terms of spatially distributed temperatures; a marginal difference between the designed and actual parameters of the Thermal Eraser rather significantly impacts the spatially distributed temperature variation originated by the Thermal Eraser operation. This paper delivered a viable option for HTS magnets to efficiently mitigate highly non-uniform current densities with Thermal Eraser, a hardware-based optimal temperature control approach. We believe that it could play a key role in mitigating detrimental effects originated from *screening current* in HTS user magnets.

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## **Author contributions statement**

J.B. designed, fabricated, and tested the integrated high temperature superconducting system consisting of a high temperature superconductor coil and Thermal Eraser, and edited the manuscript; J.K. supervised experiments of the integrated high temperature superconducting system operation; J.T.L., G.K., J.P., S.H.P., and S.N. reviewed the manuscript; S.H., in addition to supervising the work, proposed the concept of optimal temperature control with the use of a customized electric-heater, drafted the first version, and subsequently edited J.B.'s drafts. All authors have read and agreed to the manuscript.

## **Competing interests**

The authors declare no competing interests.

## **Additional information**

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