

The first family of application-specific integrated circuits for programmable metasurfaces

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Abstract

Reconfigurable metasurfaces are man-made surfaces, which consist of sub-wavelength periodic elements - meta-atoms - that can be reconfigured to manipulate incoming electromagnetic waves. However, reconfigurable metasurfaces developed to-date, have limitations in terms of impedance range, reconfiguration delay and power consumption. Also, these systems are costly and they require bulky electronics and complex control circuits, which makes them unattractive for commercial use. Here, we report the first family of CMOS application-specific integrated circuits (ASICs) that enable microsecond and microwatt reconfiguration of complex impedances at microwave frequencies. Our approach utilizes asynchronous digital control circuitry, with networking capabilities, allowing simple and fast reconfiguration via digital devices and user-friendly software. Our solution is low-cost and can cover arbitrary metasurfaces, with different sizes and shapes.

Main Text

Metasurfaces are electrically thin composite materials that are composed of periodically spaced, sub-wavelength meta-atoms. These composite materials have gained the interest of many researchers, due to their ability to demonstrate novel functionalities, such as perfect absorption¹⁻⁶, anomalous reflection⁷⁻⁹, beam shaping¹⁰, and more.

Reconfigurable metasurfaces have also been demonstrated by incorporating various tunable elements within the meta-atom. Electrical tunability has been obtained using varactor diodes^{11,12}, complex-impedance integrated-circuit (IC) loading elements³⁻⁶, liquid crystals¹³ and power amplifiers¹⁴. Besides electrical tunability, other means of tunability have been demonstrated, such as magnetic¹⁵ and optical¹⁶ tunability. Optically tunable behavior has also been shown by utilizing the optical properties of PDR1A¹⁷, which has been shown to possess a memory effect¹⁸.

Recently, programmable metasurfaces have emerged^{14,19-25}. These are tunable metasurfaces that control individual meta-atom states, through software. Often, the control of each meta-atom is binary and is implemented through a field-programmable gate array (FPGA) development board^{19,21,25}. An increase in meta-atom state was achieved by incorporating digital-to-analog converters between the FPGA and the tunable elements of the meta-atom^{14,20,22,23}. With the individual meta-atom control, programmable metasurfaces have demonstrated multifunctional applications e.g. polarization, scattering and focusing control¹⁹, multi-focal spot control²⁰, holography²¹, imaging²³, non-linear harmonic manipulation²² and even beam steering while controlling the harmonic power level²⁴.

The advanced electromagnetic manipulation that programmable metasurfaces possess has made them an attractive solution for future wireless telecommunications. A recent study²⁶ showed that improved wireless connectivity can be achieved by incorporating metasurfaces in telecommunication systems. Even though this technology is still in its infancy, basic experimental verifications of simplified telecommunication systems based on programmable metasurfaces were shown^{27,28}.

Although the incorporation of programmable metasurfaces in wireless telecommunication systems can provide a clear advantage over traditional MIMO implementations and transceiver architectures^{27,28}, there are major drawbacks that need to be addressed before they can be adopted. In particular, such programmable metasurfaces need to be cost-effective, scalable, low-power and low-noise. It is apparent that having FPGAs feeding discrete shift registers, to drive multiple digital-to-analog converters, that finally bias multiple power-hungry varactor diodes will not provide a solution that is reliable, cost-effective, scalable, low-power and low-noise.

To address all of these requirements, major upgrades in the programmable metasurface architecture need to be implemented. In this paper, we present the first family of application-specific integrated circuits (ASICs) designed for programmable metasurfaces, which satisfy all these requirements. The family of ASICs presented in this work, incorporate in a single die an asynchronous control circuit, multiple digital-to-analog converters and multiple complex impedance tunable elements.

Metasurface ASIC Characteristics

The ASICs utilize an asynchronous methodology for the control circuit to reduce noise and increase speed, while simultaneously consuming less power²⁹, when compared to traditional clocked systems. The digital-to-analog converters' eight-bit resolution provides fine adjustment of the low-power complex impedance loading elements³. Four complex impedance loading elements are implemented in each integrated circuit and can be individually addressed to provide more flexible control over the metasurface meta-atoms. As was shown in simulations^{3,30}, we are able to control the amplitude and phase of the reflection coefficient for both polarizations, independently and simultaneously.

By having a low-noise, low-power, and fast asynchronous control circuit we are able to control the instantaneous amplitude and phase response of the meta-atom in real-time. Integrating all the electronic components into one package reduces the cost and size, and increases their performance, making them ideal for programmable metasurface designs which require a large number of electronic elements.

Circuit architecture and implementation

The manufactured ASICs, along with their architecture and the measured results of their sub-components are displayed in Fig. 1. The integrated circuit family is formed by six similar mixed-signal designs shown in Fig. 1a. Each ASIC version is optimized for a nominal center frequency and with a different tunable impedance range to provide additional flexibility, to cater for various metasurface designs. Detailed measurements of each one of the six ASIC versions can be found in the Supplementary Information Notes 1.

The internal architecture of the foundational ASIC is overlaid on the physical layout in Fig. 1b, to illustrate the correlation between the physical layout and the architecture. The architecture consists of four loading elements, eight digital-to-analog converters and a control circuit. Each loading element utilizes a MOSFET varistor and a MOSFET varactor to adjust the real and imaginary part of the impedance, respectively, while simultaneously having negligible static power consumption. Eight-bit digital-to-analog converters are used to finely tune the varistor and varactor of each loading element of the ASIC. The control circuit has two main operations. The first is to be part of a network grid that will send/receive data packets to/from neighboring nodes in order to store the appropriate payload in its memory. The second is to provide the necessary digital inputs to the digital-to-analog converters, and in turn to tune the complex impedance of the corresponding meta-atom.

The configuration of the chip can be achieved using an external digital device e.g. FPGA or microprocessor. Each chip can also communicate and exchange packets with other chips from this chip-family. This way, we can form an array of chips with networking capabilities embedded in the metasurface structure. Further extending this idea, we can have one chip per meta-atom of a metasurface and be able to programmatically adjust its impedance via software. With our low-power design, we can power metasurfaces of a few square meters using only batteries, which may be recharged using energy scavenging methods³¹. Also, the chip is a standalone device i.e. there is no need for any other external component on the metasurface, thus keeping the cost to a minimum. Although the idea is simple and effective, we faced some constraints due to the implementation at microwave frequencies and the manufacturing processes.

The ASICs were implemented in a mainstream CMOS 0.18 μm semiconductor technology, that balanced cost per die, mixed-signal capabilities, RF characteristics as well as low-power digital circuit capability. Our proposed chips can realize reconfigurable metasurfaces and adjust the complex loading impedance of each meta-atom individually. Depending on the application and metasurface design, a large number of chips are required⁴. These could amount to thousands of chips for a one square-meter metasurface, thus chip cost is a critical factor. Wafer Level Chip Scale Packaging (WLCSP) technology was selected because it enables both better RF performance, given bond wire parasitics and variations are eliminated, as well as lower cost per chip. The diameter of the solder-ball spheres and the pitch of the balls were chosen to be 250 μm and 400 μm , respectively. Smaller solder spheres and smaller pitch sizes are available, but this increases the printed circuit board (PCB) costs, on which the metasurface is patterned. For smaller pitch sizes, special PCB processes are required and the reliability decreases. Therefore, the balls and pitch were kept at a size to comply with widely available high-frequency laminate PCB manufacturing design rules. The size of the ASICs was chosen to be 2.2 mm \times 2.2 mm to increase their yield and subsequently reduce their cost. The size of the chips and pin pitch subsequently dictated the number of available input/output (I/O) pins to be twenty-five. The size of the ASIC and the pin limitation add constraints to the whole architecture. The number of available loading elements were chosen to be four and this dictates the number of digital-to-analog converters, and subsequently the control circuit's complexity, communication, and control scheme. Due to the pin limitation, we were forced to adopt a serial communication scheme between the chips.

The control circuit uses asynchronous circuits and communicates via handshake. Synchronous digital circuits are by far predominant in control circuit designs, however to maximize the ASIC usability for various metasurface designs and to avoid all issues associated with the clock tree synthesis of synchronous digital systems, we opted to go the asynchronous route²⁹. A synchronous digital system would require a clock tree with scalability adjustments and would have to satisfy the requirements of flexible metasurfaces and walls of irregular shapes. In addition, the clock skew would have to be well controlled to eliminate any setup and hold violations. Addressing all these with a synchronous digital system would require a static system with scalability limitations. By using asynchronous digital circuits, the scalability became as simple as connecting meta-atoms or tiles of metasurfaces together. Once the wires are connected, the network can operate without requiring any modifications or optimizations.

Power consumption is also minimized by using the asynchronous circuit approach. At static conditions, the asynchronous control circuit consumes only leakage current whilst the synchronous counterpart would consume both static and dynamic current, at every clock cycle. Specialized circuitry and techniques can be adopted to turn off certain parts of the chip when not needed, but still the buffers of the clock tree would be enabled. Also, the available area for the control circuit is limited due to the small size of the chip and such techniques would consume a significant amount of our free space allocated for the digital-to-analog converters and the loading elements.

The last major advantage from the asynchronous circuit approach, is related to the significantly reduced levels of electromagnetic emissions (EMI) that are generated during programming³². A synchronous approach generates significant amounts of broadband noise during switching activity, given all transitions will happen at the same time. This will create problems for metasurface absorber³⁻⁵ applications, given that the surface will be radiating EM waves at all times. This is not the case in our control circuit because the noise generated is both lower and more evenly spread timewise, since only the chips that exchange data are enabled, while the rest are idle.

The performance of the control circuit from the manufactured chips was evaluated and the results are presented in Fig. 1c. Each control circuit has sixty-four storage cells connected in a series configuration, and has eight cells allocated per digital-to-analog converter. Thus, the packet length is sixty-four bits and the total number of different states per chip is 2^{64} . Neighboring chips (sender and receiver in Fig. 1c) communicate via handshake and respect the 4-phase dual-rail

asynchronous protocol, whereby each bit is represented by two signals ('data.true' and 'data.false') and there is also the acknowledge signal ('data.ack') which declares the end of each cycle.

Table 1 Chip Characteristics	
Technology	0.18 mm CMOS Mixed-Signal RF 1P6M
Supply Voltage (core and IO)	1.8 V
Die Size	4.84 mm ²
Package Type	WLCSP
Number of memory cells	64
Bit Rate	68 MBits/s
Energy Consumption per Bit	79 pJ
Packet Frequency	1 MHz
Energy Consumption per Packet	5.1 nJ
Static Power Consumption	328 mW
Digital-to-Analog Converter range	0-1.793V
Digital-to-Analog Converter resolution	7 mV/bit

A detailed explanation of the 4-phase dual rail protocol can be found in the Supplementary Notes 2. Due to the 4-phase dual-rail asynchronous nature of the circuits, the ASIC's configuration time is not dependent on the data packet content. The fastest configuration time per chip is measured to be around 1 ms. Fig. 1c shows the signals exchanged at the channel between the communicating chips. The static power consumption of the chip is 328 mW. The energy consumed per bit exchanged is 79 pJ/bit and the energy consumed per chip configuration is 5.1 nJ/chip considering the delays of the buffer stages and the PCB tracks between the chips. These results imply that a configured metasurface consisting of a few thousand meta-atoms with one chip per meta-atom, would consume power on the order of a few milliwatts, easily provided by small-sized batteries. The reconfiguration is performed with a user-friendly software, as described in Supplementary Information Notes 3. Furthermore, in a few milliseconds, we can change the configuration data of each meta-atom individually and apply one of the 2^{16} values for each of the four available loading elements per chip. The chip characteristics and measured performance are summarized in Table 1.

Our digital-to-analog converter is based on a two-stage resistor string architecture, with a resolution of eight bits. The advantages of this architecture are its accuracy, monotonicity, and its small layout. Also, it can connect directly to the loading elements since its output impedance is much lower than the controlling input impedance of the varistors and varactors. Fig. 1d shows the output voltage for each of the 256 binary inputs.

The loading element design methodology was reported in our previous work³, along with an example metasurface design. The loading elements are designed utilizing MOSFET components but for the sake of simplicity the circuit is simplified to a parallel connection of a varactor and a varistor as shown in the architecture of Fig. 1b. The resistance and capacitance values of the loading elements are tuned with the V_r and V_c voltages, respectively. These voltages are the output of the digital-to-analog converters, as shown in the ASIC architecture (Fig. 1b). The loading element's measurements for design version 4 are plotted in Fig. 1e on a Smith chart. For a particular frequency, an area on the

Smith chart is outlined where the loading element can be operated. This area is formed by controlling the input code of the two digital-to-analog converters that bias the loading element at the V_r and V_c nodes. The measured area perimeter is plotted with a dashed red line at 3 GHz. Additionally, the frequency dependency is illustrated by including plots from 2 GHz to 6 GHz for the four corners of the plotted area. Sample points are also plotted at 3 GHz to illustrate the ability to obtain intermediate states in the plotted area.

In summary, Fig. 1 highlights the six ASICs of the chip-family used for programmable metasurfaces. The ASICs are asynchronous and can be programmed in about 1 ms with an asynchronous 4-phase dual-rail asynchronous protocol. Within the ASIC, eight digital-to-analog converters are programmed to bias the four complex impedance loading elements. The presented ASIC architecture increases the EM manipulation capabilities of the meta-atom by providing independent programmability to four locations within the meta-atom. The meta-atom can be programmed in three dimensions, meaning control over the resistance, capacitance and in time. The ASICs can form a network without the need for any external power-hungry and bulky components e.g. external digital-to-analog converters, shift registers and crystal oscillators. In addition, they consume micro-Watts of power which is an order of magnitude improvement over existing programmable metasurface designs.

Applications and Future Prospects

The presented family of ASICs is expected to drive a new generation of programmable metasurfaces that are ready to be incorporated into future telecommunications systems, but which can also be retrofitted into current systems. The programmable telecommunication environment, as described in work by C. Liaskos et al.²⁶ is shown in Fig. 2a, where metasurfaces are used to improve the throughput and the security of indoor telecommunication systems. Furthermore, they are expected to improve outdoor telecommunication systems in multi-user environments (Fig. 2b) by incorporating metasurfaces within base stations, thus improving their adaptive multibeam capabilities. The family of ASICs is a key component in future metasurface-enabled telecommunications systems, where multifunctional performance has been demonstrated by incorporating ASICs onto various metasurfaces³⁻⁶. An example of such a metasurface design can be seen in Fig. 2c and Fig. 2d. The ASICs are populated on the back of the metasurface, as can be seen in the insert of Fig. 2c, and a simple square-patch periodic design has been used for the textured top side of the metasurface, seen in the insert of Fig. 2d. In this design, the meta-atom is defined as the four-square patches loaded by the ASIC. With the advanced capability of tuning both the amplitude and phase of the reflection coefficient, the example designs were able to perfectly absorb an incident wave up to oblique angles of incidence for both transverse electric and transverse magnetic polarizations³⁻⁶. This has been further extended by Kossifos et al.³ to absorb both polarizations simultaneously and independently, as shown in Fig. 2e. Anomalous reflection and polarization rotation were also demonstrated^{5,6} (Fig. 2f), but even as is, these functionalities are only a fraction of what the ASIC-equipped programmable metasurface can achieve. By controlling the amplitude and phase of each meta-atom at a sub-wavelength scale, more complex functions of the metasurface design can be achieved, such as multi-beam patterns, absorbing from one direction while reflecting in another, fine control of polarization, and non-linear reflection.

For example, multi-beam or even arbitrary beam shaping to suit the needs of a telecommunication system in a multi-user and multi-objective environment could be achieved, as shown in Fig. 2b. Additionally, the advanced functionalities of such metasurfaces can be adopted in reduced radar-cross-section (RCS) applications, stealth technology, and even cloaking. Furthermore, programmable metasurfaces also find applications in holography, which use the amplitude and phase programmability that such metasurfaces can provide. The functionalities described above only control the metasurface in two dimensions, engaging only amplitude and phase control with a slow or static operation in time. The family of ASICs utilizes fast asynchronous control circuits, which can be programmed within approximately 1 ms. Thus, the programmable metasurfaces can also quickly and accurately reconfigure their amplitude and phase response

in time. For example, for a series of 100 chips used in a typical metasurface, the programming time would be approximately 100 ms, which also incorporates the time delay of the high-speed communication lines that connect the ASICs. This ability is particularly useful, since modulation of arbitrary beam shaping can be obtained, and thus the metasurface can control not only the propagation of electromagnetic energy within its environment, but also the information that the electromagnetic wave contains.

Programmable metasurfaces are expected to reciprocally co-evolve with telecommunication systems in the near future. Similarly, the ASICs presented are expected to evolve to satisfy the growing need for low-power and low-cost electronics tailored for programmable metasurfaces. The metasurface trend will require that future ASICs will operate even faster and with wider programmable loading element ranges. Thus, technologies with smaller features are expected to be used in order to reduce the size of the chips and to increase their speed. Additionally, more exotic technologies that include memristors and/or micro-electromechanical switches will be utilized in the loading elements to increase their range. Furthermore, as silicon-germanium and gallium arsenide technologies become more affordable they will find their way into future ASICs for metasurfaces.

Conclusions

We have developed a family of low-cost, low-power, high-speed scalable ASICs for complex impedance adaptation at microwave frequencies. The ASICs can form networks on metasurfaces that can be programmed via software to control the complex impedance of each loading element in time and in space. This can be translated into a variation of the amplitude and phase response of both the reflected and transmitted waves for both TE and TM polarizations. This is due to the multi-bit resolution of the four loading elements per ASIC, which form the meta-atoms comprising the metasurface. Furthermore, each meta-atom can be individually addressed, without interfering with the incoming electromagnetic waves. This is due to the asynchronous operation of the control circuit, that leads to low electromagnetic noise emissions. Even with these additional functionalities, each member of the ASIC family requires only microwatts for its static operation. The performance of the chips highlights the potential of using ASICs for realizing programmable metasurfaces. Our work is a leap forward towards the development of real-time programmable metasurfaces that can be integrated into indoor/outdoor telecommunication systems. It also paves the way for the development of metasurfaces for use in extraordinary applications that previously seemed infeasible, such as cloaking of not only static but also moving objects, moving holograms, dynamic manipulation of incoming signals and many more.

Methods

Chip fabrication and packaging. The dies were fabricated in a commercial 0.18 mm CMOS process technology. They were then retrieved by a third-party company for packaging using the Wafer Level Chip Scale Package (WL CSP) technology, forming each individual chip used in this work. This approach minimizes the parasitics added to the input nodes due to the wire bond connections of typical packages. The solder balls used are lead-free SAC405 solder spheres.

PCB fabrication and population. The PCBs used for testing the chips were designed in-house and fabricated using a commercial PCB manufacturing technology. Each PCB board was populated with one chip. The use of via-in-pad technology was used to connect to the chip pads due to the very small pitch of the pads (0.4 mm). Each board had specific connections available to form an array of PCBs/chips, enabling the testing of various network topologies. The entire metasurface PCB was fabricated using a custom PCB manufacturing technology.

Experimental Setup. All measurements were performed at room temperature in a controlled environment with ESD protection. During the communication measurements, an OPAL KELLY XEM6010 module that uses a Xilinx Spartan-6 FPGA was used for providing data to the system. A custom graphical user interface was developed to easily construct the input packets and visualize the input/output signals. For power consumption measurements, a Keithley 4200 SCS was used to provide power to the chips and measure the current drawn by the system. To visualize the response at high frequencies, the Tektronix MSO70604C mixed-signal oscilloscope was used. For maximum speed measurements the Digilent Digital Discovery module was used, which also uses the Xilinx Spartan-6 FPGA. The responses of the loading elements were measured using a Keysight N5227B four-port vector network analyzer. The PCBs used for the measurements, along with the de-embedding PCBs were designed on a Rogers 4350B substrate. The measurements were de-embedded using the well-known through-reflect-line method.

Declarations

Data availability

The data that support the plots within this article and other findings of this study are available from the corresponding authors upon reasonable request.

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Author contributions

L.P and K.K designed the circuits and performed the experiments. M.A. and J.G. provided overall supervision and guidance. All authors discussed the results and reviewed the manuscript.

Competing interests

The authors declare no competing interests.

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Figures

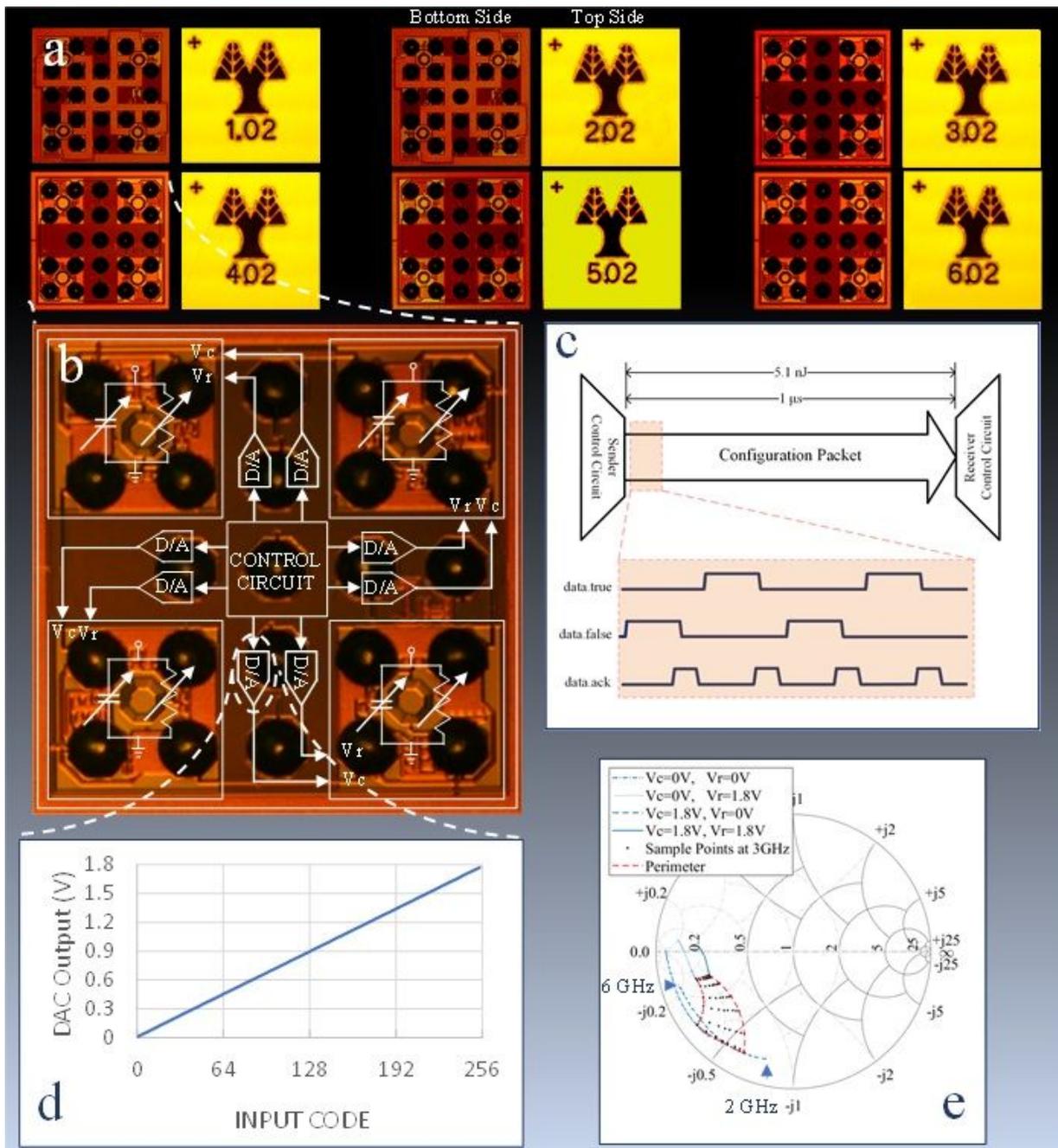


Figure 1

a, Integrated circuit microphotographs of the ASIC family, showing both top and bottom sides. b, Bottom view of integrated circuit (version 4) with overlaid architecture. c, Measurements of asynchronous configuration packet. d, Measurements of a digital-to-analog converter. e, Measurements of the integrated circuit loading element.

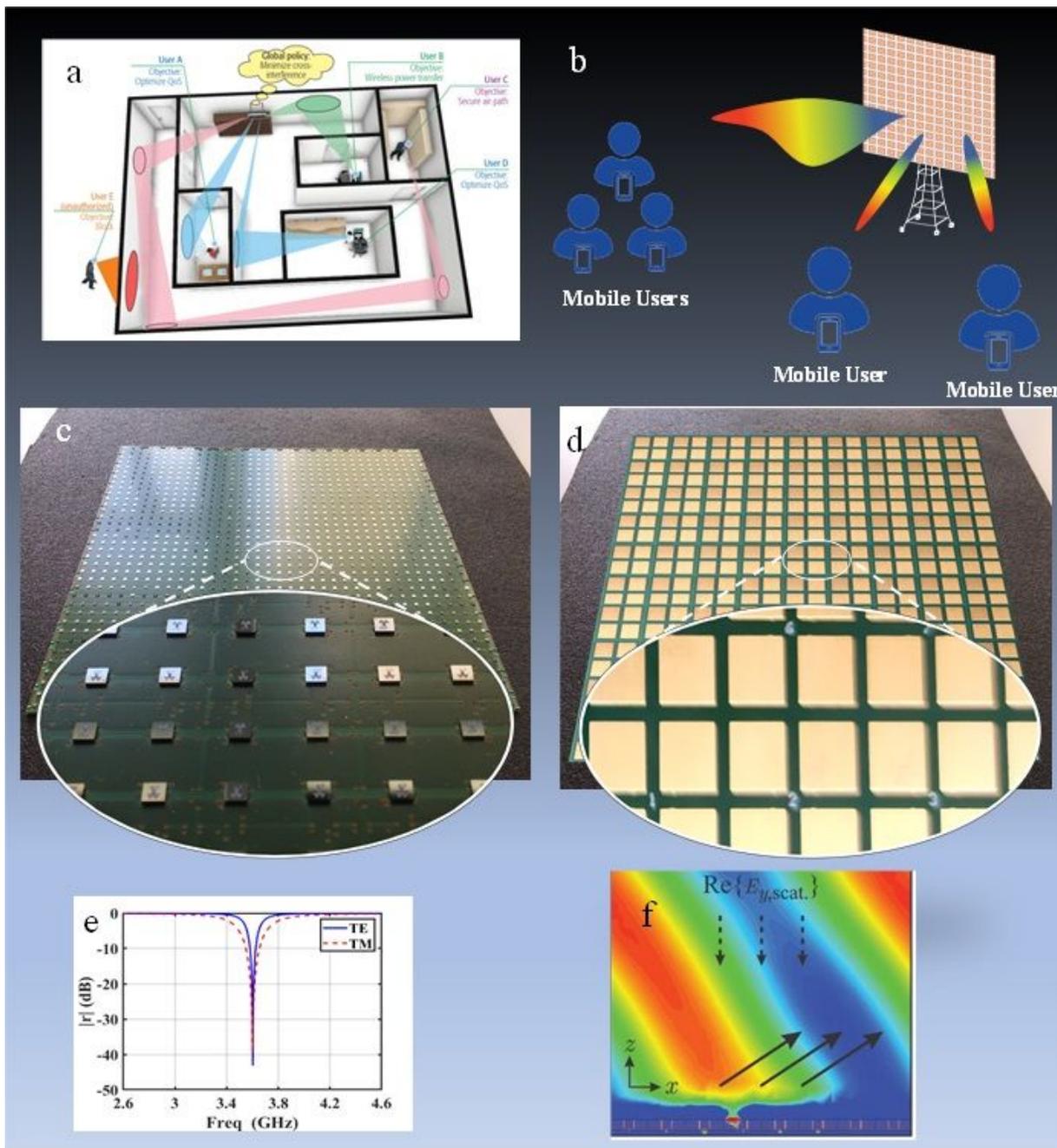


Figure 2

Potential applications of the family of ASICs in telecommunication systems. Illustration of: a, A metasurface based indoor telecommunication system²⁶ and b, A metasurface improving base station systems with multiuser communication. Example metasurface design as reported in 4,5 c, Side where the integrated circuits are populated d, Periodically textured side. Example capabilities of metasurface designs e, Simultaneous dual-polarization perfect absorption³ and f, anomalous reflection⁵.

Supplementary Files

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- [SupplementaryInformationThefirstfamilyofapplicationspecificintegratedcircuitsforprogrammablemetasurfaces.pdf](#)