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Design of Heterojunction Tunnel Field-Effect Transistors with SiO₂ isolation between Source and Drain for Low Power Application

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Abstract—This paper presents a numerically simulated Ge-source based Tunnel Field Effect Transistor with (TFETs) SiO₂ segregation between the channel and drain. The developed device has been compared with conventional TFET and without isolated heterojunction TFET. The use of oxide segregation between channel and drain enhances the performance of the device in terms of ON-state current as well as subthreshold swing (SS). The electrical characteristics such as surface potential, electric field, transfer characteristics, output characteristics of the proposed device have been studied. The temperature variation of the proposed device has also been studied. The proposed device offers high ON current of 3×10^4 A, I_{ON}/I_{OFF} ratio of $\sim 10^{11}$ and enhanced SS of 30 mV/dec. The validity of the proposed device has been done by Synopsys Sentaurus TCAD.

Keywords— Tunnel Field Effect Transistor; Subthreshold Swing; Heterojunction; Band-to-band Tunneling; Silicon-on-insulator.

Declarations

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I. INTRODUCTION

The escalation of technologies and the rising miniaturization of electronic devices like smartphones, tablets, sensor networks, etc., has been making Internet of Things (IoT) an important innovation in the current scenario of an information-based society. IoT connects everything and makes daily lives better, and becomes essential for the future of the world. Some of the facets that are particularly relevant to explain the acceleration of IoT technologies, i.e., the dimension of the devices, ability of the device to be integrated in the real world, the ability of the device for computational and memory capacities, etc. On that account, the development of device technologies is necessary to get the final objective of real and big-scale IoT applications [1-2]. The low power specially low stand-by power is the most essential requirement for devices in IoT application [3].

In device technology, further scaling in the nanoscale MOS devices faces numerous issues like threshold voltage roll-off, short channel effects, non-scalable SS, etc.[4]. Today's technology needs new and novel device designs that use carrier transport which achieves lower subthreshold swing (SS) and simultaneously suppresses the short channel effects (SCEs)[5]. Many emerging device concepts are investigated, such as Tunnel Field Effect Transistor (TFET) [5-8], FinFET [9], Silicon Nanowire Field-Effect Transistor [10], Carbon Nanotube Field-Effect Transistor [11-12], where technology boosters like high-k dielectric materials, channel engineering, gate engineering, bandgap engineering, oxide engineering, etc. has been applied.

Among various emerging devices, TFETs, based on the band-to-band tunneling (BTBT) mechanism, have proven to be promising device in terms of lower OFF current, SS below 60 mV/dec, unsusceptible toward SCEs, and suitable for low power high speed switching devices [13-14]. TFET has a significant issue of low ON than conventional MOSFETs current[15], however, heterojunction TFET has been widely studied in recent years due to the possibility of overcoming low ON current, bipolarity, high threshold, etc[16-18].

In this work, we proposed a heterojunction TFET with SiO₂ isolation between source and drain of gate length 50 nm at $V_{DS} = 0.4$ V. The proposed device is compared with conventional TFET and Ge- source TFET without isolation. The proposed device offers high ON current of 3×10^4 A, I_{ON}/I_{OFF} ratio of $\sim 10^{11}$, and enhanced SS of 30 mV/dec, respectively. The impact of temperature has also been studied to show the reliability of the reported device.

II. TUNNEL FIELD EFFECT TRANSISTOR

In this section, the basic overview of TFET in terms of the device structure, operating principle, and physics has been discussed. It has already been revealed from various studies that TFET works by interband tunneling mechanism. The electrons as charge carriers transfer from one energy band into another band at a heavily doped $p^+ - i - n^+$ junction, as shown in Fig. 1(a).

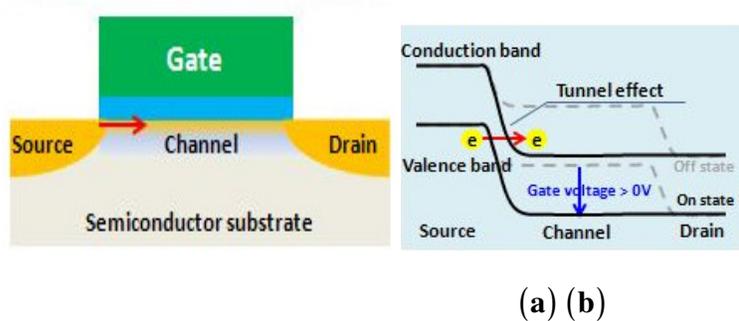


Fig. 1. (a) Conventional structure of TFET (b) device principle of the TFET, where dotted gray lines indicate the off state and black solid line on state [19].

In the ON-condition of TFET, the gate voltage (V_G) carriers are tunnel into the channel through the potential barrier, based on BTBT. In the OFF-condition of TFET, the channel barrier is large, so there is no flow of current. Practically, not zero due to the thermal distribution of carriers, as shown in Fig 1(b). Only the P-I-N diode leakage current flows between the source and drain, and this current can be extremely low [19].

III. HETEROJUNCTION TUNNEL FIELD EFFECT TRANSISTOR

In the past few decades, several researchers have been working for effective gate control and enhancing tunneling probability of heterostructure TFET by using different device engineering such as gate engineering, tunneling barrier engineering, spacer engineering, gate engineering, etc. [7]. The fundamental difference between the homojunction and heterojunction TFET, as shown in Fig. 2. It is clear from the figure that both homojunction and heterojunction TFET have been designed with asymmetrical doping of the source and drain so that it acts as reverse-biased gated p-i-n diodes. Keeping these points in mind, our work has been based on heterojunction TFET [20-21]. In this section, the physics of the heterojunction TFET has been discussed and compared with homojunction TFET.

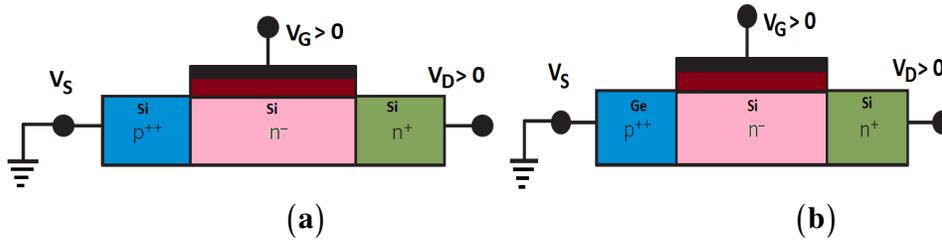


Fig. 2. Schematic view of (a) homojunction TFET (b) heterojunction TFET.

The energy band diagram for homojunction and heterojunction is shown in Fig. 3. The advantage of heterojunction TFET over homojunction TFET is clear from the figure.

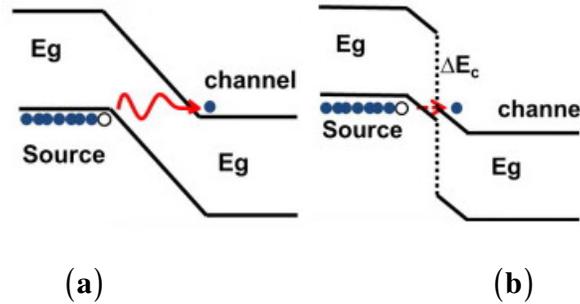


Fig.3 Tunneling barrier engineering of (a) homojunction TFET (b) heterojunction TFET for on-condition current.

The tunneling barrier (T_b) is large and gives low ON current, which is one of the disadvantages of convention TFET, as shown in Fig. 3 (a).The T_b has been reduced using heterojunction, which enhances the tunneling current, as shown in Fig. 3(b).

IV. ARCHITECTURE OF PROPOSED DEVICE

The proposed device is a Ge-source based Tunnel field-effect transistor (TFET) with SiO_2 isolation between source and drain. The proposed structure (D1) has been compared with a silicon-based TFET without SiO_2 isolation (D1) and a Ge-source-based structure without SiO_2 isolation (D2), as shown in Fig. 4.

For all the three TFET designs, the source, drain, and channel have been doped with $1e20$, $1e19$, and $1e15$, respectively. The gate length is 50 nm and is made up of polysilicon. The length of source and drain are 20 nm each, respectively. The dielectric is 1nm thick and is made off high-k dielectric named HfO_2 . A box structure made up of SiO_2 is place to provide

isolation between source and drain. The problem with a Si-based design was low ON current, ambipolarity, and leakage current. To address these problems, the source has been replaced with germanium as it has higher ON current, as well as less ambipolarity. The various optimized parameters used for the proposed device are listed in the Table I.

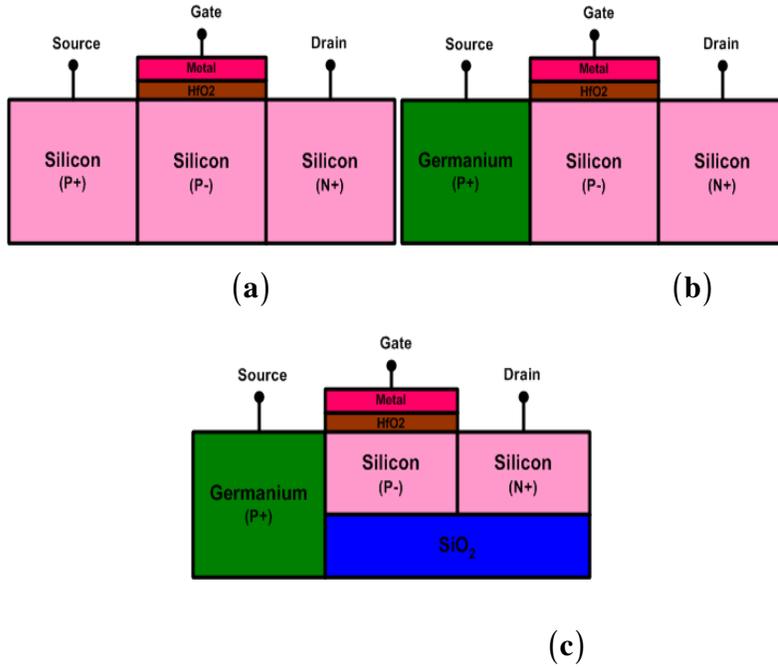


Fig. 4. Cross-sectional view of the (a) conventional TFET (D1)(b) Ge-source TFET without SiO₂ isolation (D2) (c) Ge-source TFET with SiO₂ isolation (D3).

Table I: Optimised device parameters

Parameters	Value
Channel Length	50 nm
Length of source	20 nm
Length of drain	20 nm
Thickness of the channel	15 nm
Thickness of the source	25 nm
Thickness of the drain	15 nm
Thickness of the SiO ₂	10 nm
Length of the SiO ₂	70 nm
Source doping	$1 \times 10^{20} / \text{cm}^3$
Channel doping	$1 \times 10^{15} / \text{cm}^3$
Drain doping	$1 \times 10^{19} / \text{cm}^3$
Gate work function	4.1 eV

First of all, the TCAD simulation data of the reported device have been calibrated against the experimental data of reference [21] at drain voltage 0.5V as shown in Fig. 5. It is observed that there is a good matching of both data, which certify the validity of the selected models.

In this part The comparison between all the devices D1, D2, and D3 has been made at fixed $V_{DS} = 0.4$ V, as shown in Fig. 6. For the D1 device, the ON current and OFF current are low, whereas the threshold voltage is high compared to D2 and D3. For the D2 device, the ON current and threshold voltage has been enhanced as compared to D1. In comparison to D1 and D2, in every aspect, the simulated results of device D3 show better performance in terms of ON current, threshold voltage, I_{on}/I_{off} ratio, and SS.

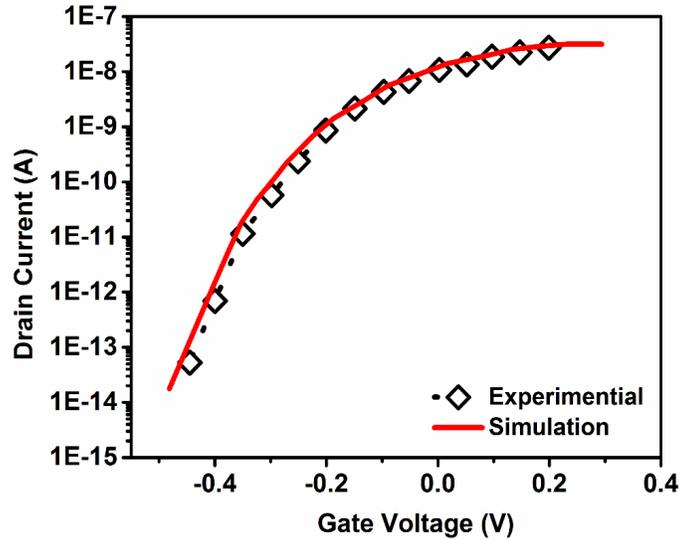


Fig. 5. Calibration of TCAD simulation set up of proposed device with experimental data of reported paper [21].

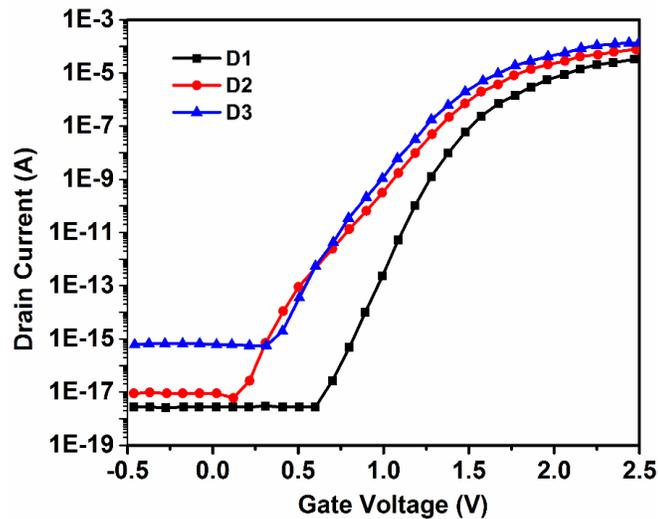


Fig. 6. Drain current vs. gate voltage at $V_{DS} = 0.4$ V for conventional TFET (D1), Ge-source TFET without SiO_2 isolation (D2), and Ge-source TFET with SiO_2 isolation (D3).

V. PROPOSED TUNNEL FET PROCESS STEPS

The proposed Ge-source-based TFET with SiO_2 segregation may be fabricated on a lightly doped p-type SOI wafer, as shown in Fig. 7. The following steps have been required for the possible fabrication of the proposed device.

- **Thermal Oxidation:** This technique has been used to scale down the SOI layer to 15 nm and then remove the grown oxide. The optical lithography and dry etching have been used to pattern the active area [21], as shown in Fig.7(a).
- **Atomic Layer Deposition:** This technique has been used to place the aluminium as gate (Al), Low-temperature- oxide (LTO) gate-hardmask, aluminium nitride as an interfacial layer, hafnium oxide as capping layer [22], as shown in Fig. 7(b).
- **Ion Implantation and Thermal Annealing:** Ion implantation technique has been used for masking, whereas thermal annealing has been used for heavy n-type impurity doping in the drain region [21].

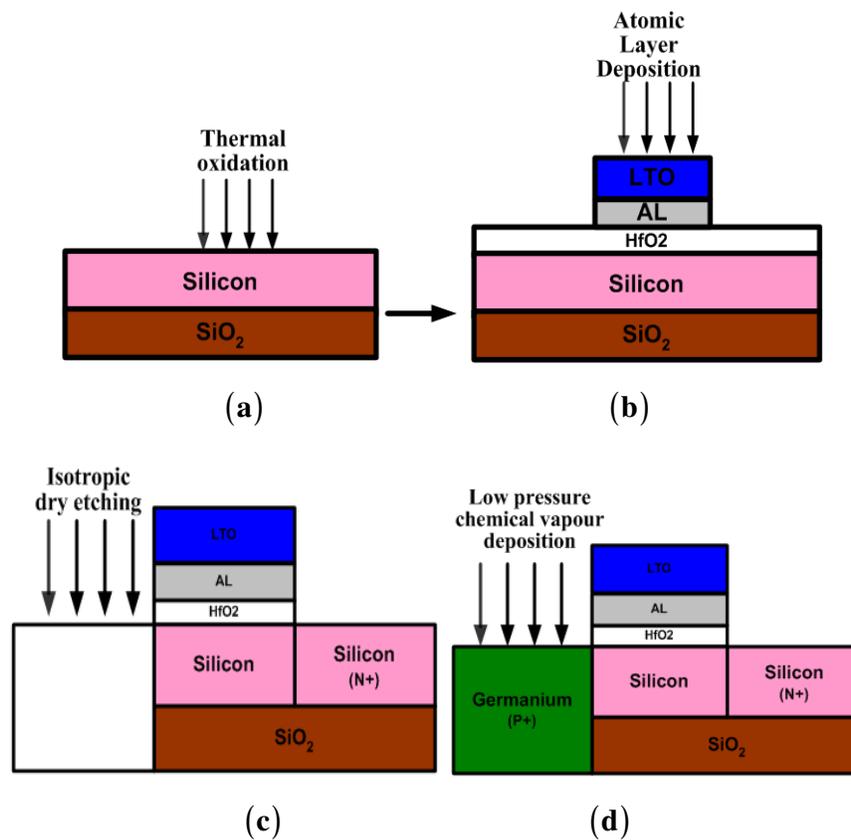


Fig. 7. The possible process steps used to fabricate the proposed device (a) Thermal oxidation (b) Atomic layer oxidation (c) Isotropic dry etching (d) Low pressure vapor deposition.

- **Isotropic Dry Etching:** This process has been used to recess silicon in the source area undercutting the gate electrode, as shown in Fig. 7 (c).
- **Low Pressure Chemical Vapour Deposition:** This Low Pressure Chemical Vapour Deposition (LPCVD) reactor has been used to deposit the boron doped germanium. To permit direct probing of the gate, source, and drain pads, an additional patterned and etched LTO layer has been deposited. At last, the gas annealing has been used to enhance contact resistance as well as the properties of the interface [22], as shown in Fig. 7(d).

VI. RESULTS AND DISCUSSION

This section has discussed and validated the proposed device's results using the Synopsys Sentaurus TCAD simulation tool. The non-local BTBT, Shockley–Read–Hall recombination, Auger recombination, Lombardi model, Fermi-Dirac model, bandgap narrowing model has been used for the TCAD simulation of the proposed device [23]. The non-local model has been used for BTBT of the charge carrier to get the accurate band to band tunneling rate at the junction of channel and source region. The recombination models named SRH and Auger has been used because of the high impurity atom concentration in the channel region. The Fermi-Dirac model has been used to determine and minimize the charge carrier concentrations. The concentration dependent mobility model (CONMOB) and electric field dependent mobility model (FLDMOB) and Lombardi model has been used as mobility models. The band gap is one of the important parameter, which decreases with doping concentration and directly influence the tunneling current. Due to this reason, bandgap narrowing model (BGN) has been used for highly doped source as well as drain region [23]. Fig. 8 shows the surface potential variation along with the channel position for different V_{DS} . In Here, the surface potential is calculated by the potential along with channel of the device at the Si-SiO₂ interface and the potential is computed in respect of source Fermi level.

Fig.9 shows the electric field variation from source to drain region for different gate voltages. In the ON condition of the device, the source doping will enhance the energy bands in source region and this decreases the tunneling barriers for electron as charge carrier to tunnel to the drain region. The increase in the electric field is observed due to a steep transition between energies of channel and source region. It is observed from figure that as the gate voltage

increases the electric field at the source-channel junction also increase due to the maximum number of charge carriers to tunnel through the junction [24].

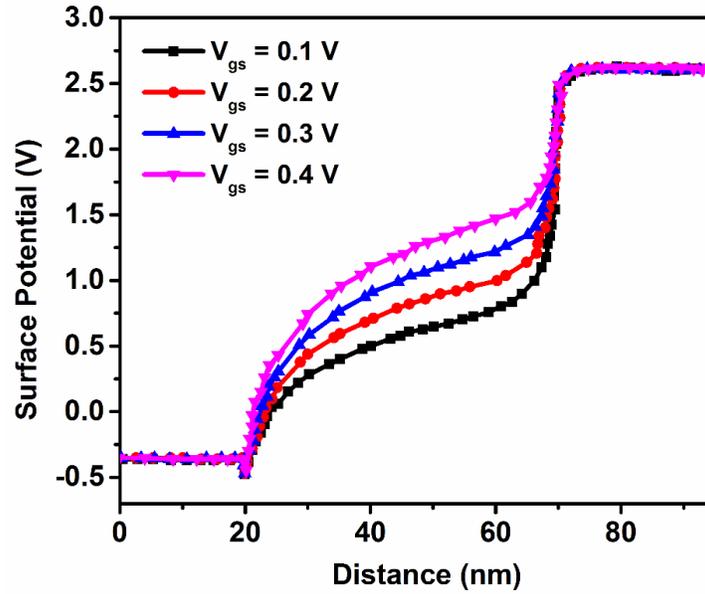


Fig.8. Surface potential vs. position of the channel for different gate voltages of the device.

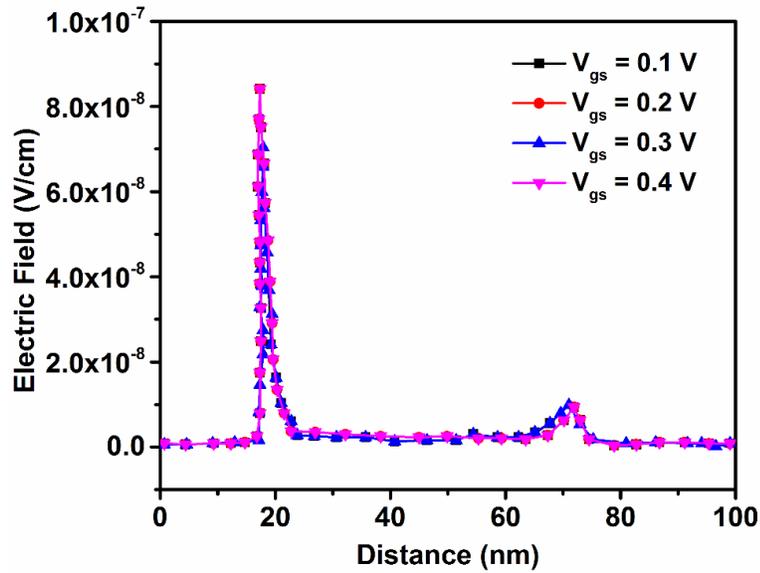


Fig. 9. Electric field vs. position of the channel for different gate voltages.

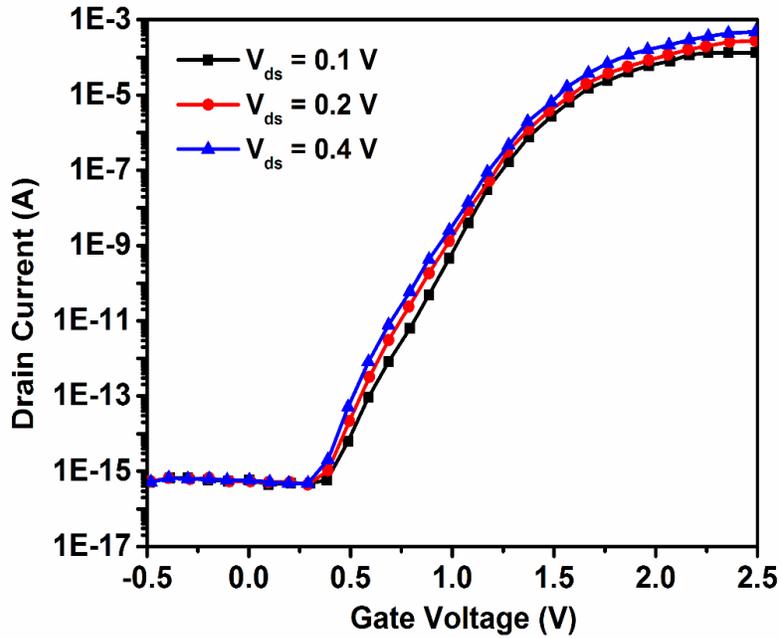


Fig.10. Drain Current vs. gate voltage for different drain voltages.

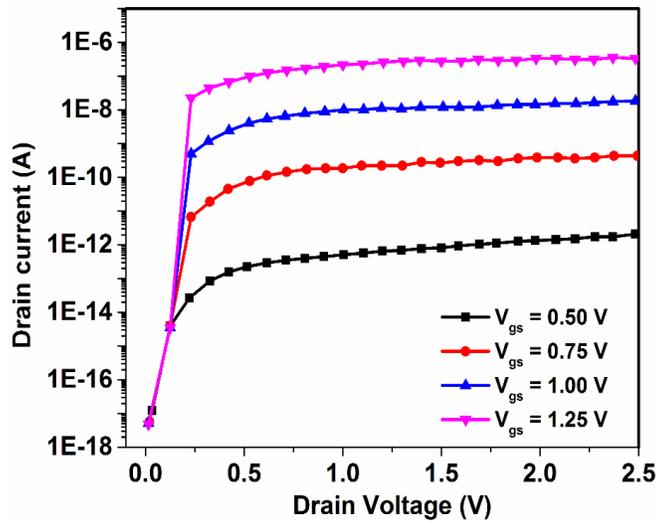


Fig.11. Drain Current vs drain voltage for different gate voltages of the proposed device.

Fig. 10 shows the drain current variation with respect to gate voltage variation for different drain voltage. The beauty of the reported device is that the slight increase of drain voltage and enhances SS, ON current, threshold voltage, I_{ON}/I_{OFF} ratio. Moreover, there is no ambipolarity as expected for the heterojunction devices. The output characteristic $I_{DS}-V_{DS}$ of the proposed device for different gate voltage V_{gs} is shown in Fig. 11. The tunneling barrier

decrease as the gate voltage increase and this enhance the drain current due to large number of electron passes from source region to channel region.

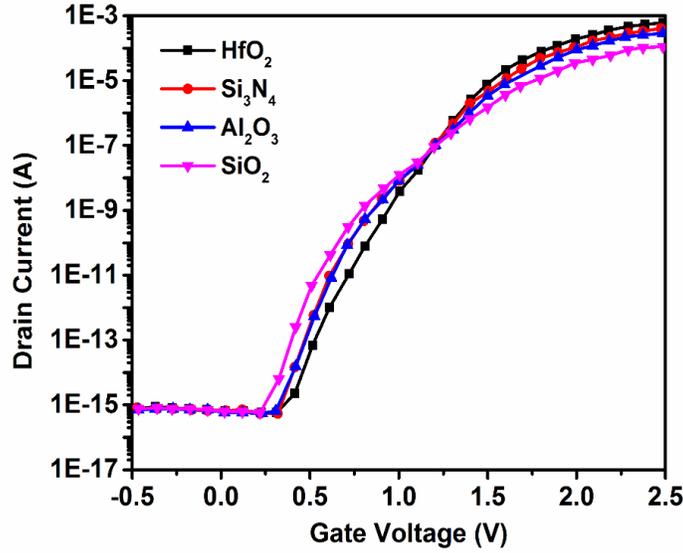


Fig. 12. Drain Current vs. gate voltage for different gate-dielectrics at drain voltages = 0.4 V.

The transfer characteristics for different dielectric materials is shown in Fig. 12. The dielectric constant value of SiO₂, Si₃N₄, Al₂O₃ and HfO₂ used for the reported device are 3.9, 7.5, 11, 22, respectively. The dielectric material with large dielectric constant decreases the equivalent oxide thickness (EOT) as well as the gate leakage. The reduced EOT increases the electric field at the source-channel junction and this is responsible for the enhancement of drain current. So we can say that the change in dielectric constant directly effect the ON current as well as SS of the device [25].

The drain current vs gate voltage for different temperatures is shown in Fig. 12. It will clear from the energy gap equation as it is the function of temperature and is given by [26-30].

$$E_g(T) = E_g(0) - \frac{\gamma T^2}{T + \beta}$$

where, γ (4.7×10^4 eV/K) and β (235 K) are the fitting parameters for Ge.

It is clear from the above equation that the energy gap depends on temperature. The drain current depends on the energy gap, so it also depends on temperature. The slight increase in ON current and SS has been shown in the figure. It is noticeable from the plot that OFF current increases for temperature variation, but it is below the ITRS requirement.

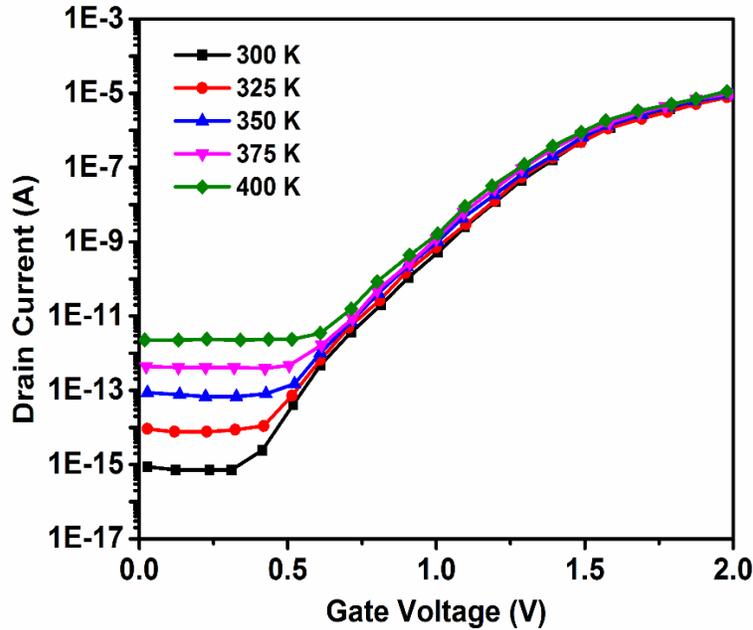


Fig.13. Drain Current vs gate voltage for different temperatures at drain voltages =0.4 V.

VII. CONCLUSIONS

In this work, a numerically simulated Ge- source-based TFET with SiO₂ segregation between channel and drain has been investigated for the low power applications. The analyzed device has been compared with conventional TFET and heterojunction TFET without segregation between channel and drain. The use of segregation amplifies the performance of the proposed device in terms of ON current, OFF current, SS and ambipolarity. The proposed device has also been analyzed with temperature variation. The proposed device has been validated by Silvaco Synopsys TCAD. The proposed device is a low power device and it is suitable candidate for low power digital applications. Moreover, in the current scenario of an information-based society, it can be used for Internet of Things (IoT) application.

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