Drain-Engineered Reconfigurable Transistor Exhibiting Complementary Operation

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Research Article

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Drain-Engineered Reconfigurable Transistor Exhibiting Complementary Operation

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***Abstract*—In this paper, we propose and simulate a multifunctional transistor that exhibits device reconfigurability and realizes both nFET and pFET electrical characteristics when adequately biased. The use of this device will significantly reduce the transistor count in realizing sequential and combinational circuits and will result in highly compact design. The device uses a dual fin structure having a single mid-gap workfunction gate (≈ 4.65 eV) alongside dual metal (metal-silicide) drain regions. It employs n^+/p^+-i junctions at the source-channel interface along with the Schottky junctions at the channel-drain interface. In practice, metal-silicides such as erbium/ytterbium silicide ($ErSi_x$/$YbSi_x$) for the n-drain and platinum silicide (PtSi) for the p-drain can be used as they provide smallest electron and hole Schottky-barrier heights (SBHs). Simulations carried out using calibrated parameters show better drive current (10^{-2}≈10^{-3} A/μm) compared to the quantum tunneling current in simulated state- of-the-art multifunctional devices (10^{-4}- 10^{-5}A/μm). In addition, butterfly curves show symmetric high (NM_H) and low (NM_L) noise margins of 0.43V and 0.29V for zero and finite SBHs, respectively. The switching characteristics is shown to have an overshoot of 0.15 V for realistic SBHs which is then eliminated for the case of zero SBHs. In the last section, it is also demonstrated that a simplified structure having single mid-gap workfunction (~4.65 eV) drain of Nickel silicide (NiSi) does not hamper the reconfigurability of the device.**

***Index Terms*—MOSFET, Multifunctional circuit, CMOS, Schottky junction.**

I. Introduction

For the past four decades, the primary technique used in the VLSI industry to keep Moore's law valid is the aggressive scaling of the MOSFET physical dimensions. This so far has resulted in high level of device integration and has given rise to integrated circuits (IC's) with high speed and density [1], [2]. However, as CMOS dimensions have entered into the nanometer regime, the ever-increasing short-channel effects (SCEs) along with the unscalable subthreshold slope (SS~60mV/dec) limit of the MOSFET [2], and similar current transport devices [3], [4], has resulted in a rapid rise in the leakage current. This increases the standby power consumption significantly, and in consequence, has imposed the limit on transistor integration alongside the switching speed [5].

Steered by the need to overcome the aforementioned limitations, various advanced device geometries including FD SOIs [3], III-V MOSFETs [5], FinFETs [6], nanowire FETs [7] have been proposed in the literature. Alternate current transport devices based on the band-to-band tunneling (BTBT) such as silicon based lateral/line Tunnel FETs [8]–[10], graphene based TFET [11], negative capacitance (NC) based nanowire TFETs [12] and electrostatically-doped source-drain TFETs [13] have also been explored. In addition, to overcome the doping limitations, DG architecture based on charge plasma concept [14], nanowire(NW) and nanosheet (NS) junctioless FETs [15]–[17] have also been heavily investigated. All these geometries have so far focused on achieving the increased performance out of the individual device unit alongside supply voltage (V_{DD}) scaling, whereas a few handful of them have tried to increase the device functionality instead [18]–[20]. In this regard, Si NWs based reconfigurable transistor that can be programmed dynamically by an external voltage were fabricated [21]. The NWs are undoped and are controlled by a dual Schottky junctions at the source-channel and channel-drain ends. In consequence, carrier injection (holes for pFET and electrons for nFET) can be modulated by keeping one gate voltage constant and other variable. Another device fabricated that exhibit reconfigurability is a vertically-stacked (VS) Si Gate-all-around (GAA) NW FET having control-gate (CG) and polarity-gate(PG) [22]. PG is kept constant which determines the mode and CG acts as a conventional gate in that particular mode. Earlier, a complementary device using a double-gate (DG) architecture based on a Schottky-barrier (SB) tunneling has also been demonstrated via simulations [19]; however, it has certain downsides: 1) the inherently low drive current associated with the SB FET; 2) the need of two individually tuned gate workfunctions for optimum device functionality; 3) the leakage due to the coupling between non-isolating channels during the pFET and nFET operation. Other than this, in terms of fabrication, complementary operation in a single device so far reported [19], [21]–[24] have been at the cost of high operating voltages (V_{DD} of ≥ 1.4V).

Most of the complementary devices are based on the Schottky tunneling based current injection mechanism; however, they inherently suffer from low drive current compared to conventional FET. To understand the reason for this, we revisited the fundamentals. For a silicide source, the emitted current density J_s is composed mainly of two components, i.e., the thermal emission J_{th} and the current due to quantum mechanical tunneling through the Schottky barrier J_{fe} (thermionic field-emission and field-emission current are clubbed together here for simplicity). At small V (gate voltage), J_s equals

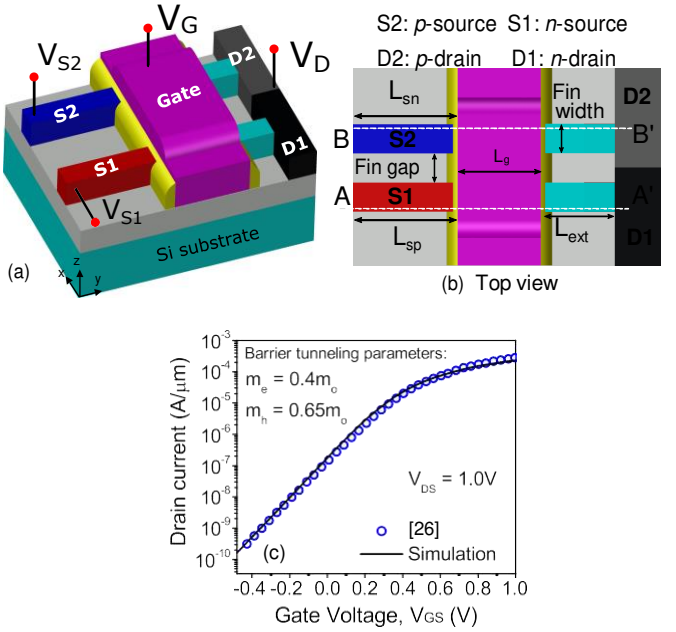

Fig. 1. (a) Bird's eye view of the proposed DE RFET schematic with terminals shown. (b) Shows the top view of the DE RFET having dual fins. Cutlines/Cutplanes AA' and BB' are drawn the fins. Simulation models were calibrated from fabricated the tri-gate SOI JLT [26] by matching the transfer characteristics. In addition, lateral tunneling parameters are taken from [27] to account for the OFF-state leakage.

J_{th}; however in the ON-state, when there is a high field, J_s is mainly dominated by the J_{fe}. So, unlike the conventional FET wherein current is controlled by the thermal-emission barrier in the channel, current in SB FET is limited by the tunneling barrier at the source [25]. For this reason, a low current drivability in SB FET is observed.

Keeping in view the above drawbacks, in this paper, a transistor exhibiting device reconfigurability is proposed and simulated and can also be biased in the inverter mode. The veracity of the complementary switching mechanism is envisaged using a dual fin design having doped *n*/*p* sources and metal (metal-silicide) as drains. The device is being termed as a Drain-Engineered Reconfigurable FET (DE RFET) due to the connected metal (metal-silicide) drains. It overcomes the low drive current originating from the quantum tunneling current J_{fe}, as present in the silicide-source SB FET architecture [19]. Additionally, the wrap-around gate architecture facilitates the path to volume inversion compared to that of a thin inversion layer in DG architecture.

Recently, we have also proposed a vertically stacked dual drain exhibiting reconfigurability [35] but its junctionless behavior demands complex doping strategy, and therefore, dual fin design mitigates this to some extent. The present work employs single gate and differs from [35] as it has double gate architecture. In addition, in the present work, the choice of single silicide drain having midgap workfunctin to simplify the device architecture is also proposed in the last section.

II. Device Structure

Fig. 1(a) and (b) shows a bird's eye view alongside the top view of the proposed DE RFET. Fin isolation width of 60nm is used to separate N-source (donor $N_D = 1 \times 10^{20}$ cm^{-3}) and P-source (acceptor $N_A = 1 \times 10^{20}$cm^{-3}) regions. Two silicon fins, controlled by a single gate, will contribute individually to the *n*/*p* sections of the device operation. Both the sections have an extended undoped channel length of L_{ext}. In addition, dual-connected *n*/*p* silicide drains of suitable workfunction, φ_{Dn} and φ_{Dp} (or SBH, Φ_{Dn} and Φ_{Dp}), are used to sink-in the electron and hole currents, respectively, during the *n*/*p* FET operations. All other device parameters are provided in the table I.

It is an arduous task to come up with a detailed process flow until the device has actually been fabricated. However, key processing possibly include: starting with an SOI wafer, the device island can be patterned with fins [28]. Next, gate dielectric can be thermally grown or deposited. After this, gate metal layer such as titanium nitride (TiN) can be deposited via chemical or plasma vapor deposition (CVD or PVD) and then patterned [29]. Next, silicon nitride gate-sidewalls spacers can be formed [28]. Thereafter, selective deposition of borosilicate glass (BSG) layer and phosphosilicate glass (PSG) layer, respectively, for *p*-type and *n*-type doping can be done, followed by the high temperature annealing process [29]. Selective deposition of near band-edge workfunction Pt metal for D2 and Er or Yb metal for D1 can next be done, followed by silicidation to form connected drains. Unreacted metals can be removed using wet chemical etch. Finally, metallization and chemical mechanical polishing (CMP) can be done.

III. Simulation Methodology

To have a proper Schottky junction at the channel-drain interface, complementary or near band-edge metal-silicides are required. The choice of workfunctions for the same are as follows :$\varphi_{Dn} < \varphi_{Si} < \varphi_{Dp}$ where $\varphi_{Si} = \chi_{Si} + E_g/2$, is the undoped silicon workfunction; χ_{Si} is the electron affinity (4.05eV), φ_{Dn} and φ_{Dp} are *n*/*p* metal drain work functions and E_g is the bandgap of bulk silicon (1.12eV). $\varphi_{Dn} < \varphi_{Si}$ [30], [31] provides no barrier to electron flow but creates barrier for hole diffusion from silicon to metal (metal-silicide). Similarly, $\varphi_{Dp} > \varphi_{Si}$ [30], [31] provides no barrier to hole flow but creates barrier for electron diffusion from silicon to metal (metal-silicide). In practice, near band-edge metal-silicides such as erbium silicide $ErSi_x$ or ytterbium silicide $YbSi_x$ ($\Phi_{Dn} \sim$ 0.27–0.36eV for electrons) [31], [32] for the *n*-drain (D1) and nickel or platinum silicide (Φ_{Dp} 0.15–0.27eV for holes) [31], [32] for the *n*-drain (D2) can be used. Here, Φ_{Dn} and Φ_{Dp} are, respectively, the smallest electron and hole SBH reported with the silicon, [32]. Ideally, the SBH Φ_{Dn} and Φ_{Dp} equals $(\varphi_{Dn} - \chi_{Si})$ for the *n*-drain and $(E_g - \varphi_{Dp} + \chi_{Si})$ for the *p*-drain, respectively, however, it may vary depending upon the non-idealities. In addition, close to mid-gap workfunction for the gate, corresponding to the TiN metal [33] (~4.6-4.9eV), is chosen.

TABLE I
DEVICE SIMULATION PARAMETERS

Parameter	Value
Fin width, W_{fin}	10-20 nm
Fin gap	60 nm
Fin height, H_{fin}	20-60 nm
Gate length, L_g	20-50 nm
Effective oxide thickness, t_{ox}	1 nm
n/p source length, L_{sn}=L_{sp}	50 nm
Extended channel, L_{ext}	5-20 nm
Gate workfunction (φ_G)	4.65 eV
n/p drain workfunction (φ_{Dn}/φ_{Dp})	4.05/5.02 eV

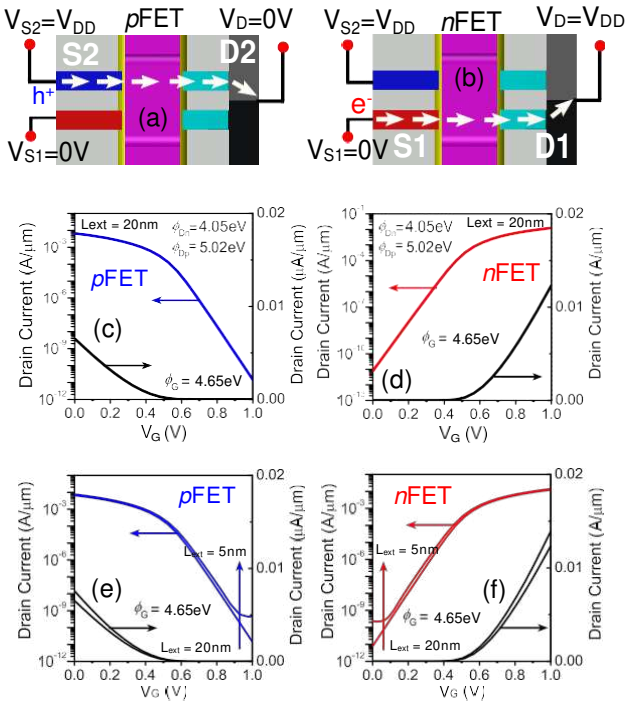

Fig. 2. (a) Holes flowing in the DE RFET during *p*FET operation, (b) electrons flowing during *n*FET operation. Transfer characteristics during (c) *p*FET and (d) *n*FET operation. Transfer characteristics comparison for L_{ext} = 5nm, 20nm during (e) *p*FET and (d) *n*FET operation. φ_G = 4.65eV.

All 3-D simulations were performed on the Synopsys Sentaurus TCAD [34]. Various models invoked in the simulations are Philips unified mobility model that takes into account the concentration dependent mobility along with its degradation due to both impurity and carrier-carrier scattering. In addition, Bandgap narrowing model (BGN) due to the highly doped *n/p* source, Shockley-Read-Hall (SRH) and Auger recombination models are also invoked. Fermi statistics is utilized in conjunction with the drift-diffusion physics. As indicated in the Fig.1(c), simulation models were first calibrated by reproducing the transfer characteristics and matching it with the tri-gate SOI JLT [26]. To account for the lateral tunneling dominant in the OFF-state, nonlocal BTBT model calibrated from the [9], [27], [34] is activated. Besides, carrier confinement due to the quantization effect is taken care of using the modified local density approximation (MLDA) model.

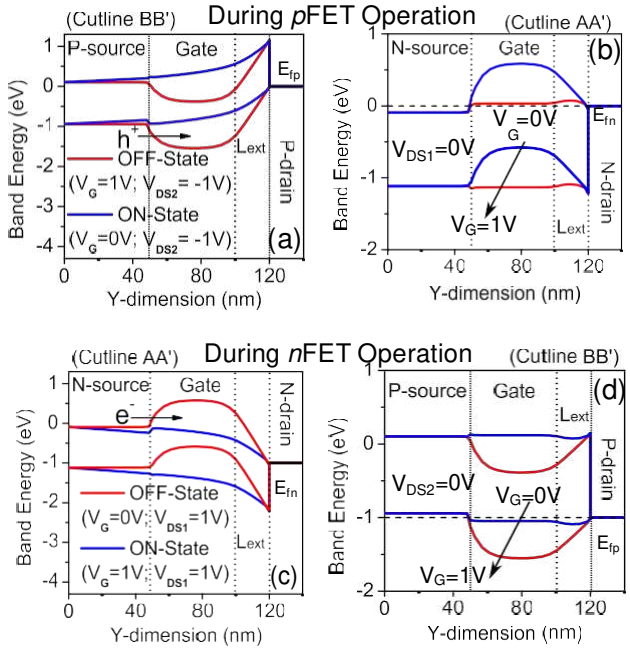

Fig. 3. ON- and OFF-state band diagrams for (a) *p*FET (cutlines BB'), (b) *p*FET (cutlines AA'), (c) *n*FET (cutlines AA') and (d) *n*FET (cutlines BB').

IV. RESULTS AND DISCUSSION

A. Biasing scheme and transfer characteristics

Fig 2(a) and (b) shows the working and biasing scheme of the device for the *n/p* FET operations. For *p*FET, the *n*-section of the fin remains in equilibrium and vice-versa. As shown in the figure, during *p*FET operation, at V_G=0V, a path for hole flow between the *p*-source (S2) and *p*-drain (D2) is created and conduction occurs. Similarly, for *n*FET operation, with V_G= V_{DD}, a path for electron flow between the *n*-source (S1) and *n*-drain (D1) is created. Fig. 2(c) and (d) shows the I_D-V_G characteristics for the *p*FET obtained by biasing the V_{S2} to V_{DD}, V_D to 0V, and sweeping the V_G from 0V to V_{DD}. Similarly, for *n*FET, I_D-V_G characteristics are obtained by biasing V_{S2} to V_{DD}, V_D to V_{DD}, with V_G being swept from 0V to V_{DD}.

Further, in addition, Fig. 2(e) and (f) shows the I_D-V_G characteristics for two different L_{ext} values of 5nm and 20nm at a fixed gate workfunction, φ_G of 4.65eV. We observe that reducing the L_{ext} increases the OFF-state current. This occurs due to the band overlap between the channel valence band (VB) and the drain conduction band (CB) during the OFF-state, which in turn, results in lateral tunneling of charge carriers.

B. Band diagrams during n/p FET operation

Fig 3(a) and (b) shows the band diagrams, respectively, for the *p*FET configuration taken across the cutline AA' and BB'. In a *p*-section fin, we observe a barrier to the current flow (h^+s) at the source-channel junction in the OFF-state, which then is eliminated with the applied gate bias in the ON-state. Note that the *n*-section during the *p*FET operation remains in

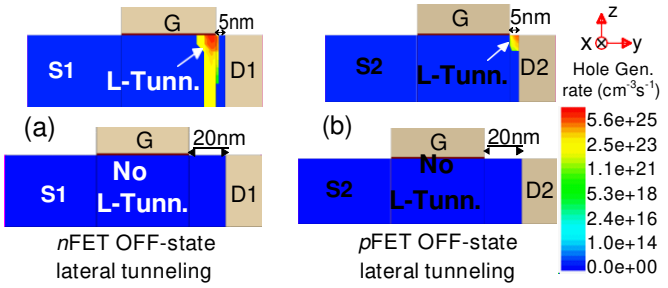

Fig. 4. 2-D contour profile showing OFF-state holes generation rate for (a) *n*FET along the cutplane AA', (b) *p*FET along the cutplane BB'.φ_G = 4.65eV.

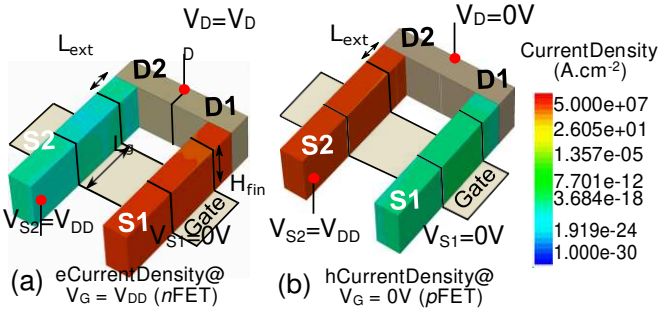

Fig. 5. (a) *n*FET e^- Current Density at V_G=V_{DD}. Shows negligible e^- Current Density between S2 and D2. (b) *p*FET h^+ Current Density at V_{in}=0V. Shows negligible h^+ Current Density between S1 and D1. Gate where V_G is applied, is deliberately removed for clarity.

equilibrium and remains inactive. Similarly, during *n*FET as shown in the Fig.3(c) and (d), *p*-section fin remains inactive and the other fin contribute to the conduction with the proper gate bias. Here, E_{fn} and E_{fp} represent the fermi-level in the *n*-drain (D1) and *p*-drain (D2) regions, respectively.

C. OFF-state leakage during n/p FET operation

Further, to understand the reason for the OFF-state leakage, Fig 4(a) shows the *n*FET OFF-state 2-D hole generation rate showing the increased lateral tunneling at smaller L_{ext} of 5nm, verifying the increased leakage in the OFF-state, shown in the Fig. 2(e) and (f). In *n*FET, carriers tunneling constitutes of the holes moving from the metallic drain region (D1) and CB of the underlap region into the channel VB. As shown in the Fig. 4(b), we also observe the tunneling during *p*FET operation for φ_G = 4.65eV at reduced L_{ext} = 5nm. This is due to the sufficient band bending across the channel/drain region during the *p*FET operation, which results in the tunneling of electrons from the metallic drain region (D2) and CB of the underlap region into the channel VB.

D. Current density profile during n/p FET operation

Fig 5(a) and (b) shows the e^- Current Density and h^+ Current Density, respectively, for the *n*FET and *p*FET operating conditions. At V_G=V_{DD}, only *n*-section fin is active and have a large e^-Current Density constituting the *n*FET current while at the same time, *p*FET fin remains inactive. Similarly, during *p*FET operation, at V_G=0V, only *p*-section fin is active

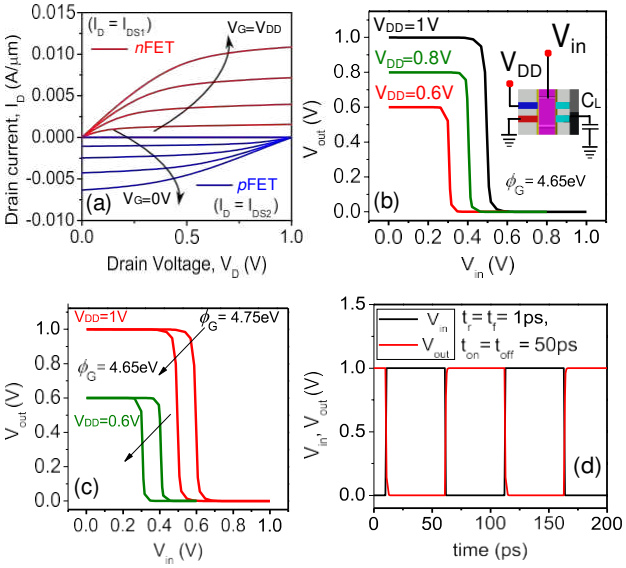

Fig. 6. (a) Output curves of both the *n/p* FETs are shown. Voltage transfer characteristic (VTC) of the DE RFET (b) with V_{DD} scaling, (c) for different φ_G. Inset of (b) shows the device operating in inverter mode. (d) Switching characteristics of the DE RFET at V_{DD} = 1V.

and have a large h^+ Current Density accounting for the *p*FET current while the *n*FET fin remains inactive. This verifies the complementary FET operation realized using the dual fins in a single device.

E. Output, VTC and transient characteristics

The output characteristics corresponding to the *n/p* FET configurations are shown in Fig 6(a). The *p*FET drain current flows between the terminal D2 and S2, denoted by I_{DS2} and corresponding, *n*FET drain current flows between the terminal D1 and S1, denoted by I_{DS1}. A reasonable output characteristics with good saturation are obtained for both the modes. As depicted in Fig. 6(b), when DE RFET is configured as as an inverter unit with biasing scheme shown as an inset in the figure, a reasonable symmetric VTC curve with good high and low logic levels (V_{OH} and V_{OL}) were obtained at V_{DD}=1V. The reason is the matched *n/p* FET characteristics obtained with the gate workfunction tuning, φ_G to 4.65eV (slight ON-current mismatch occurs due to the mobility difference between the holes and electrons).

However, φ_G of 4.75eV adversely shifts the cross-over *n/p* FET voltage close to 0.6V, as illustrated in the Fig 6(c). This will, in turn, result in the asymmetric noise margins (NM_H > NM_L), which was reduced by an optimum φ_G of 4.65eV. A slight mismatch in *n/p* FET ON-currents still persists; however, VTC curve remains close to symmetric, implying equal high and low noise margins. We have also shown the impact of the V_{DD} scaling on the VTC curve upto 0.6V. DE RFET design offers the possibility of scaling the V_{DD} without much degradation in the VTC. Further, Fig 6(d) shows the transient analysis of the DE RFET when subjected to a ramp input pulse of 1V peak-voltage with rise time: t_r = 1ps, fall time: t_f = 1ps and on time: t_{on} = 50ps. A close to CMOS-like

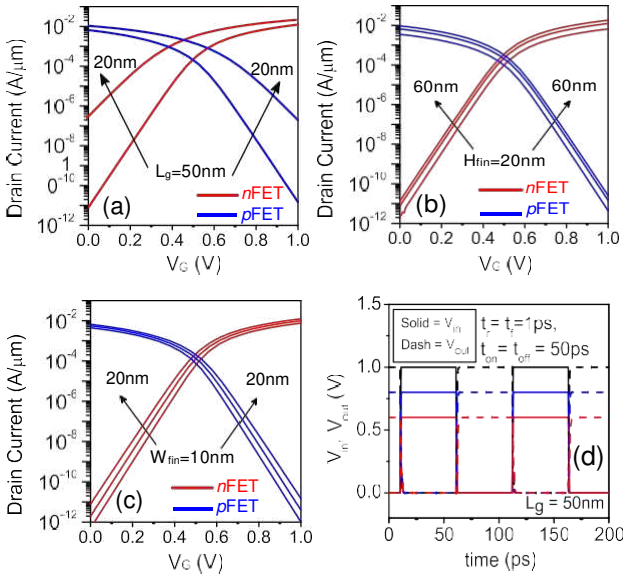

Fig. 7. (a) *n/p* FET transfer characteristics for (a) L_g =50nm and 20nm, (b) H_{fin} from 20nm to 60nm, (c) W_{fin} from 10nm to 60nm. (d) Impact of V_{DD} scaling upto 0.6V on the inverter characteristics at L_g = 50nm.

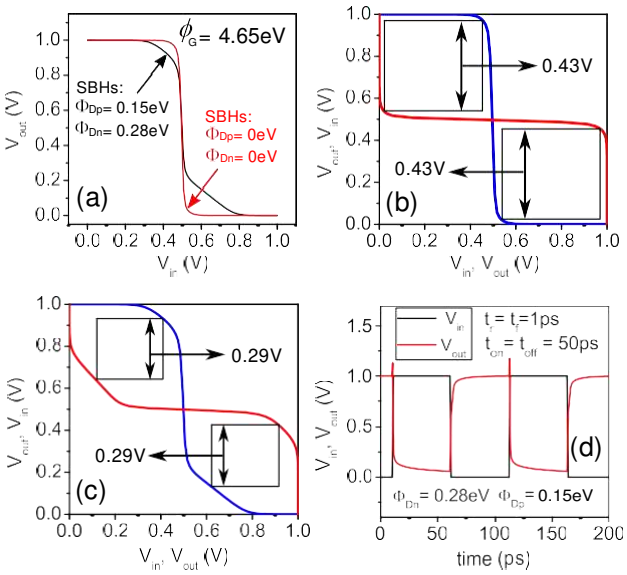

Fig. 8. (a) VTC with zero and finite SBH. Noise margins for the (b) zero SBH and (c) finite SBH. (d) Switching characteristics for the finite SBH.

switching characteristics with minimal rise/fall propagation delay is achieved using only a single device.

F. Impact of device parameter scaling on reconfigurability

With recent trends moving towards the device scaling, it is essential to explore its impact on the device performance. In this regard, Fig.7(a)-(c) compares the impact of gate length, L_g, fin width, W_{fin} and fin height, H_{fin} scaling upon the reconfigurability of the DE RFET. We observe a significant deterioration in the ON/OFF ratio at L_g = 20nm compared to that at 50nm, both for the *n*FET ($\approx 10^6$) and the *p*FET ($\approx 10^4$) operation of the device. This is due to the increased short-channel-effects (SCEs) causing reduced gate controllability at short gate lengths. This can be mitigated by reducing the fin width alongside the use of smaller EOT of 0.5nm. We further observe that increasing the fin height increases the ON-current of the device without much degradation in the OFF-state current. Similar observation is also made for the fin width. With reduction in the W_{fin}, tight gate control results in better subthreshold slope. Despite all these variations, the reconfigurability aspect of the DE RFET remains intact with reasonable deviations in the device parameters. Further, Fig.7(d) explores the plausibility of using the proposed DE RFET as the supply voltage, V_{DD} is scaled. The device works reasonably well in the inverter mode up to the V_{DD} of 0.6V.

Moreover, DE RFET, as a reconfigurable device has also been compared with the existing literature, as listed in the table II. The device is comparable in terms of performance with the window for further reducing the operating voltage.

G. Impact of finite SBH

So far we have taken D1 and D2 workfunctions as such that the effective SBH is close to zero. However, in practice the SBHs are not negligible rather it has a finite value. Therefore, here we set the electron SBH for D1: $\Phi_{Dn} \approx 0.28$eV, corresponding to the erbium silicide $ErSi_x$ and hole SBH for D2: $\Phi_{Dp} \approx 0.15$eV, corresponding to the platinum silicide PtSi. We then observe in the Fig. 8(a) that the VTC curve is slightly degraded due to the increased barrier resistance existing at the channel-drain junctions. To assess and evaluate the noise margin, we have considered two conditions, as indicated in the Fig. 8(b) and (c): 1) VTC with ideally zero SBHs and 2) VTC with finite SBHs. In both cases we have drawn butterfly curves and calculated the high and low noise margins, NM_H and NM_L. For the case of zero SBHs, $NM_H = NM_L = 0.43$V while for the finite SBHs, $NM_H = NM_L = 0.29$V is observed. Equal noise margin indicates that the VTC is close to symmetric. Further, in Fig.8(d), the impact of finite SBHs on the inverter characteristics is analyzed. We observe increased overshoot voltage alongside increased output delay in comparison to the zero SBH case shown in the Fig.7(d).

H. Impact of single mid-gap silicide on reconfigurability

In this section, a new device architecture having a single silicide as a drain region is analyzed instead of two near band edge silicides, as shown in the Fig.9(a). A mid-gap drain silicide (NiSi) corresponding to the workfunction of 4.65eV is used. We observe marginal decrement in the ON-state current during both modes of operation. This occurs due to the increase in SB height at the channel-drain junction of both the fins. Further, it is noteworthy that the mid-gap silicide also increases the lateral tunneling of carriers during the OFF-state. The use of single drain silicide, however, does not hamper the reconfigurability and we observe good I_D-V_G characteristics, as shown in the Fig. 9(b) and (c). Finally, we can infer that the proposed concept is generic in nature, and

TABLE II
STATE-OF-THE-ART FOR MULTIFUNCTIONAL DEVICES WITH *n*FET AND *p*FET CHARACTERISTICS

Devices	**Design**	**Ref.**	**Current injection at source**	**Lg**	**Modes**	**V_D**	**V_G**	**I_{ON}**	**SS(mV/dec)**
SSS; simulated.	DG	[19]	Schottky tunneling	50nm	*n* *p*	0.5V -0.5V	0.5V -0.5V	$\approx 1\times10^{-5}$ A/μm $\approx 7\times10^{-6}$ A/μm	$\approx$ 130 $\approx$ 85
SiNW RFET; fabricated.	NW	[21]	Schottky tunneling	-	*n* *p*	1V -1V	3V -3V	$\approx 2.5\times10^{-4}$ A/μm $\approx 5\times10^{-5}$ A/μm	$\approx$ 220 (min) $\approx$ 90 (min)
DH-FET; fabricated.	Bulk	[23]	Thermionic emission	-	*n* *p*	2.5V -2.5V	2.5V -2.5V	$\approx 7\times10^{-4}$ A/μm $\approx 3.5\times10^{-4}$ A/μm	- -
TF-TFET; simulated.	DG	[24]	BTBT tunneling	30nm	*n* *p*	0.5V -0.5V	0.5V -0.5V	$\approx 1\times10^{-5}$ A/μm $\approx 1\times10^{-5}$ A/μm	$\approx$ 30 (min) $\approx$ 30 (min)
SiNW GAA FET; fabricated.	NW	[22]	Schottky tunneling	45nm	*n* *p*	2V 2V	4V -1V	$\approx 1.7\times10^{-3}$ A/μm $\approx 5\times10^{-4}$ A/μm	$\approx$ 70 $\approx$ 64
VS NS JLFET; simulated.	JL/Stacked Nanosheet(NS)	[35]	Thermionic emission	50nm NS width=7nm	*n* *p*	0.8V -0.8V	0.8V -0.8V	$\approx 1.8\times10^{-4}$ A/μm $\approx 1.4\times10^{-4}$ A/μm	$\approx$ 95 $\approx$ 80
DE RFET; simulated.	SOI (fin)	This work	Thermionic emission	50nm	*n* *p*	1V -1V	1V -1V	$\approx 1.2\times10^{-2}$ A/μm $\approx 6.5\times10^{-3}$ A/μm	$\approx$ 60 (min) $\approx$ 60 (min)

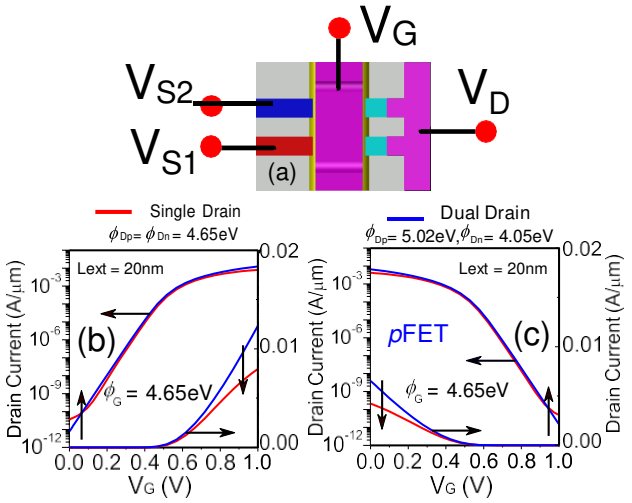

Fig. 9. (a) Schematic of DE RFET with single mid-gap silicide, $\varphi_{Dn} = \varphi_{Dp} = 4.65$eV. Comparison of I_D-V_G characteristics (b) during n-FET operation and (c) during p-FET operation.

therefore can be further extended to other device geometries or alternate current transport devices.

V. Conclusion

In summary, using 3-D mixed-mode simulations, a new device concept, DE RFET, is proposed and investigated. The device can be reprogrammed as an *n*-type, *p*-type FET and a complete inverter unit with adequate biasing. The use of single mid-gap silicide or connected dual near band-edge metal (metal-silicide) drains envisage the complementary switching action. Insights into the device operation reveals device re-configurability, CMOS-like inverter action with a window for future V_{DD} scaling.

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