Flexible and Energy-efficient Synaptic Transistor with Quasi-linear Weight Update Protocol by Inkjet Printing of Orientated Polar-electret/High-k Oxide Hybrid Dielectric

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Abstract

Artificial synapse by inkjet printing is promising in cost-effective and flexible applications, but remains challenging in emulating synaptic dynamics with a sufficient number of stable and effective conductance states under ultra-low voltage spiking operation. Hence, for the first time, a synaptic transistor gated by inkjet-printed hybrid dielectric of electret polyvinyl pyrrolidone (PVP) and high-*k* Zirconia oxide (ZrO_x) is proposed and thus synthesized to solve this issue. Quasi-linear potentiation/depression characteristics with large variation margin of conductance states are obtained through the coupling of these two dielectric components and the facilitating of dipole orientation, which can be attributed to the orderly arranged molecule chains induced by the carefully designed microfluidic flows in droplets. Crucial features of biological synapses including long-term potentiation/depression (LTP/D), spike-timing-dependence-plasticity (STDP) learning rule, “Learning-Experience” behavior, and ultralow energy consumption (< 10 fJ/pulse) are successfully implemented on the device. Simulation results exhibit an excellent image recognition accuracy (97.1 %) after 15 training epochs, which is the highest for printed synaptic transistors. Moreover, the device sustained excellent endurance against bending tests with radius down to 8 mm. This work presents a very viable solution for constructing the futuristic flexible and low-cost neural systems.

1. Introduction

Artificial intelligence (AI) has attracted increasing attention with the coming big data era and intelligent age in recent years, but the conventional von Neumann architectures have limited data transfer rate for neuromorphic computing due to the physical separation of storage and processor units. The adopted silicon complementary metal-oxide-semiconductor (CMOS) chips are not ideal for emulating the intelligent behaviors in brain-like ways and limited to small systems in regard to energy consumption and design complexity, where at least seven silicon transistors are needed to build an electronic synapse[1]. Our brain has a huge advantage of handling complicated and unstructured issues such as comprehension, determination, recognition, and learning concurrently in a robust and fault-tolerant way with extreme energy-efficiency of only ~20 W. Synapses are widely recognized as the essential nodes for realizing brain functions by the modulation of their connection strength, which is referred to as the synaptic weight. Although extensive researches on solid-state artificial synapse in single device level have been carried out to simulate brain functionalities, the realizing of low-cost and flexible synaptic devices with improved performances and limited energy consumption remains challenging, thus has received increased attention in the scientific community[2].

Recently, the idea of building a cost-effective and flexible synaptic device using the drop-on-demand, non-contact and atmospheric processing inkjet printing, instead of sophisticated operation process and vacuum-based physical deposition techniques, has been conceptualized, especially in the fabricating of three/multi-terminal synaptic transistors, which have advantages over two terminal memristors in that they have independent terminals for signal transmission (via drain biased channel flow) and learning operation (via gate biased weight update), thus can eliminate the complex synchronizing algorithms and

simplify the learning scheme[3]. The attempts of inkjet printing mainly focus on the electrodes (PEO:P3HT[4], etc.) and the channel layers (sc-SWCNTs[5,6], P(VP-EDMAEMAES)[7], In_2O_3[8], ITO[9] etc.) in synaptic transistors, while to fabricate the dielectrics is blocked by the basic need of analog multi-state weight update in biological like protocol. Nonvolatile manipulation of the dielectrics and a further step of achieving sufficient states are critical on the efficiency of synaptic functions, for example, the recognition speed and accuracy in image recognition. Bao et al. with Stanford University first utilized organic electrolyte dielectric (PVDF-HFP) by inkjet printing to prepare a stretchable synaptic transistor, but significant impediments still maintain in achieving controllable weight update with nonvolatile and sufficient states[10]. Significantly, the achieving of sufficient dielectric states is still a burden even for non-inkjet-printed synaptic transistors, although tremendous contributions have already been made to achieve the nonvolatile behavior based on diverse kinds of dielectric materials (ferroelectric[11,12], electret[13–15], electrochemical[16,17], two-dimensional[18–20], hybrid materials[21–23], etc.) and structures (floating gate[24–30], heterojunction[31–34], etc.).

Polymer electrets offer a great potential as an exciting candidate for inkjet printing and flexible fabrication[35]. The electrostatic interaction between the captured charges and dipoles is beneficial to the acquisition of the semi-stable nonvolatile states[36]. Among all electret-based synaptic transistors, non-polar electrets are generally employed as efficient chargeable dielectrics, but a high stimulation voltage over 10 V is always required based on the charge trapping/de-trapping mechanism[37]. The use of polar-electrets is limited by the rapid dissipation of the transferred charges and the disorderly arrangement of the dipoles, which leads to an ignorable polarization intensity. High stimulating voltages up to tens of volts for polar-electrets with strong polar side groups on the polymer chains are reported to induce considerable polarization[38–40]. However, the orientation of dipoles is still lacking of regulation methods compatible with the inkjet-printing or the non-inkjet-printing devices.

Strong dipoles on intrinsic ordered two-dimensional fluorographene (FGR) has been proposed in a synaptic transistor to have a large margin weight update under a stimulating voltage as low as 3 V, which demonstrates the significance of molecule alignment for energy-efficient synaptic devices based on the polarization mechanism[41]. Although the traits of microfluidic regulation have attracted intense interests in the field of inkjet printing and are desirable for the alignment of electret molecules, which may be conducive to the orientation of dipoles along the chains, they have not been applied yet in a synaptic transistor. The lack of overlap between these two fields thus far is due to the challenges associated with the developing of new printable dielectric inks that simultaneously meet the needs of microfluidic control and high-efficient synaptic functions.

In this work, a flexible synaptic transistor gated by inkjet-printed hybrid dielectric of polar-electret polyvinyl pyrrolidone (PVP) and high-*k* Zirconia oxide (ZrO_x), which are both low in processing temperature ($\leq$ 200°C), solution processable, and bio-compatible, is first suggested to emulate synaptic dynamics with a sufficient number of stable and effective conductance states under ultra-low voltage spiking operation. The composites are very promising due to the combination of their predominant advantages, such as the

flexibility of PVP and the prospective of ZrO_x toward low voltage transistors[42]. A co-solvent PVP/ZrO_x hybrid ink is developed with carefully designed microfluidic flows, in which the induced compositional Marangoni flows and capillary compensation flows are all outward directions, enhancing the shearing strength on PVP molecules and leading to an orderly arranged morphology of the film. The variation margin and linearity, which are the key to achieving sufficient effective states, are improved in the developed synaptic transistor due to the nonvolatile polarization of a satisfactory number of dipoles divided into discrete regions by the coupling of PVP and ZrO_x components. The demonstrated nonvolatile behavior may be attributed to the electrostatic interaction between the dipoles and trapped electrons in oxygen-deficient ZrO_x. Hundreds of strong dipoles (polar butyralactam side groups) contained in each of the PVP chains and the alignment of the molecules provide a great opportunity for the regulation of polarization under low voltages. As a result, crucial features of biological synapses with a minimum energy consumption lower than 10 fJ/pulse and an excellent image recognition accuracy up to 97.1 % after 15 training epochs, which is the highest for printed synaptic transistors, are successfully implemented on the device, and sustained excellent endurance against bending tests with radius down to 8 mm. This work has significant reference for the inkjet printing of high-performance and low-energy-consumption synaptic transistors applied in the futuristic flexible and low-cost neural systems.

2. Results And Discussion

2.1 Inkjet-printed PVP/ZrO_x hybrid synaptic transistor

The learning of neuromorphic system is governed by the synaptic plasticity, i.e. the ability to modulate the strength of connection between neurons (synaptic weight, W) to store and process information. External stimulus or incoming action potentials from the pre-synapse induce the releasing and diffusion of neurotransmitter molecules and depolarize the membrane of the post-synapse, engendering a tunable postsynaptic current (PSC). In a synaptic transistor, channel conductance (G) is analogous to W. The current difference before and after the stimulus (ΔG) represents the change of synaptic weight (ΔW). When ΔW is increased or decreased by applying positive or negative pulses, synaptic device exhibits excitability and depression, triggering excitatory postsynaptic conductance (EPSC)/inhibitory postsynaptic conductance (IPSC), respectively (Fig. 1a). The proposed device is fabricated on flexible PI substrate with PVP/ZrO_x hybrid dielectric deposited by inkjet printing (Fig. 1b), which has a regular surface morphology with orderly arranged molecules (Fig. 1c, **Supplementary Figure S1**). The deposited films are constructed with multi-droplets released by printer nozzles, where micro-fluid flows are unignorable on account of the low viscosity (4 ~ 20 mPa.s) nature for both the developed PVP and PVP/ZrO_x inks. When a droplet reaches its equilibrium states after impacting on the substrate, the triple line (air-solid-liquid) will be pinned during the solidification process. The uneven evaporation rate along the surface will induce outward compensation flows from the center to the periphery area inside of the droplet, thus making the long chains of PVP molecules arranged in the same direction. The alignment of PVP chains is further enhanced by using co-solvents of 2MOE and EG in the developed inks, which leads to the outward compositional Marangoni flows along the surface of a droplet. The directions of the

surface and the interval flows are the same as a result of both the higher boiling point (T_b) and the higher surface tension (σ) of EG (T_b = 197.3°C, σ= 46.5 dyne/cm) compared with 2MOE (T_b = 124.5°C, σ= 27.6 dyne/cm). The faster evaporation rate will increase the component proportion of the higher boiling point solvent (EG), which make the surface tension gradually increased from the center to the edge of the droplet. The same flow direction ensures the orientation consistency of PVP molecules in the solidified films (Fig. 1d).

The smoothness and uniformity of the PVP/ZrO_x hybrid layer provide a good interface basis for the growth of a-IGZO, which is demonstrated by the SEM images shown in Fig. 1e. The gate electrode (Al) is regarded as a presynaptic neuron, and biological synaptic functions can be emulated by applying appropriate gate stimulus to modify ΔG dynamically, which is highly related to the hysteresis effect induced mainly by the dielectric. As indicated in Fig. 1f, dual-scan transfer curves of the synaptic transistor are presented with a large and counterclockwise hysteresis window near 5 V in a small V_{GS} scanning range from − 5 V to 5 V (V_{DS}= 0.1 V), which indicates that a positive forward gate potential increases the channel conductance (“potentiation” of the synaptic weight), while a negative one decreases the channel conductance (“depression” of the synaptic weight). It is notable that the transfer curves of both PVP and PVP/ZrO_x devices fabricated by inkjet printing have anticlockwise hysteresis loop direction, while the ZrO_x device shows a clockwise hysteresis loop direction (**Supplementary Figure S2**), which implies the polarization of the nonionic PVP-K30 molecules and the trapping of electrons from a-IGZO to the trapping sites of the oxygen vacancies induced in ZrO_x (**Supplementary Figure S3**, XPS, Oxygen vacancy in ZrO_x).

Under positive gate bias, the trapped electrons in ZrO_x will reduce the channel current, but the polarization of PVP molecules provides internal dynamics that drive the increased analogue-channel conductance-switching behavior. Stronger polarization of the dielectric can be induced from its initial state to the saturated state under continuous gate spikes due to the facilitated orientation of dipoles in the aligned PVP chains, which can be inversed simply by the rotation of the polar butyralactam side groups at low voltages (Fig. 1g). As a consequence, the hysteresis window is extremely large for the inkjet-printed PVP/ZrO_x synaptic transistor, which presents great potential of reproducing synaptic weight by an intrinsic analogue state of channel conductance with V_{GS} controlled dependence.

2.2 Basic biological behaviors and non-volatile features

Figure 2a shows a schematic diagram of a dynamically adjustable artificial synapse. The potentiation and depression responses can effectively mimic the subjective regulation of certain tactile perception in nervous system. During the operation, the positive and negative pulses represent the two external environmental stimuli received by the receptors of the human brain. These stimulus signals are applied to the gate electrode and transmitted to the channel to induce a PSC. The EPSC and IPSC responses triggered by a sequence of gate input spikes are exhibited in Fig. 2b and Fig. 2c, respectively. Obvious potentiation and depression phenomenon can be observed under small gate spikes that have the identical amplitude (± 2 V), fixed source-drain voltage (V_{DS} = 0.1 V), and different width ranging from 100

ms to 500 ms. The PSCs show a sudden saltation during spikes, but decay back slowly due to the nonvolatile switching of the states. The strong EPSC and IPSC responses are consistent with the large hysteresis shown in Fig. 1f. As shown in **Supplementary Figure S2**, the polarization hysteresis window of the PVP/ZrO_x device is much larger than the PVP device, which may stem from the nonvolatile characteristic enhanced by the electrostatic interaction between the dipoles and electrons trapped by the oxygen vacancies in ZrO_x. Nonvolatile characteristic makes the modulated weight states more stable, thus multi-states can be easily achieved by gate stimuli with different pulse width.

Paired pulse facilitation/depression (PPF/D) depicts a physiologic behavior, in which the subsequent response of synapses is temporally enhanced/depressed by a prior impulse[15]. Such a property can be observed in Fig. 2d and Fig. 2e by applying two consecutive impulses (1 V/-2 V, 100 ms) with different pulse intervals. PPF changes can be manifested and calculated by introducing PPF index with the expression $((A_2 - A_1)/A_1) \times 100\%$, where A_1 and A_2 are the relative current of the pre- and post-spike responses, respectively. The conductance potentiation gradually decays as the time interval increases and this phenomenon between the EPSCs and spike interval observed in our artificial synapses can be described by a double exponential function

$$\mathrm{PPF} = C_0 + C_1 \exp(-t/\tau_1) + C_2 \exp(-t/\tau_2) \quad (1)$$

where C_0 is a constant, t is the pulse interval, C_1 and C_2 are the initial potentiation amplitudes, and τ_1 and τ_2 are the relaxation times. All these parameters were extracted from the fitting equation: C_0 = 144%, C_1 = 16.6%, C_2 = 67.0%, τ_1 = 19.5 ms, τ_2 = 534.1 ms for PPF. The decay times of the short-term and long-term segments are 19.5 ms and 534.1 ms, which matches well with the time scale in biological synapse[28]. The successfully achieved PPF/D is similar to the case of chemical synapses, where the weight update of synapses can be enhanced by reducing the pulse interval.

The controllability and reversibility of the weight update under alternating positive (1 V) and negative (-1 V) voltages are explored in Fig. 2f. The enhanced synaptic connectivity under positive pulses can be easily restored when negative pulses continue to be applied, which is similar to the highly repetitive stimulation of the action potential found in the biological nervous system. Figure 2g verifies the short-term and long-term potentiation (LTP/STP) simulated under consecutive pulses with different amplitudes. The conductance is regulated to a suppressed state before the measurement by applying a -1 V voltage of 50 s. A near three magnitudes potentiation is induced after 10 consecutive pulses (1 V/100 ms), and then slowly decays to a stable equilibrium state, which is still about two magnitudes higher than the initial conductance, indicating a LTP behavior. When the pulse amplitude decreases to 0.5 V, the potentiated conductance decays back to its initial value in only 10 s due to the spontaneous relaxation of the unstable regulated states, indicating a STP behavior. Multi-state controllability of the conductance ascribed to the non-volatile characteristic is further evidenced by symmetric long-term potentiation/depression (LTP/D) behaviors (Fig. 2h). When the repetitive number (N) of the stimulation

pulses (2 V/-2 V, 100 ms) increases (N1 to N30), persistent transition to the high/low conductance state of the device can be clearly observed, successfully simulating the LTP/D mechanism of biological synapses, which are presumed to play a significant role in learning processes in the brain. The randomly orientated polar side groups on the aligned PVP chains of the initial dielectric state might be necessary to allow dipoles to have a nearly symmetrical response to contrary pulses, as a result that a symmetrical weight update of the potentiation and depression can be achieved. To make the nonvolatile capacity of the synaptic device clear, the retention characteristics of the transistor are measured after 10 gate input spikes with amplitudes from − 1 V to 3 V (V_{read} = 0.05 V). As shown in Fig. 2i, the conductance state keeps longer than 10^4 s after stimuli as low as 2 V and − 1 V for the potentiation and depression, respectively. Although the current after 1 V stimuli decays slowly in 1000 s, the stored data retention is stable enough and suggests a promising feature for neural computing.

2.3 Synaptic plasticity for learning functionalities

Physiological learning, forgetting, and relearning processes are emulated by applying low voltage pulses (1 V, 100 ms) to the synaptic transistor (Fig. 3a). Although the PSC decays slowly (forgetting) after 20 pulse trains (learning), it can be enhanced back to the same level in 8 pulse trains (relearning), and afterwards only 2 pulse trains are demanded for the re-learning operation. Interestingly, the persistent time (forgetting) increased from 503 s to 631 s after the re-learning process, which is extremely similar to the re-learning process in our human brain, that is, the old knowledge becomes more and more difficult to forget after repetitive learning. We also confirm the spike timing dependent plasticity (STDP) learning protocol of the synaptic devices, as shown in Fig. 3b. STDP refers to the weight update with relative timing between the presynaptic and postsynaptic spikes ($\Delta t_{pre-post}$), thus has the potential to transform the time information in neural networks into memory storage, and is widely considered as a key feature of a biological neural system. As a biological process in neuromorphic learning, STDP represents the famous Hebbian learning rule and can be divided into asymmetric and symmetric types. It is noteworthy that the LTP/D coexistence in our device enables various types of STDP, while the learning function is determined by the shape of the successive action potentials. Asymmetric learning, where the synapse weight is simultaneously determined by the time difference ($|\Delta t_{pre-post}|$) and timing order ($\Delta t_{pre-post} > 0$ or $\Delta t_{pre-post} < 0$), is mimicked here by using a pair of stimuli that consisted of a positive triangular spike (0 V to 2 V, 300 ms) following a negative triangular spike (-2 V to 0 V, 300 ms) on both of the pre- and postsynaptic parts of the synaptic transistor (**Supplementary Figure S4**). It is indicated that the potentiation and depression take place when $\Delta t_{pre-post} > 0$ and $\Delta t_{pre-post} < 0$, respectively. Moreover, the greatest change in synaptic plasticity happens in the ± 10 ms scale, whereas the smallest weight modification happens when the time interval between the pre- and postsynaptic spikes is relatively long. According to the empirical relationship of spike time-related plasticity, the dependence of synaptic weight changes on the $\Delta t_{pre-post}$ can be described as follows[33]:

$$G(\Delta t_{pre\text{-}post}) = \begin{cases} A_+ \exp\left(\frac{\Delta t_{pre\text{-}post}}{\tau_+}\right) & \text{if } \Delta t_{pre\text{-}post} \geq 0 \\ A_- \exp\left(\frac{\Delta t_{pre\text{-}post}}{\tau_-}\right) & \text{if } \Delta t_{pre\text{-}post} < 0 \end{cases} \quad (2)$$

where A_+, τ_+ and A_-, τ_- are the scaling factors and time constants for the positive and negative $\Delta t_{pre-post}$, respectively. The calculated results of τ_+ = 28.5 ms and τ_- = -30.8 ms are similar to the time scales of STDP in a typical biological system[43]. The successful implementation of STDP provides a novel working model for the development of neuromorphic systems[44].

For the efficiency of synaptic functions, it's critical to achieve sufficient and effective weight states, where the variation linearity and margin are the two key factors. The developed device demonstrates an extremely large variation margin (G_{max}/G_{min} = 1.35×10^5, G_{max}-G_{min} = 10 μS) through relative high operation voltages of 5 V and − 3.8 V for the potentiation and depression, respectively (**Supplementary Figure S5**). The high-*k* nature of ZrO_x and the improved nonvolatile characteristic by the coupling of the mechanisms of dipoles (from PVP) and the trapped electrons (from ZrO_x) may be responsible for the result, which can be evidenced by the apparently improved variation margin of the PVP/ZrO_x device compared with the PVP ones (Fig. 3c, **Supplementary Figure S6**). It is also indicated that the variation linearity is improved with a considerable variation margin when the voltages are decreased to 1V. The low voltages are suitable to avoid abrupt switching of the conductance at the premise of excellent state persistence in such a small interval time of 100 ms. Moreover, we assume that the coupling of the PVP and ZrO_x components induces discrete regions of the polarization, which allows the dynamic switching of polarization states more linear (Fig. 3d). Figure 3e exhibits repeated cycles of LTP and LTD under consecutive positive (1 V, 100 ms) and negative (-0.8 V, 100 ms) gate input pulses. Steady and linear variation of both the LTP (Nonlinearity, NL = 0.0058) and LTD (NL = -0.38) in each cycle maintains for a large number of weight states up to 200, which is ultra-high compared with previous reports (below 100 for most cases) and shows potential of dealing with complex and efficient computing tasks using the developed artificial synapse.

2.4 Flexibility and neuromorphic simulation for image recognition

The flexibility of the inkjet-printed PVP/ZrO_x synaptic transistor is measured with a bending radius of 8 mm (Fig. 4a, **Supplementary Figure S7**). The polymer chains of PVP act as connections and buffer between high-*k* ZrO_x molecules without deterioration, and simultaneously improve the leakage and mechanical flexibility of the dielectric layer. Basic synaptic functionalities, including PPF/D index as a function of pulse interval (**Supplementary Figure S8**), LTP/D response to different pulse amplitudes and stimulation numbers (**Supplementary Figure S9**), and physiological learning experiences (**Supplementary Figure S10**), are successfully mimicked for the flexible artificial synapse, although higher stimulation voltages are demanded for achieving the similar synaptic behavior before bending. We suppose that the orientation of the polar side groups on PVP molecules (dipoles) is affected by the deformation of the polymer chains and the re-distribution of surrounded electron-trap sites, leading to the slightly decreased

retention time of the potentiated state under a positive stimulation voltage of 1 V. The overlapping diagrams of adjacent LTP (1 V, 100 ms) and LTD (-0.8 V, 100 ms) processes (20 weight states) for the devices measured under bend (R = 8 mm) and flat conditions are presented in Fig. 4b and Fig. 4c, respectively. The reproducible and consistent LTP/D performance of both the bend and flat devices verifies their reliability of the synaptic plasticity, and indicates excellent flexibility of the developed artificial synapse, although a superior linearity is observed for the flat device due to its better non-volatile behavior. It can be evidenced by the more linear conductance modulation achieved in **Supplementary Figure S11**, where an increased stimulation voltage (2 V) is applied to improve the non-volatile characteristic. It is notable that further increasing the voltages will make abrupt conductance switching during the first few pulses (Fig. 3c), thus non-volatile behavior under low voltages is of great concern for the achieving of linear weight update.

The artificial neural network (ANN) based on the developed flexible and inkjet-printed PVP/ZrO_x artificial synapse before and after bending is constructed to investigate the applicability of artificial intelligence in pattern recognition (Fig. 4d). The weight update data for the simulation comes from Fig. 4b and Fig. 4c for the bend and flat devices, respectively. The images (handwritten digits from “0” to “9” randomly taken from the MNIST database) used to verify the recognition effect are processed and rescaled to “8×8” (small) and “28×28” (large) pixels. The altering values of synaptic weights are calculated by comparing the real output and target output in each training epoch, and using the input signal from the training images. Figure 4e shows the recognition evolution of the bend and flat devices for both small and large images. An extremely high pattern recognition efficacy is validated in aspect of both the recognition accuracy (up to 97.1 % after 15 training epochs for the flat device) and speed (over 90 % recognition accuracy in only 10 training epochs). Although the non-linearity for both the enhancement and suppression behaviors of the bend device (NL = 0.11/-0.54) is higher than that of the flat device (NL = 0.014/-0.045), a minimum conductance difference at nS level ensures all the 20 weight states valid for the simulation, which enhances the fault tolerance of the recognition system and improved the recognition accuracy, as a result that the reliability of the developed devices for flexible applications is demonstrated. Importantly, we further investigate the minimum energy consumption demanded for reliable synaptic plasticity, and find that obvious EPSC behaviors could be mimicked successfully after 1000 gate input pulses with different widths/interval time of 100 ns, 1 μs, 10 μs and 20 μs (Fig. 4f). A near 20 % potentiation of the conductance is observed even for the case when the pulse width and interval time are 100 ns and 100 ns, respectively. An ultra-low energy consumption of about 1.43 fJ per event is estimated by $I_{peak} \times t_{width} \times V_{DS}$, which exhibits great potential to mimic the real energy consumption of human brain like artificial synapse (about 10 fJ per event). The ultra-short pulse stimulus is attributed to the fast response of dipole inversion on the aligned PVP chains. As indicated in Fig. 4g, the recognition accuracy and the energy consumption are comparable or superior to most of the reported synaptic transistors[15,24,26,28,29,45–59]. Moreover, we are first to demonstrate the image recognition capability for flexible and inkjet-printed synaptic transistors. This superior performance means that the developed device has the potential to be a promising candidate for flexible or even wearable artificial neural network, in which pattern recognition is regarded as a necessary task.

3. Conclusion

We first demonstrate a flexible synaptic transistor with PVP/ZrO_x hybrid dielectric deposited by inkjet printing, and achieve orderly arranged polar-electret molecules by microfluidic control, which ensures the capability of mimicking biological behaviors based on polarization mechanism. The coupling of PVP and ZrO_x dielectric components contributes to the flexibility, energy-efficiency and nonvolatile controllability of the synaptic device. Basic biological behaviors and learning functionalities like STP to LTP transition, LTP/D, “Learning-Experience” behavior, STDP learning rule are all successfully mimicked. Reproducible synaptic weight update with cycles of quasi-linear and large margin LTP/D is demonstrated to have a large number of effective states over 200. Nevertheless, the near ideal weight update protocol makes a small number of distinct states (N20) adequate for the simulation of image recognition, which exhibits an excellent recognition accuracy (97.1 %) after 15 training epochs, and is the highest for printed synaptic transistors. Although the conductance variation linearity is slightly deteriorated for the devices after bending (R = 8 mm), a recognition accuracy over 90 % is also resulted. Considering the ultra-low energy consumption of about 1.43 fJ per event for inducing synaptic plasticity, the developed synaptic transistor by cost-efficient inkjet printing technique may be promising to construct futuristic artificial synapse extremely analogous to that in our brain.

4. Experimental Section

Ink Preparation: The PVP/ZrO_x hybrid dielectric inks are synthesized by dissolving $ZrOCl_2 \cdot 8H_2O$ in a mixture of 2-methoxyethanol (2MOE) and ethylene glycol (EG) at a ratio of 1:1, and then adding 5 % of nonionic PVP-K30 powder. The solution was stirred at room temperature at 800 r/min for 5 h. The viscosity of the ink is maintained at 4 ~ 20 mPa.s, and the surface tension is preserved in 25 ~ 35 mN/m.

Device Fabrication: A 120 nm thick Aluminium (Al) gate electrode is deposited on a 50 μm spin-coated polyimide (PI) flexible substrate by DC magnetron sputtering. It is worth noting that a buffer layer of SiO_x/SiN_x on PI substrate exists for all devices, which is not described in the text to simplify the discussion. Afterwards, a PVP/ZrO_x hybrid dielectric layer (≈ 200 nm) is deposited by inkjet printing with a drop space and nozzle temperature of 30 μm and 30°C, respectively. Inkjet printing equipment (DMP-2800, Fujifilm Dimatix, Japan) with a piezoelectric printhead is selected, and the diameter of nozzles in the cartridge (DMC-11610, Fujifilm Dimatix, Japan) is 16 μm. The hybrid dielectric is UV treated for 30 minutes followed by 200°C annealing for 1 hour in an atmospheric environment. Subsequently, a 10 nm thick IGZO film was deposited at room temperature by pulsed DC magnetron sputtering with a pressure of 1 mTorr in mixed atmosphere (Ar: O_2 = 20: 1). The semiconductor layer was annealed in atmospheric environment at 150°C for 1 hour. Finally, source and drain electrodes (Al) with a thickness of 150 nm are deposited by DC magnetron sputtering at room temperature.

Characterization

The surface morphologies of the films are characterized by Atomic Force Microscopy (AFM, Asylum Research). The cross-sectional morphologies of the device are investigated by field emission scanning electron microscope (SEM, NP-O10, ZEISS Gemini 500). The electrical properties of the synaptic devices are measured using a high-precision semiconductor device analyzer (Agilent B1500A) equipped with high-voltage semiconductor pulse generator unit (HV-SPGU, B1525A), which can generate pulses of magnitude up to ± 40 V and width from 10 ns to 10 s. The V_{DS} applied for all electrical measurements is 0.1 V. The flexible transistors are peeled off from the glass substrate and then pasted on the stainless-steel half cylinder. All electrical measurements are performed in the dark and vacuum atmosphere (10^{-3} Pa), which can remove the moisture in the dielectrics and simplify the discussion of the ionization effect of the nonionic PVP-K30 molecules.

Declarations

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Contributions

Y. L. and W. C. contributed equally to this work. R. T., X. L. and H. N. conceived the project. W. C. was involved in the fabrication. Y. L. and R. T. performed the characterization experiments and analysis; Y. L. and R. T. co-authored this paper. R. T., X. L. and H. N. supervised the project. All authors discussed the results and commented on the manuscript.

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Competing interests

The authors declare no competing interests.

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Figures

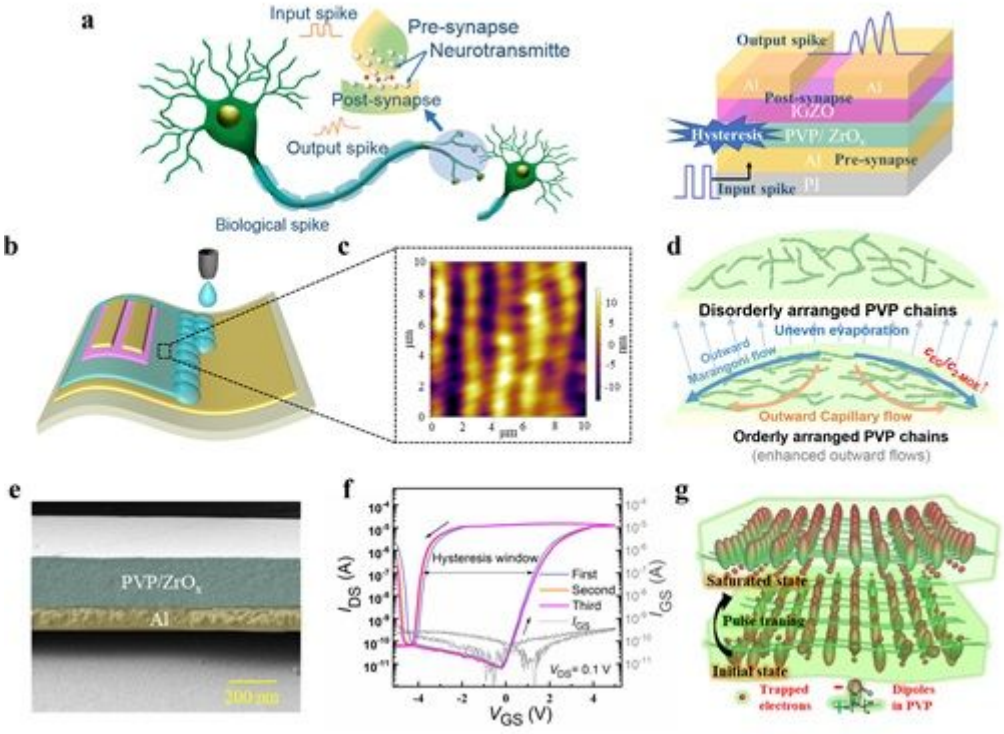

Figure 1

Schematic diagram and characterization of the flexible synaptic transistor deposited by inkjet printing. a Structures of a synapse and the transistor-based device proposed to emulate synaptic functions. b Schematic diagram of the inkjet printing of PVP/ZrOx hybrid dielectric in the transistor on PI substrates. c AFM surface morphology of the dielectric. d Schematic diagram of the orderly arranged PVP chains regulated by microfluidic fluids in co-solvent ink system. e SEM cross-sectional image of the dielectric. f Transfer curves of the transistor measured in double sweep and showing hysteresis of IDS (PSC) as a function of the VGS (pre-synaptic stimulus) when VDS = 0.1 V. The hysteresis loop direction is anticlockwise with a sweep range from -5 V to 5 V and then back to -5 V. g Schematic diagram of the inversion of dipoles from the initial to the saturated state of the dielectric.

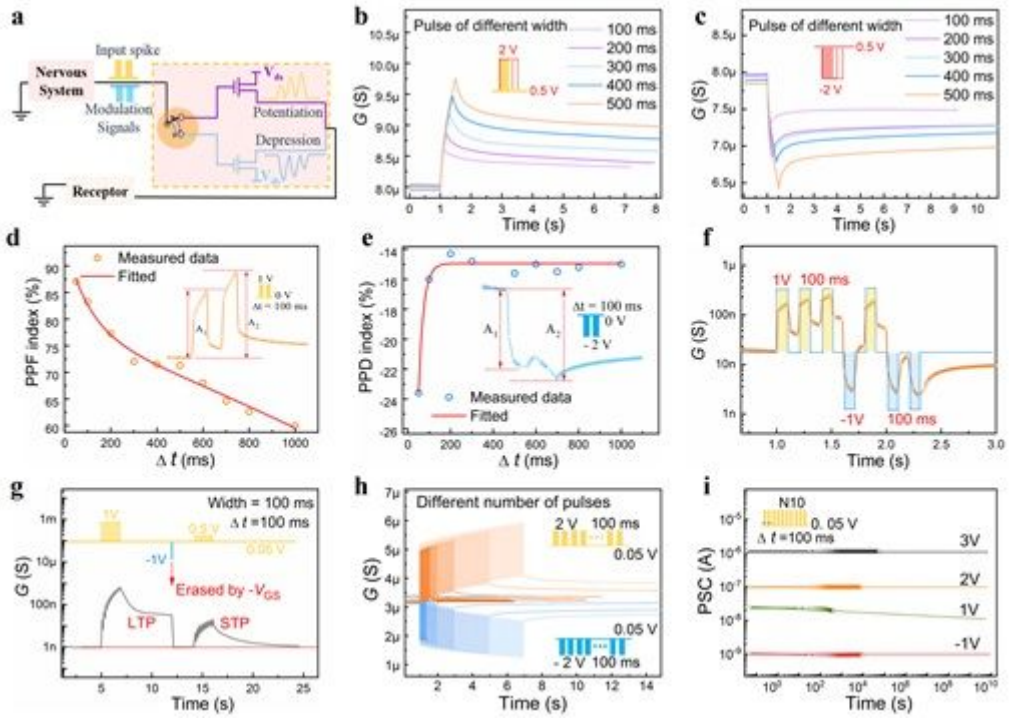

Figure 2

Reversibility, symmetry and stability of the conductance states for the potentiation and depression responses. a Schematic diagram of working principles of the potentiation and depression in neuron system. b, c Typical EPSC and IPSC responses triggered and modulated by gate spikes (2 V/-2 V) with different pulse width from 100 ms to 500 ms. d, e PPF/D index and fitting plotted as a function of pulse interval. The inserted pictures are the EPSC/IPSC generated by a pair of presynaptic pulses with amplitudes of 1 V/-2 V and an interspike interval time of 100 ms. A1 and A2 represent the relative amplitudes of the first and second EPSCs/IPSCs, respectively. f Stability of the conductance state under alternating positive and negative voltages. g Continuous LTP and STP behaviors simulated under pulse voltages of 1 V and 0.5 V, respectively. h Stable and symmetric LTP/D manipulation by applying increased pulse number ranging from 1 to 30. i Retention life time of the transistor measured after 10 gate input spikes with amplitudes from -1 V to 3V (VDS = 0.1 V).

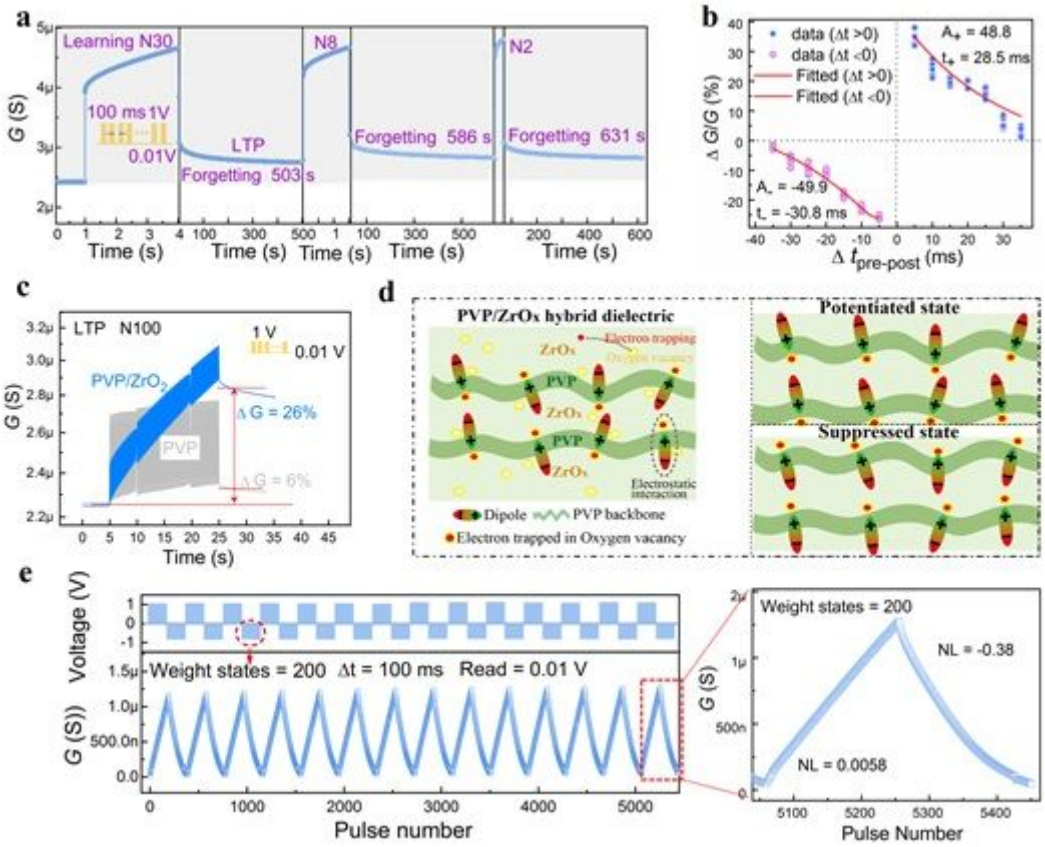

Figure 3

Synaptic functionalities in PVP/ZrOx inkjet-printed transistor. a Physiological learning, forgetting, and relearning experiences of the synaptic transistor. b STDP behavior obtained in the synaptic device, where the net programming voltage (Vpre − Vpost) applied across the device depends on the positive or negative moments Δtpre-post. c The comparison of the dynamic conductance switching responses for PVP/ZrOx and PVP devices to 100 consecutive pulses (1 V, 100 ms). d Diagram for the non-volatile polarization of the inkjet-printed PVP/ZrOx hybrid dielectric exhibiting both the potentiated and suppressed states after pulse training. e Endurance test shows reproducible synaptic weight update with cycles of conductance potentiation and depression. Each cycle consists of 200 identical voltage pulses (1 V/-0.8 V for 100 ms spaced 100 ms apart).

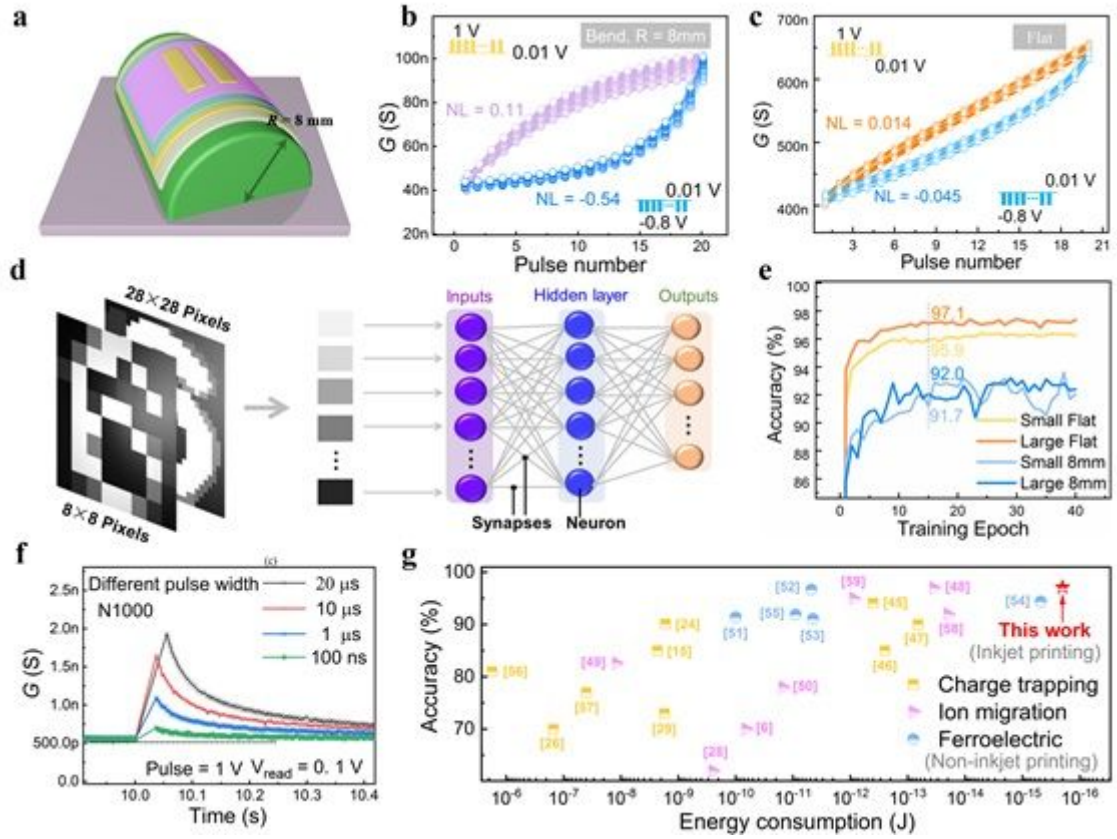

Figure 4

Mechanical flexibility and neuromorphic computing simulations for image recognition. a Schematic diagram of the flexible inkjet-printed PVP/ZrOx synaptic transistor under a bending radius of 8 mm. b, c Overlapping diagrams of adjacent LTP and LTD processes (20 weight states) for the devices measured under bend (R = 8 mm) and flat conditions, respectively. d The architecture of the ANN for image recognition. Different layers of neurons, including input layer, hidden layer and output layer, are connected by synapses. e The recognition accuracy and speed of small (“8×8”) and large (“28×28”) images based on MNIST database for the flexible and inkjet-printed PVP/ZrOx synaptic transistors training under bend (R = 8 mm) and flat conditions. f Conductance responses after pulse stimulations (N1000) with different width on micro (20 μs, 10 μs and 1 μs) and nano (100 ns) levels. g A statistical comparison of the image recognition accuracy and the minimum energy consumption for synaptic responses with previously reported work on transistor-based devices. The lack of published data for image recognition in other inkjet-printed devices is due to their challenges existed in achieving multi-state weight update using inkjet-printable dielectric materials.

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