Optimized Design of an All-Optical XOR Gate with High Contrast Ratio and Ultra-Compact Dimensions

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Optimized Design of an All-Optical XOR Gate with High Contrast Ratio and Ultra-Compact Dimensions

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Abstract—**In this work, an optimized structure of an XOR gate working in the optical domain is put for- ward to achieve high contrast ratio and extremely compact dimensions using a photonic crystal platform. The above structure employs silicon rods in a hexagonal lattice configuration. The design works purely on linear interference effect between the incoming light signals and does not involve any non-linear materials. The Finite Difference Time Domain based simulations are utilized to study the propagation of light within the structure and the Plane Wave Expansion Method is applied to generate bandgap structure. After optimization of the various design parameters, a contrast ratio of 31.76 dB is attained by the proposed structure along with a response time of 0.46 ps and a footprint of 42.24 μm². The device can be operated in the C Band with optimum performance at 1550 nm, which is the telecommunication wavelength. The operating bit rate for the proposed structure is 2.17 Tbps. All-optical XOR gate being a universal gate forms the building blocks of various sequential and combinational logic designs suitable for optical computing and communication applications.**

Keywords— **Photonic Crystal, FDTD, PWE, All Optical logic, XOR gate**

1. INTRODUCTION

Recent advances in technology calls for ultra-high speed data transmission with low latencies to keep up with the user demands. Optical technology plays a pivotal role in dominating all areas of communication and computing due to its wide bandwidth, high speed, compactness and throughput [1]. Owing to the huge popularity of internet-based communications, the availability of bandwidth and high speed is already overwhelmed and leads to the electronic bottleneck problem. The electronics-based system can longer keep pace with the ever-increasing demands of the recent applications and user demands. This calls for a shift towards a complete optical domain wherein all the processes are performed fully using optical signals and there is no requirement for electro-optic conversions and vice versa [2].

In a complete optical network, the various all-optical devices utilize optical logic gates as the fundamental building blocks [3]. Several combinational and sequential logic circuits for applications such as switching, multiplexing, parity checking, encoding, filtering and so on are constructed using logic gates [4]. All these circuits can be implemented using optical logic gates without any electro-optic conversions [5] [6] [7] [8] [9]. Several methods have been utilized to implement these gates such as using non-linear ring resonators [10], Semi-conductor Optical Amplifiers (SOA) [11], non-linear directional couplers [12], Highly Non-Linear Fibers [13], photonic crystals [14], plasmonic slot waveguides [15] and quantum dot SOA [16]. However, most of these designs lack chip level integration capability due to bulky dimensions and flexibility issues [17]. SOA based designs endure gain saturation and make use of high driving current resulting in low-speed operation. Non-linear fibers suffer from bulky design and sensitiveness to environmental factors despite providing better response times. PPLN based devices require accurate temperature control and high input powers for better operation [18]. Currently, photonic crystal platforms are gaining a lot of attention owing to their fascinating features like high integration capability with existing electro-optic as well as optical integrated circuits, flexibility in design, ultra-compact dimensions, wide operating bandwidth, high speed and low power consumption [19]. Photonic crystals possess a unique feature called bandgap which enable efficient manipulation of light in the required direction over a wide operating bandwidth [20]. Photonic crystal-based logic gates usually operate on the principles of self-collimation, Kerr non-linear effect or linear interference effect. Among these, designs based on non-linear effect require higher operating power and self-collimating effect has limitations in attaining compact dimensions [21]. Interference effect based all-optical logic gates enable compact and power efficient designs with high compatibility for advanced optical integrated circuits.

The all-optical XOR (AO-XOR) gate or Exclusive OR gate is highly popular as it supports several applications such as optical computing, parity checking, all-optical error correction and detection, network coding, pseudorandom number generation and so on. The AO-XOR gate forms the fundamental component in the design of complex logic circuits for these critical functionalities [22]. Several works on the design of photonic crystal-based AO-XOR gates are already available in the literature. A design based on a T-junction and nano resonators using two-dimensional (2D) photonic crystals possessed a footprint of 85.22 μm² along with a contrast ratio (CR) of 43.33 dB [23]. An AO-XOR was proposed using Y-branch waveguide with a CR of 33 dB and footprint of 160.08 μm² [24]. A simple design for AO-XOR gate in silicon on insulator with and operating wavelength of 1550 nm was proposed [25]. An implementation using silicon dielectric with square lattice with a footprint of 45.36 μm² attained a CR of 8.29 dB at 1550 nm [26]. A linear structure of footprint 60.2 μm² for AO-XOR operation was proposed with a CR of 14.7 dB and low response time [27]. A configurable structure working on interference effect with dimensions of 192 μm² was designed to achieve XOR functionality with an extinction ratio (ER) of 23 dB [28]. It can be observed that photonic crystal-based designs working on interference effect having compact dimensions and high contrast ratio can be seen as potential candidates for the future optical integrated circuits (OICs). Achieving high contrast ratio without the use of any additional phase control elements leads to a compact and energy efficient design.

In this paper, an optimized AO-XOR gate on a photonic crystal platform using silicon material working on interference principle is implemented. The already proposed structure of reconfigurable AO-XOR/ NOT gate [29] is taken so as to optimize the various structural parameters in order to achieve the maximum contrast ratio and compact dimensions with low response times. The Finite Difference Time Domain (FDTD) technique based simulations are utilized to study the light propagation within the structure whereas the bandgap structure is simulated utilizing Plane Wave Expansion (PWE) method. Section 2 describes the mathematical analysis and principle of operation followed by optimized structure of the AO-XOR gate in section 3. Section 4 details the simulation results and analysis for the optimized design. Section 5 concludes the work followed by references.

2. MATHEMATICAL ANALYSIS AND PRINCIPLE OF OPERATION

Photonic crystals are periodic dielectric structures with low loss that can trap light and manipulate their propagation in the desired path due to bandgap engineering. The photonic bandgaps which arise due to periodic interactions within the crystal are the frequency bands which cannot propagate in the crystal. By properly inserting suitable defects such as line, point and surface defects within the perfect crystal, light gets localized inside and various logic functionalities can be realized [30]. The macroscopic Maxwell's equations govern the distribution of magnetic and electric fields inside the photonic crystal. The following equations are satisfied by electromagnetic waves passing through isotropic, non-magnetic, and nonconductive media [31].

$$\nabla . \mathbf{B} = 0 \tag{1}$$

$$\nabla \times \mathbf{E} + \frac{\partial \boldsymbol{B}}{\partial t} = 0 \tag{2}$$

$$\nabla . \mathbf{D} = \mathbf{0} \tag{3}$$

$$\nabla \times \mathbf{H} - \frac{\partial \boldsymbol{D}}{\partial t} = 0 \tag{4}$$

where, H and B represent the magnetic field and magnetic flux density. E and D represent the electric field and electric flux density. The solutions of Maxwell's equations maybe treated as the product of a plane wave in periodic function as per the Bloch's theorem [32].

$$\boldsymbol{E}\,(r) = \varphi\,(r). \exp(ik\,.r) \tag{5}$$

Here, φ (r) and k denote the periodic function and Bloch's wave number respectively. On the basis of these assumptions, the time independent relations for the wave equations are,

$$\frac{1}{\epsilon_r} \nabla \times \nabla \times \mathbf{E} = \left(\frac{\omega}{c}\right)^2 \mathbf{E} \tag{6}$$

$$\nabla \times (\frac{1}{\epsilon_r} \nabla \times \mathbf{H}) = \left(\frac{\omega}{c}\right)^2 \mathbf{H} \tag{7}$$

Here, ω and ϵ_r denote the frequency and macroscopic dielectric function respectively. These equations can be solved to determine the propagation modes within the proposed photonic crystal structure. The solution at one scale can be used to determine the solution at any other scale since the photonic crystals are scale invariant.

The beam interreference effect can be utilized to determine the logic state of the gate output. The interference maybe destructive or constructive depending on the phase of the arriving signals which can be controlled by changing the path length of waveguides. Constructive interference phenomena arises if the input waves have a phase difference of an even multiple of π. This generates a higher optical intensity or a logic high output state. Destructive interference arises when the difference in phase becomes an odd multiple of π resulting in cancellation of signals leading to low output power or logic low state [33]. The proposed AO-XOR design consists of waveguides of different pathlengths leading to phase difference between the input signals resulting in XOR operation without using any additional phase control mechanisms.

3. DESIGN OF MODIFIED AO-XOR GATE

This work aims to boost the performance of the already designed AO-XOR gate [29] by proper optimization of the structural parameters. The new optimized structure for the AO-XOR gate is illustrated in Fig. 1. Table 1 depicts the truth table for XOR gate. There is one output port (Y) and two input ports (A, B). It consists of a hexagonal lattice of 17×11 silicon rods surrounded by air with a lattice constant (a) of 523 nm. Each rod has a radius (r) of 0.21a. Hexagonal lattice tends to provide larger bandgaps as compared to square lattice, hence it is chosen. The photonic bandgap diagram for the proposed structure is given in Fig. 2. There are two large bandgaps existing in TE mode as inferred from the diagram. These correspond to the values 1622.5 nm to 1062.9 nm in the first band and from 809.7 nm to 633.9 nm in the second band. The first band comprises of the operating wavelength of 1550 nm.

Table 1. Truth table of XOR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

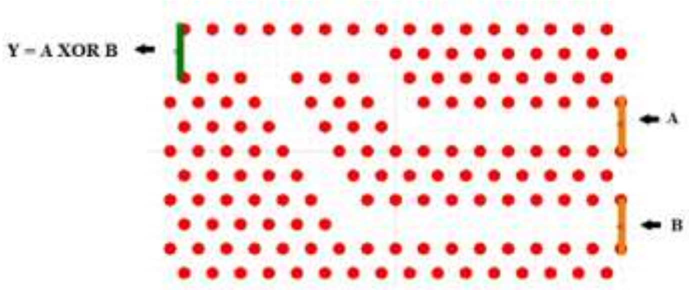

Fig. 1. Proposed structure of AO-XOR gate

The two input ports have considerable isolation between them so as to prevent intermixing of signals. As it can be seen, the distance covered by the optical wave to propagate towards output port Y from input A is shorter compared to the distance between port Y and port B. Hence, when both the input ports have optical signals, these traverse different path lengths giving rise to a difference in phase that is an odd multiple of π thus cancelling them out. When only one input port has an optical signal, there is no interaction occurring and the same signal arrives at the output. The detailed design parameters are tabulated in Table 2. All these parameters are chosen after proper optimization as given in the next section.

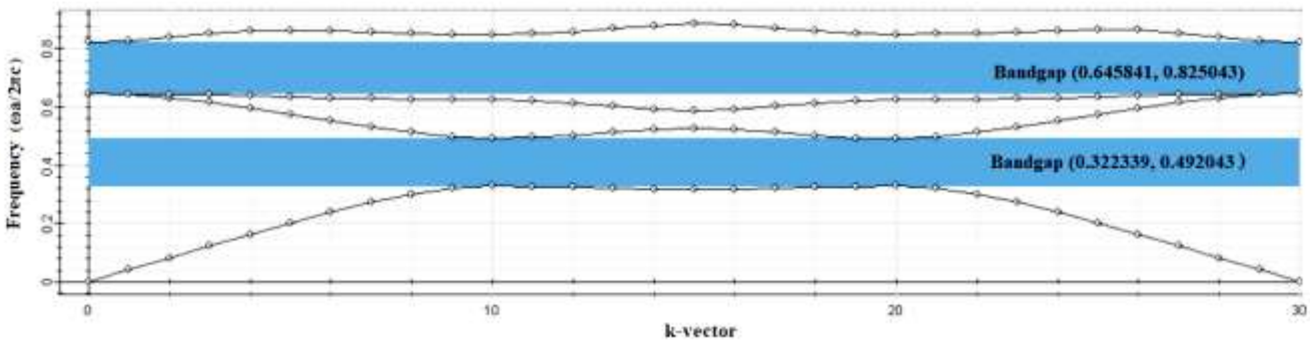

Fig. 2. Photonic bandgap structure for 17×11 Si rods in air

Table 2. Design parameters for modified AO-XOR gate

Lattice Type	Hexagonal
Lattice dimensions	17×11
Lattice Constant (a)	523 nm
Dielectric Material	Silicon (Si)
Refractive Index of dielectric	3.47
Radius of rods (r)	0.21×a = 109.83 nm
Input Power	1 mW
Wavelength	1550 nm
Footprint	42.24 μm^2

The above structure has several advantages as it is composed only of silicon material. The absence of non-linear materials leads to a less complex design with lower power consumption and the silicon-based structure increases the compatibility with existing CMOS logic system as well as with the hybrid electro-optic and future all-optical integrated circuits. The use of hexagonal lattice provides larger bandgaps and a wider bandwidth of operation. No additional control signals are used to achieve the XOR functionality. The design has ultra-compact dimensions which increases the flexibility and integration capability with other AO-devices.

4. SIMULATION RESULTS & ANALYSIS

Simulation of the structure is performed by 2D FDTD technique utilizing Synopsys RSoft CAD software to analyse the propagation of light within the device and its various performance characteristics. The open-source software by Optiwave Systems called Opti-FDTD is utilized to generate the bandgap diagram using PWE method. To compute the optical power distribution, the absorbing boundary condition of Perfectly Matched Layers (PML) is applied. To check the working of the proposed gate, a Gaussian optical source generating a continuous light signal of wavelength 1550 nm is kept at each of the input ports. A monitor is placed at output port Y in order to measure the optical intensity arriving at the output. The input power P_{IN} at ports A and B are fixed at 1 mW/ μm^2. The spatial grid has to be small in order to generate a complete simulation. This is indicated by the wavelength of the material used. For stable operation, the space time grids should follow the given condition [34],

$$c\Delta t < \frac{1}{\sqrt{\frac{1}{\Delta x^2}+\frac{1}{\Delta z^2}}} \tag{8}$$

where, Δt denotes the step time, c denotes the free space velocity of light, and Δx, Δz represents the space steps along x- and z- axis respectively.

Table 3 shows the digital as well as optical truth table for the optimized AO-XOR gate. Here, the measured output power is expressed as a fraction of the input power P_{IN}. In order to distinguish between logic 1 and logic 0 levels, the optical intensity levels of each state must be specified. In this work, power level below 0.005 P_{IN} denotes logic 0 state and power level above 0.1 P_{IN} denotes logic 1 state. The various performance metrics are computed to characterize the performance of the optimized design. The contrast ratio (CR) is a mathematical expression consisting of the output power levels for the two logic states [35]. i.e.,

$$CR\ (dB) = 10 \log_{10} (P_h/P_l) \tag{9}$$

where, P_h and P_l denotes the lowest value of optical intensity in logic high state and the highest value of optical intensity in logic low state respectively. The higher the value of CR, the easier it is to distinguish between the logic states and hence better the operation. Another parameter that determines the speed of the device is the bit rate [36]. The approximate operating bit rate of the device is given by the inverted value of response time. In addition, the dimensions of the device or the footprint is also of prime importance due to the need to integrate a large number of such devices onto a single chip. Lower response times and smaller dimensions are preferred for high-speed operation and easy integration with OICs.

Table 3. Digital and optical truth table for optimized AO-XOR gate

Input A		Input B		Output Y	
Logic state	Power level	Logic state	Power level	Logic state	Power level
0	0	0	0	0	0 P_{IN}
0	0	1	P_{IN}	1	0.139 P_{IN}
1	P_{IN}	0	0	1	0.135 P_{IN}
1	P_{IN}	1	P_{IN}	0	0.00009 P_{IN}

The proposed structure has four different operating states owing to two different inputs. Depending on the interactions between the incoming light signals, the output port produces either a high intensity signal or a low intensity signal. In the first case, the two input ports have zero intensity or logic 0 state i.e., A = B =0. Then, no light propagates through the structure giving rise to zero intensity output or logic 0 state at port Y. For the second case, the first input port has zero intensity and the second port has an input light signal of P_{IN} power i.e., A = 0, B = 1. Then, only one optical wave enters the structure and it propagates along the input waveguide towards the output Y giving rise to a logic 1 output. This is depicted in Fig. 3.

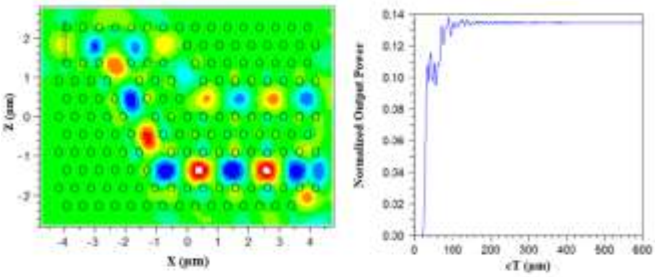

Fig 3. (a) Optical field intensity (b) normalized output power for (A, B) = 01

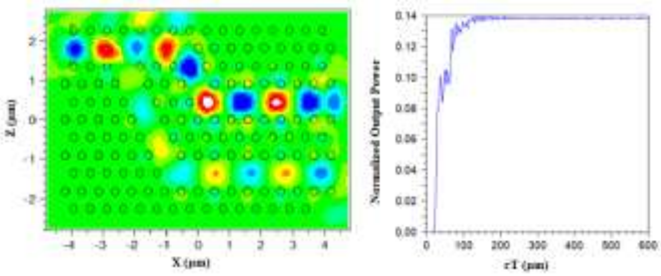

Fig 4. (a) Optical field intensity (b) normalized output power for (A, B) = 10

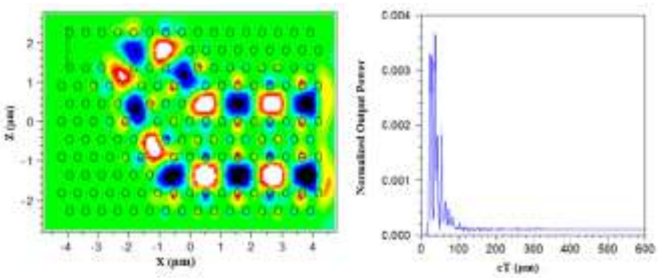

Fig 5. (a) Optical field intensity (b) normalized output power for (A, B) = 11

For the third case, the first input port has a light signal while the second port has zero intensity i.e., A = 1, B = 0. Then, only one signal travels through the structure without any interactions giving rise to logic high result. This is illustrated in Fig. 4. For the fourth case, two high intensity waves propagate along the structure. i.e., A = B = 1. In this case, the two signals travel different path lengths and undergo a change phase giving rise to a destructive interference effect. The signals get cancelled out and very low intensity corresponding to logic 0 state reaches Y. This is shown in Fig. 5.

For different values of wavelengths from 1549 nm to 1553 nm, the normalized output powers for the four different input states are studied. This is tabulated in Table 4. For A, B = 10 and 01 cases, the output port Y has high intensity light corresponding to logic 1 output. As seen from Fig. 6, the maximum values are obtained for 1550 nm of wavelength. The design shows reasonable power ratios for 1549 nm and 1551 nm as well. For A, B = 00 and 11, very low intensity or no light appears at port Y resulting in logic 0 state. As seen from Fig. 7, the lowest values are obtained for 1550 nm followed by 1552 nm. Overall, the best performance is attained for 1550 nm wavelength. The plot of CR versus input wavelength is depicted in Fig. 8. A CR value of 31.76 dB is attained by the device at 1550 nm.

Table 4: Normalized power and CR (dB) for different values of wavelength (nm)

Wavelength (nm)	Normalized Power P_O/P_{IN}				CR (dB)
	00	01	10	11	
1549	0	0.12	0.13	0.0028	16.6
1550	0	0.139	0.125	0.00009	31.76
1551	0	0.115	0.12	0.0034	25.5
1552	0	0.11	0.12	0.00066	22.5
1553	0	0.085	0.09	0.0011	19.21

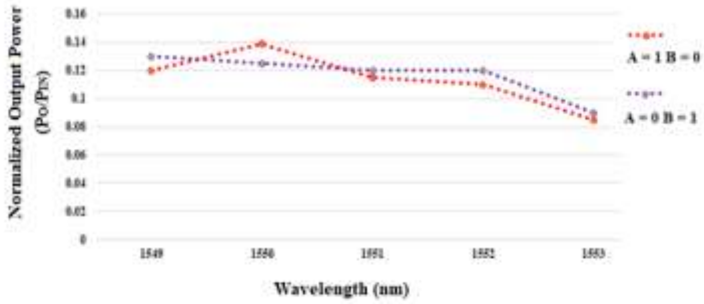

Fig 6. Plot of Normalized output power versus input wavelength (nm) for A, B = (10), (01)

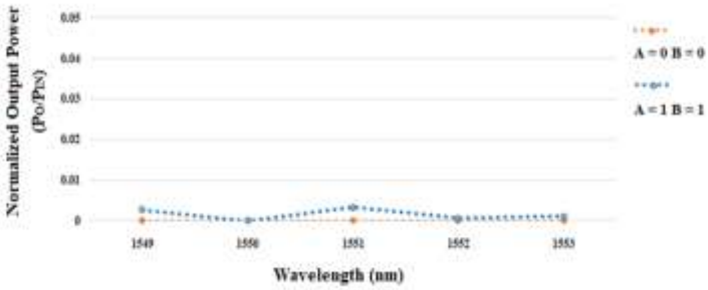

Fig 7. Plot of Normalized output power versus input wavelength (nm) for A, B = (00), (11)

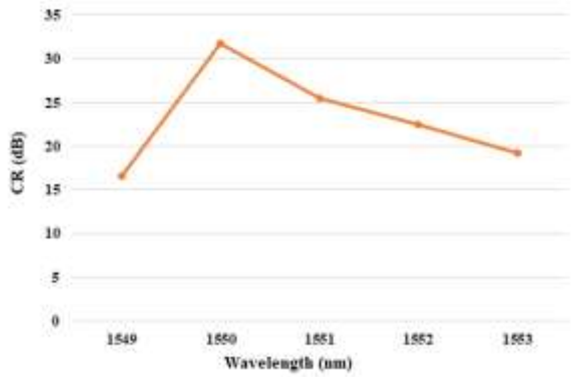

Fig 8. Variation of contrast ratio (dB) versus operating wavelength (nm)

The various structural parameters were chosen carefully after optimizing the design for achieving maximum contrast ratio with low response times. These metrics are directly affected by changes in radius of rods, operating wavelength, lattice constant and the material refractive index. The silicon rod radius is varied from 0.18a to 0.22a as shown in Table 5. The variation of bit rate and response time with Si rod radius is plotted in Fig. 9 and that of CR with Si rod radius in Fig. 10. The maximum CR value and the least response time is achieved for the radius value of 0.21a. Table 6 depicts the variation in lattice constant from 520 nm to 524 nm. The plot of response time and bit rate versus lattice constant is illustrated by Fig. 11. The highest bit rate of 2.17 Tbps and maximum CR is attained for lattice constant of 523 nm as seen from Fig. 12. The highest value of CR is achieved at a = 523 nm as seen from Fig. 12.

Table 5: CR (dB), response time (ps) and bit rate (Tbps) for different values of Si rod radius

Radius of Si rods (nm)	CR (dB)	Response time (ps)	Bit rate (Tbps)
0.18×a	6.75	0.89	1.12
0.19×a	8.94	0.68	1.47
0.20×a	16.02	0.65	1.54
0.21×a	31.76	0.46	2.17
0.22×a	17.69	0.52	1.92

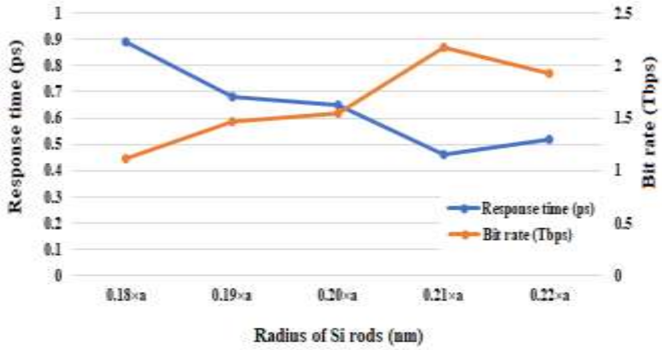

Fig 9. Variation of response time (ps) and bit rate (Tbps) versus radius of Si rods (nm)

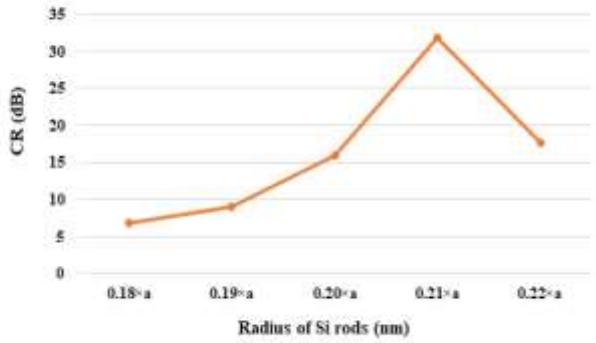

Fig 10. Variation of contrast ratio (dB) versus radius of Si rods (nm)

Table 6: CR (dB), response time (ps) and bit rate (Tbps) for different values of lattice constant, a (nm)

Lattice Constant (nm)	CR (dB)	Response time (ps)	Bit rate (Tbps)
520	25.18	0.68	1.47
521	25.7	0.5	2
522	25.3	0.49	2.04
523	31.76	0.46	2.17
524	24.35	0.6	1.66

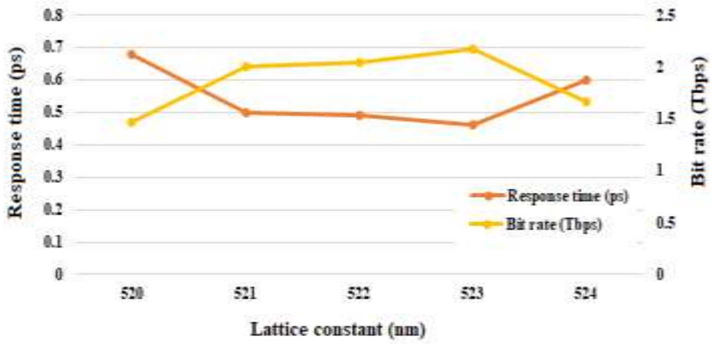

Fig 11. Variation of response time (ps) and bit rate (Tbps) lattice constant (nm)

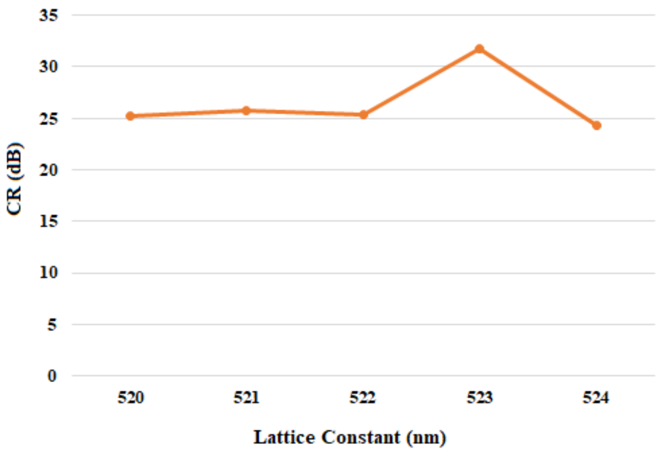

Fig 12. Variation of contrast ratio (dB) versus lattice constant (nm)

From the above plots, operational characteristics of the newly designed AO-XOR structure is optimized to attain the maximum CR, highest bit rate and the least response time. Thus, the final structure has the optimized design parameters of lattice constant 523 nm, radius 0.21×a and input wavelength 1550 nm.

The newly proposed design for AO-XOR gate has improved the already existing design and optimized the various structural parameters to attain a high contrast ratio of 31.76 dB without using any non-linear material or additional phase control elements along with a footprint of extremely low dimensions. The device is realized on wafer dimensions of 42.2 μm^2. A bit rate of 2.17 Tbps and response time of 0.46 ps is attained by structure. The entire device is composed of only silicon material which enables easy integration with hybrid electro-optic as well as upcoming OICs. Table 7 shows a comparison of the performance of the improved AO-XOR gate with existing works from the literature. It can be observed that achieving a CR above 30 dB for a structure based only on linear interference effect with extremely low dimensions and low response time (< 1ps) can be considered as a huge step towards the practical realization of a complete optical network based on integrated all-optical devices

Table 7: Performance comparison of the proposed work with existing works

Paper	Technique & Principle	Contrast Ratio (dB)	Response time (ps)	Footprint (μm^2)	Operating wavelength (nm)	Bit Rate (Tbps)
The proposed work	**Hexagonal lattice 2 D photonic crystals & Interference effect**	**31.76**	**0.46**	**42.24**	**1550**	**2.17**
E. G. Anagha et. al., 2020	Square lattice 2 D photonic crystals & Interference effect	7.16	0.4	93.5	1550	2.5
S. E. Kordi et. al., 2020	Square lattice 2 D photonic crystals & Interference effect	15	0.14	60.2	1533 - 1556	**
DGS Rao et. al., 2021	Square lattice 2 D photonic crystals & Interference effect	8.29	**	45.36	1550	**
A. Mohebzadeh-Bahabady et. al. 2018	Hexagonal lattice 2 D photonic crystals & Interference effect	19.25	0.466	252	1550	2.145
Preeti Rani et al.2015	Hexagonal lattice 2 D Photonic crystals & Interference effect	8.49	1.024	**	1550	0.976

** Not discussed

5. CONCLUSION

In this work, an optimized design of AO-XOR gate based on beam interference effect in 2D photonic crystals is proposed. The design is achieved after proper optimization of the structure parameters to attain a maximum contrast ratio of 31.76 dB. The structure possesses very low dimensions of 42.2 μm^2 with an operating speed of 2.17 Tbps. The light wave propagation within the structure is studied with the help of 2D FDTD technique. This work proves to be a potential candidate to build various combinational and sequential all-optical logic circuits for applications in the areas of optical computing and telecommunications.

Declarations
I declare that the work is carried out by all the authors and it is not published or submitted for publication to any other journals.

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Availability of data and material Not Applicable
.
Code availability Not Applicable.

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Consent to Participate Not Applicable.

Consent for Publication Not Applicable.

Author contributions All authors equally contributed for the preparation of the manuscript.

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Massimo V. Fischetti
The Editor-in-Chief
Journal of Computational Electronics – Springer

Dear Editor,

I am pleased to submit a research article entitled "Optimized Design of an All-Optical XOR Gate with High Contrast Ratio and Ultra-Compact Dimensions" for consideration of publication in Journal of Computational Electronics – Springer.

In this paper, we propose the realization of an optimized all-optical XOR gate using two dimensional photonic crystals. Owing to its high contrast ratio, ultra-compact dimensions and purely silicon-based structure, the proposed work promises to be a potential candidate to build various combinational and sequential optical logic circuits for the future optical integrated circuits. These logic circuits have wide applications in the areas of all-optical computing and high-speed communications systems. The highlight of this work is the design of extremely compact photonic crystal-based structure with contrast ratio and high data rates suitable for operation in the telecommunication wavelength of 1550 nm.

This work is technically significant because it focuses on integration aspects for the design of future all-optical networks with high speed and efficiency to ultimately overcome the electronic bottle neck problem of the conventional digital electronics network. The paper should be of interest to readers in the areas of Photonics, Optical Computing and Optoelectronics as it contains the design aspects of all-optical logic devices and its integration for developing optical integrated circuits for a wide variety of applications

We believe that this manuscript is appropriate for publication by Journal of Computational Electronics – Springer. This manuscript has not been published and is not under consideration for publication elsewhere. We have carefully followed your manuscript preparation guidelines for formatting and style, and we look forward to receiving your valuable comments on our efforts.

Please address all correspondence concerning this manuscript to me at jeyachitra@nitt.edu.

Thank you for your consideration of this
manuscript.

I look forward to your reply.

Sincerely,

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