Modeling and Design of Mott Selector for ReRAM Based Non-Volatile Memory Cell in Crossbar Architecture

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Modeling and Design of Mott Selector for ReRAM Based Non-Volatile Memory Cell in Crossbar Architecture

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Abstract

In this work, we developed a model for a non-volatile memory cell, based on the electrical model for TiO_X/HfO_x ReRAM cell and the hybrid electro-thermal model of VO_2 Mott selector developed recently by our team. Both models are calibrated and validated with experimental data, and the operating characteristics of one-selector-one-ReRAM (1S1R) memory cell are studied. The length of the selector layer is varied as a design parameter to meet the design requirements for proper read, write and erase operations. Simulation results suggest that modified selector cell with 60 nm length of VO_2 layer meets all the requirements for proper operations with the cell write voltage of 1.6 V and erase voltage of 2.5 V. The access time for this structure is studied by benchmarking with experimental data and is estimated to be less than 10.5 ns for write operating and less than 16ns for the erase operation.

Keywords: Non-Volatile Memory (NVM), Modeling, Memory selector, Insulator to Metal Transition (IMT), Vanadium Oxide, Resistive Random Access Memory (ReRAM).

1. Introduction

Resistive random access memory (ReRAM) is a competitive candidate for the next-generation of non-volatile memories due to its excellent scalability, fast switching speed, simple device fabrication, and two-terminal structure. This device has the potential to be used in 3D-stacked memories [1]-[5]. It also received significant attention for neurocomputing hardware due to nonlinear characteristics which can emulate the spike signal communicated between neurons [6]-[8]. Conversely, crossbar architecture provides great potential for high-density ReRAM array implementation, in which the cell size could be as small as $4F^2$ (F is the minimum feature size) [9]. However, the crossbar architecture has a significant drawback with pure passive ReRAM cells. Parasitic current paths through neighboring cells, which are referred to as sneak paths, may cause leakage and may alter unselected memory cells during read or write operations [10]. A selector device connected in series with the memory element is used to solve the sneak path issue. Various types of selector devices have been proposed, including diodes (1D1R), CMOS transistors (1T1R) [11], BJT transistors (1BJT1R), or even a second ReRAM cell [12]. Among those methods, the 1T1R and 1BJT1R have complex fabrication process [13] and require three-terminal device which is not fully compatible with crossbar structure. Mott devices based on transition metal oxides exhibiting conductivity switching or insulator to metal transition (IMT) at room temperature are one of the promising candidates for selector devices in crossbar architecture that has a switching time in the order of a few ns. There are several studies investigating selector properties of Vanadium dioxide (VO_2) and Niobium dioxide (NbO_2) as Mott selector devices [14]-[17]. A Mott selector connected in series with a ReRAM forms a 1S1R memory cell structure. The device modeling community has tried to develop comprehensive models to accelerate the analysis, design, and development of NVMs. The ReRAM models usually aimed to simplify the complex process of ion and vacancy migration and formation of a single dominant conductive filamentary path [18]-[22]. Among those, Stanford-PKU compact Verilog-A model [18] is a viable choice to simulate the ReRAM along with other circuit elements [18]. For Mott selector modeling, there are two main mechanisms proposed in the literature to explain the IMT: (I) Structural changes induced by Joule

heating (thermal) [23] and (II) Field assisted carrier generation (electrical) [24]. We have recently proposed an analytical hybrid model which takes into account the interaction of both Joule heating and field assist transition [25]. In this model, the contribution of electric field, temperature, and carrier concentration as main parameters affecting the transition is considered [25]. The main advantage of the proposed model is that it can estimate the device characteristics from pure thermal transition to pure electrical transition as the design parameter varies, which is crucial feature for a design oriented model.

In this paper, we used the proposed model [25] calibrated with an experimental device [26] along with the Stanford-PKU ReRAM model [18] calibrated with experimental data [19] to design a 1S1R NVM cell for crossbar structure. Then we used the proposed model to check the design requirements and make the cell more robust against sneak path leakage.

This paper is arranged as follows: In section 2, device structures, modeling approaches, and models calibration for ReRAM and Mott Selector are presented and design requirements for proper read, write and erase operations are discussed. Section 3 illustrate simulation results and discusses the improvement of the selector by adjusting the VO_2 layer length to meet the design requirements. Finally, Section 4 concludes the paper.

2. Device structure and modeling

2.1 ReRAM Element

Fig. 1(a) shows the schematic cross-section of the ReRAM element, obtained from the experimental report [18], which consists of TiN/TiO_X(~5 nm)/HfO_x(3.3 nm)/Pt. The HfO_x is the active ReRAM layer sandwiched between TiO_x and the bottom electrode.

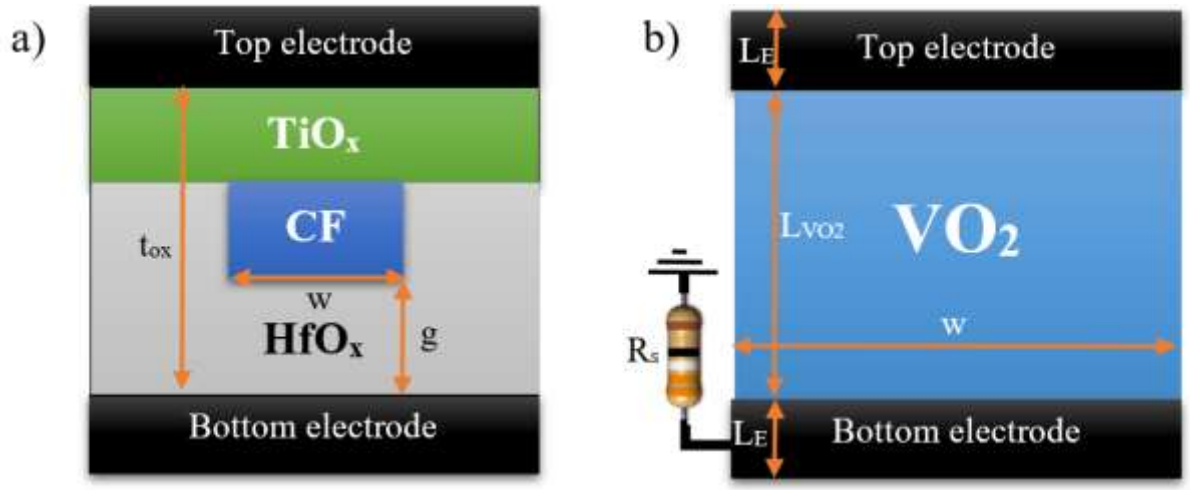

Fig. 1 (a) schematic cross-section of ReRAM element, CF stands for conductive filament formed in response to applied voltage in the middle part of HfO_x oxide, (b) schematic cross-section of VO_2 Mott selector element.

The operation of ReRAM is described by conductive filament (CF) formation as a result of oxygen ion movement, vacancy generation, and recombination events [6]. In the Stanford-PKU model [18], a single dominant filament is assumed, and the core variable is the gap size (g) between the filament and

the bottom electrode which controls the resistance of the cell. The time derivative of "g" is related to oxygen ions activation energy barrier and the applied voltage as:

$$\frac{dg}{dt} = -v_0 \times \exp\left(-\frac{E_a}{kT}\right) \times \sinh\left(r \times \frac{a_0}{t_{ox}} \times \frac{qV}{kT}\right) \quad (1)$$

where, "V" is applied voltage, "E_a" is active energy for vacancy generation, a_0 is the hopping site distance, t_{ox} is the oxide thickness, "k" is the Boltzmann constant, "T" is ambient temperature, and "υ_0" is a fitting parameter. Besides, as the current flows, the temperature is updated due to the self-heating effect, and the electric field in the gap region is increases as the gap size decreases. As a result, a nonlinear and hysteresis I-V characteristics is observed. Details of model equations are presented in [18]. We have implemented this model in MATLAB and calibrated it with the experimental device [19], using parameters and constants listed in Table 1.

Table 1. List of parameters and constant values used for ReRAM model calibration [18]

Ti	Descriptions	Value
$\mathbf{L_0}$	Active ReRAM layer length	3 nm
$\mathbf{w_0}$	Initial Filament width	0.5 nm
$\mathbf{E_a}$	Activation energy	0.7 eV
$\mathbf{I_0}$	Hopping current density	10^{13} A/m^2
k	Boltzmann constant	8.61733×10^{-5} eV/K
$\mathbf{V_0}$	Characteristic voltage	0.4 V
$\boldsymbol{\upsilon_0}$	Distance between Oxygen two neighbor vacancy	0.25 nm
$\mathbf{g_0}$	Initial gap length	{L_0, 0}
q	Charge of unit electron	1.6×10^{-19} C
$\mathbf{T_0}$	Ambient temperature	300 K
$\mathbf{R_{th}}$	Effective thermal resistance	5×10^5 K/W
$\mathbf{R_H}$	Oxide parasitic resistance	200 MΩ
$\mathbf{R_L}$	Electrode contact resistance	20 Ω
$\mathbf{R_{ON}}$	Low resistance state resistivity	10 KΩ
$\mathbf{R_{OFF}}$	High resistance state resistivity	1 MΩ
ρ	CF resistivity	19.64 μΩ·m

Fig. 2 (a) compares the I-V characteristic for the "Set" (write) operation obtained from the model with the experiments. This result confirms that the model fits very well with the experimental report. Assuming that there is no filament in the structure initially, and the ReRAM is in the insulator phase, the electrical potential applied to the device is increased from 0 to 2.0V to perform the write operation. The model suggests that the filament is formed entirely around 1.6V, and a jump in current is observed. In the backward path, the electrical conductivity remains high, which confirms the non-volatile storage characteristics demonstrated by the model. Fig. 2 (b) shows I-V characteristic ReRAM during "Reset" (erase) operation obtained by the model and compared with experiments [18]. The sweep begins with the device in the "Set" state, and the filament is entirely formed inside the device, and the electrical resistance is about 10KΩ. The voltage is swept from 0 to -2.5V to perform the erase operation. The filament is removed entirely at -2.5V, and the electrical resistance jumped to 1MΩ. A noticeable decrease in electrical current is observed during the backward sweep from -2.5V to 0. Again, the model shows perfect agreement with experimental data. The slight difference is attributed to the current limiter used in the experimental report.

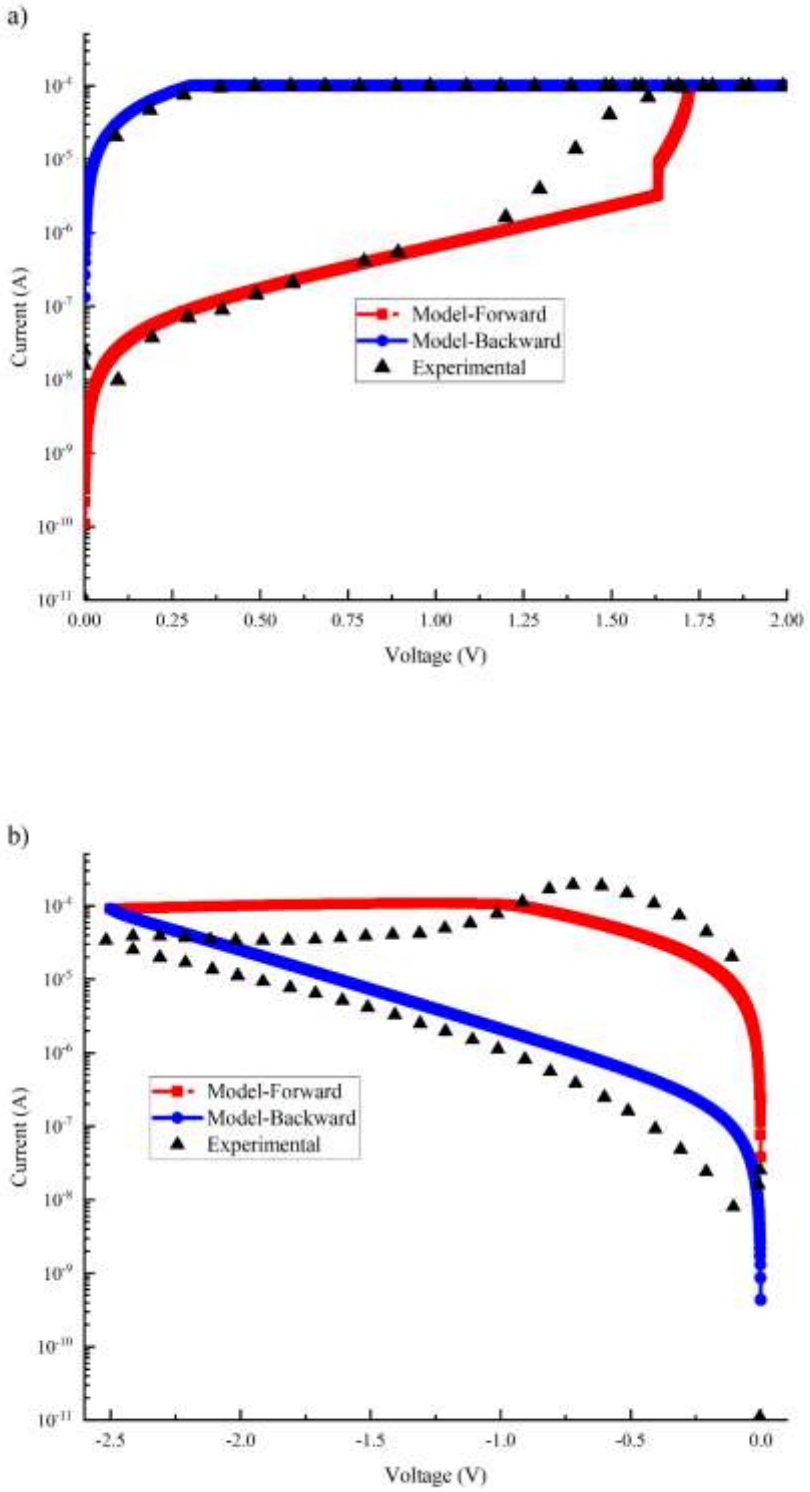

Fig. 2 I-V characteristic of ReRAM obtained by the model compared with experimental results. (a) "Set" or write operation. The red line is the model characteristics in the forward direction (0 to 2.0 V), and the blue line corresponds to model characteristics in the backward sweep. Black triangles represent the experimental data. (b) "Reset" or erase operation. The red line is the model characteristics in the forward direction (0 to -2.5 V), and the blue line corresponds to model characteristics in the backward sweep. Black triangles represent experimental results.

2.2 VO_2 Mott Selector

Fig. 1(b) demonstrates the schematic cross-section of the VO_2 Mott layer sandwiched between two electrodes. Experimental implementation of this structure as Mott selector is reported in [26]. We have proposed an electro-thermal hybrid model in [25], which captures two main mechanisms responsible for Mott transition: (I) Joule heating, and (II) Field assisted carrier generation, in the form of Poole-Frankel effect. The model for Joule heating is based on 3-D heat transfer equations and the current continuity, in the Cartesian coordinates:

$$\frac{\partial}{\partial t}(cT)=\frac{\partial}{\partial x}\left(K\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(K\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(K\frac{\partial T}{\partial z}\right)+\sigma\left[\left(\frac{\partial V}{\partial x}\right)^2+\left(\frac{\partial V}{\partial y}\right)^2\right] \tag{2}$$

$$div(j)=\frac{\partial}{\partial x}\left(\sigma\frac{\partial V}{\partial x}\right)+\frac{\partial}{\partial y}\left(\sigma\frac{\partial V}{\partial y}\right)+\frac{\partial}{\partial z}\left(\sigma\frac{\partial V}{\partial z}\right)=0 \tag{3}$$

$$div(j)=\frac{\partial j}{\partial x}+\frac{\partial j}{\partial y}+\frac{\partial j}{\partial z} \tag{4}$$

where "c" is the heat capacity, "K" is the thermal conductivity, "σ" is the electrical conductivity, "T" is the temperature, "j" is the current density, and "V" is the electrical potential. For field assist transition, the model is based on Poole-Frenkel phenomena, which relates carrier density to the applied electric field and other device parameters as below:

$$n=N_0\exp\left(-\frac{W-\beta\sqrt{E}}{k_BT}\right) \tag{5}$$

where "N_0" is the reference value of carrier concentration, "W" is the conductivity activation energy, and "β" is Poole-Frenkel constant, and "E" is the applied electric field. In this mechanism, transition take place when carrier density reaches the Mott criterion. The device length is divided into 100 segments, and for each segment, the switching threshold for both mechanisms is monitored as the applied voltage is swept and main parameters including the temperature, carrier density, and electric field interact. The VO_2 layer length (L_{VO2}) is a key parameter affecting the switching dynamics. Details of the model were presented in [25].

Table 2. List of experimental device parameters and model calibration parameters for VO_2 Mott selector [26]

Parameters	Descriptions	Value
$\mathbf{L_{VO2}}$	VO_2 layer length	20nm
$\mathbf{L_{TE}}$	Electrode length	100nm
A	Active area	5×10^4 nm^2
W	VO_2 layer width	250nm
β	Poole-Frenkel constant	1.2135×10^{-24}
$\mathbf{T_A}$	Ambient temperature	300K
$\mathbf{T_{IMT}}$	IMT temperature	326K
$\mathbf{T_{MIT}}$	MIT temperature	322K
$\mathbf{n_c}$	Mott critical concentration	3×10^8 cm^{-3}
K	Thermal conductivity	{4, 6} W/K.m
$\mathbf{R_{ON}}$	Metallic phase resistivity	110Ω
$\mathbf{R_{OFF}}$	Insulator phase resistivity	60KΩ
$\mathbf{R_S}$	Series resistor	250Ω

We calibrated the proposed model with the experimental device [26], and the device parameters and model calibration parameters are listed in Table 2. The reported VO_2 has a 20nm length, and the transition voltage is about 0.35V. At this conditions, the applied electric field is more than 10^5 V/cm, and the dominant switching phenomenon is Poole-Frankel. Fig. 3 shows the I-V characteristics of this VO_2 layer obtained by the model compared with the experiment, which indicates excellent agreement.

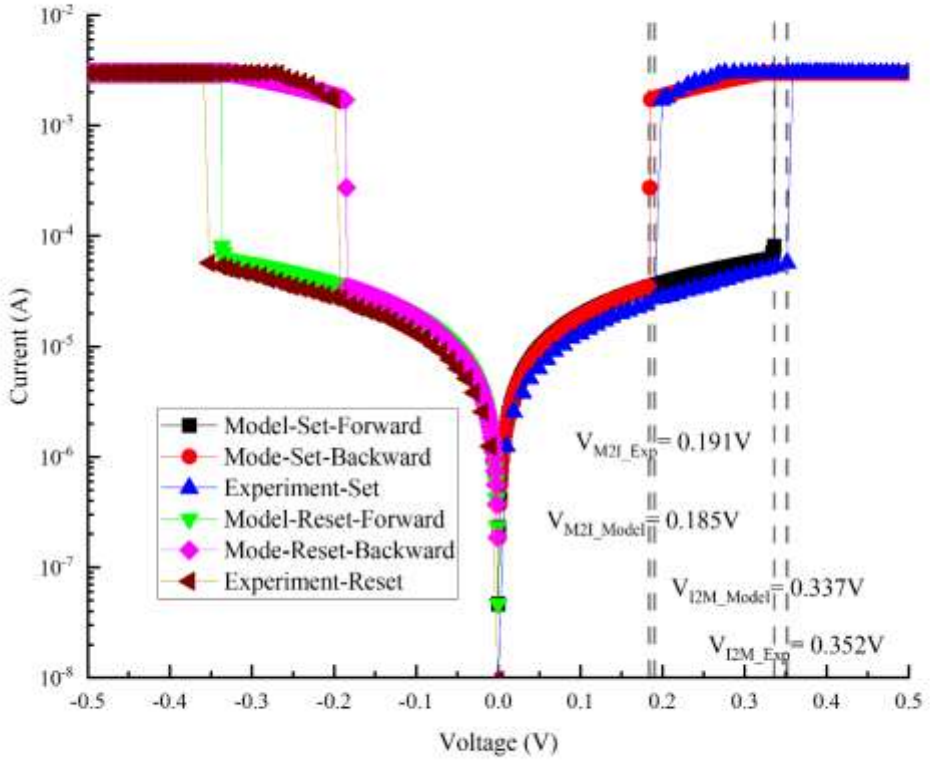

Fig. 3 I-V characteristic of VO_2 layer IMT transition obtained by the model during forward and reverse sweep and compared with experimental data [26].

The VO_2 bulk is in the insulator state at the beginning (V=0). During forward sweep, IMT switching is observed at 0.35 V. This means that the selector device turns "ON" at this voltage. In the backward path, the switching is observed at 0.19 V. This shows that the model predicts volatile characteristics of the Mott device. The proposed selector device has high current drive capability, therefore in the series combination of selector and ReRAM, the ReRAM limits the cell current. Fig. 3 indicates the VO_2 layer has a bipolar and symmetric I-V characteristics with respect to the applied voltage, which is an important selector feature for both Set and Reset operations

2.3 Design requirement for crossbar operation

A 1S1R memory cell in crossbar architecture is illustrated in Fig. 4 (a). Each cell is addressed for read and write operations by applying a voltage between the selected bit-line on the top and the word-line on the bottom. To select a cell properly, the main concern is the status of unselected neighboring cells. To avoid sneak path leakage during read, write and erase operations, the selector of the unselected

cells should be in the insulator or OFF state. Consequently, it is mandatory to apply limited voltages to word lines and bit lines of unselected cells. Kim et al. [27] proposed V/2 and V/3 schemes for the correct operation of the crossbar architecture.

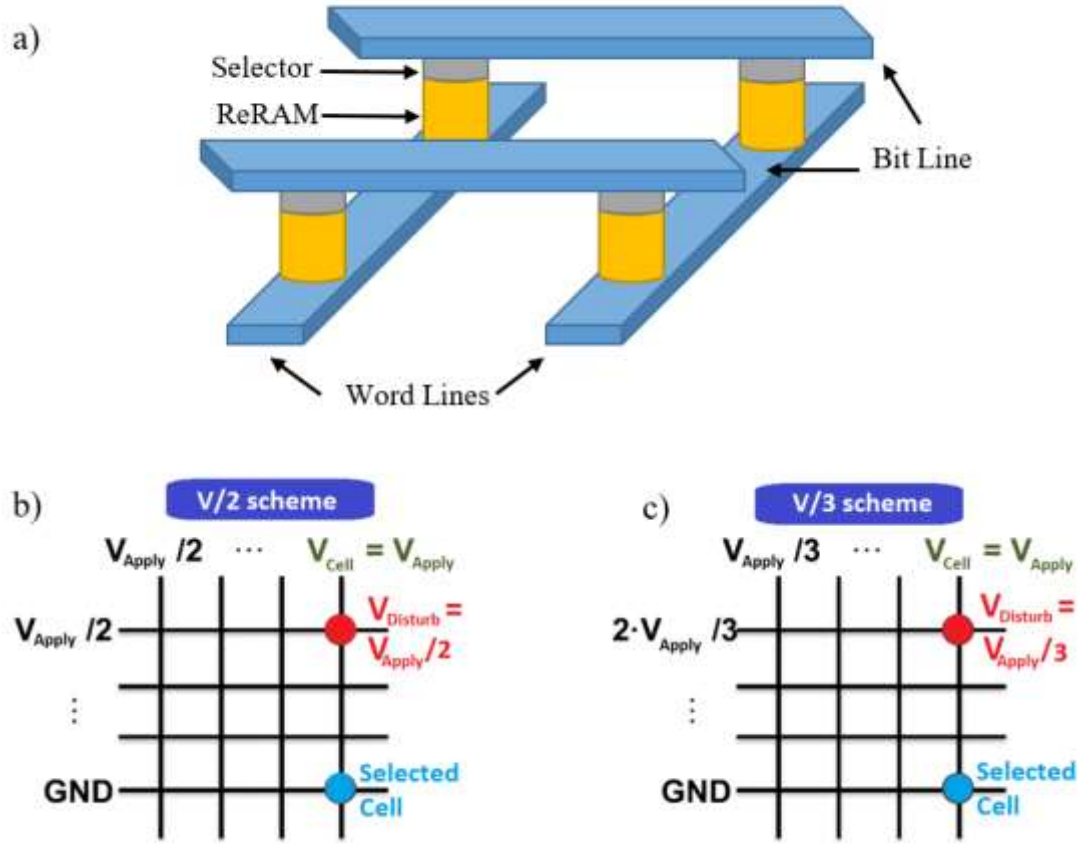

Fig. 4 (a) A simple Crossbar architecture with four 1S1R cells that word and bit lines are used for addressing. (b) V/2 scheme, (c) V/3 scheme addressing 1S1R cells to perform read, write, and erase operation.

The V/2 scheme is demonstrated in Fig. 4 (b). During read or write operation, full voltage (V_{Apply}) is applied to the selected cell, and the $V_{Apply}/2$ is delivered to all other unselected word-lines and bit-lines. Maximum voltage applied to unselected cells that share either the word-line or the bit-line with the selected cell would be $V_{Apply}/2$ which is called disturb voltage. Therefore a significant requirement for correct operation is that the disturb voltage should be lower than the threshold voltage for IMT transition of the selector to avoid sneak path leakage. Similarly, Fig. 4 (c) illustrated the V/3 scheme in which V_{Apply} and "0" are applied to selected word-line and bit- line respectively, while $V_{Apply}/3$ and $2\times V_{Apply}/3$ are delivered to unselected word-lines and bit-lines, respectively. In this scheme, the disturb voltage in worst-case is reduced to $V_{Apply}/3$. The main requirement is to ensure that unselected cell's selector does not turn ON by the disturb voltage, even if its ReRAM is in a low resistance state (LRS), while the selected cell's selector is switched ON, even if its ReRAM is in high resistance state (HRS). In general V/3 scheme is more flexible and provides a better margin; however it requires three supply voltages and is more complicated. Another critical design consideration is to limit the maximum current flow of the selected word-line to avoid electro-migration phenomena. Therefore, the maximum suitable current is limited to 135μA, assuming 30×30 nm^2 line area for a Cu metal line. Table 3 summarizes the requirements for the correct operation of the 1S1R cell for both $V_{Apply}/2$ and V_{Apply} /3 schemes.

Table 3. Design requirement and limitation for correct read, write and erase operation of a 1S1R cell in crossbar structure based on V/2 and V/3 operating schemes

Scheme	Operation	Condition I	Condition II	Condition III
V/2	read	$V_{read} > V_{IMT}$	$V_{IMT} > V_{read}/2$	Maximum acceptable current ≤ 135 μA
	write	$V_{write} > V_{Set\_ReRAM}$	$V_{IMT} > V_{write}/2$	
	erase	$\|V_{erase}\| > \|V_{Reset\_ReRAM}\|$	$V_{IMT} > \|V_{erase}\|/2$	
V/3	read	$V_{read} > V_{IMT}$	$V_{IMT} > V_{read}/3$	
	write	$V_{write} > V_{Set\_ReRAM}$	$V_{IMT} > V_{write}/3$	
	erase	$\|V_{erase}\| > \|V_{Reset\_ReRAM}\|$	$V_{IMT} > \|V_{erase}\|/3$	

3. Simulation results and discussion

3.1 Results and Analysis of 1S1R Memory

Simulation results for the 1S1R cell presented in Fig. 4(a) based on the specifications of VO_2 selector [26] and ReRAM [19] is shown for "write (set)" and "erase (reset)" operations in Fig. 5 and Fig. 6, respectively. Fig. 5(a) shows the I-V characteristics of the selector and the ReRAM elements separately, and Fig 5(b) shows the I-V characteristics of the complete 1S1R cell during SET operation. We assumed that the ReRAM is in HRS initially (at V= 0V). Based on simulation results, the selector turns "ON" at 0.39V instead of 0.34V while the "Set" voltage for the ReRAM does not change from 1.63V; this is because the voltage drops over the selector is obtained from resistance division between two components. The memory cell selector turns "OFF" during the backward sweep at 0.125V, which called hold voltage.

Fig. 6(a) shows the I-V characteristics of the selector and the Mott elements separately during "Reset", and Fig. 6(b), shows the I-V characteristics of the 1S1R cell obtained from simulation. The "Reset" operation is performed when the ReRAM is in LRS. A current jump observed at V= -0.39V during forward sweep is the signature of selector turns "ON" (IMT transition). This jump is small because of the selector's high drive capability. The complete erase operation is performed when the voltage reaches -2.5V. Therefore, a low current level is observed during backward sweep in Fig. 6(b).

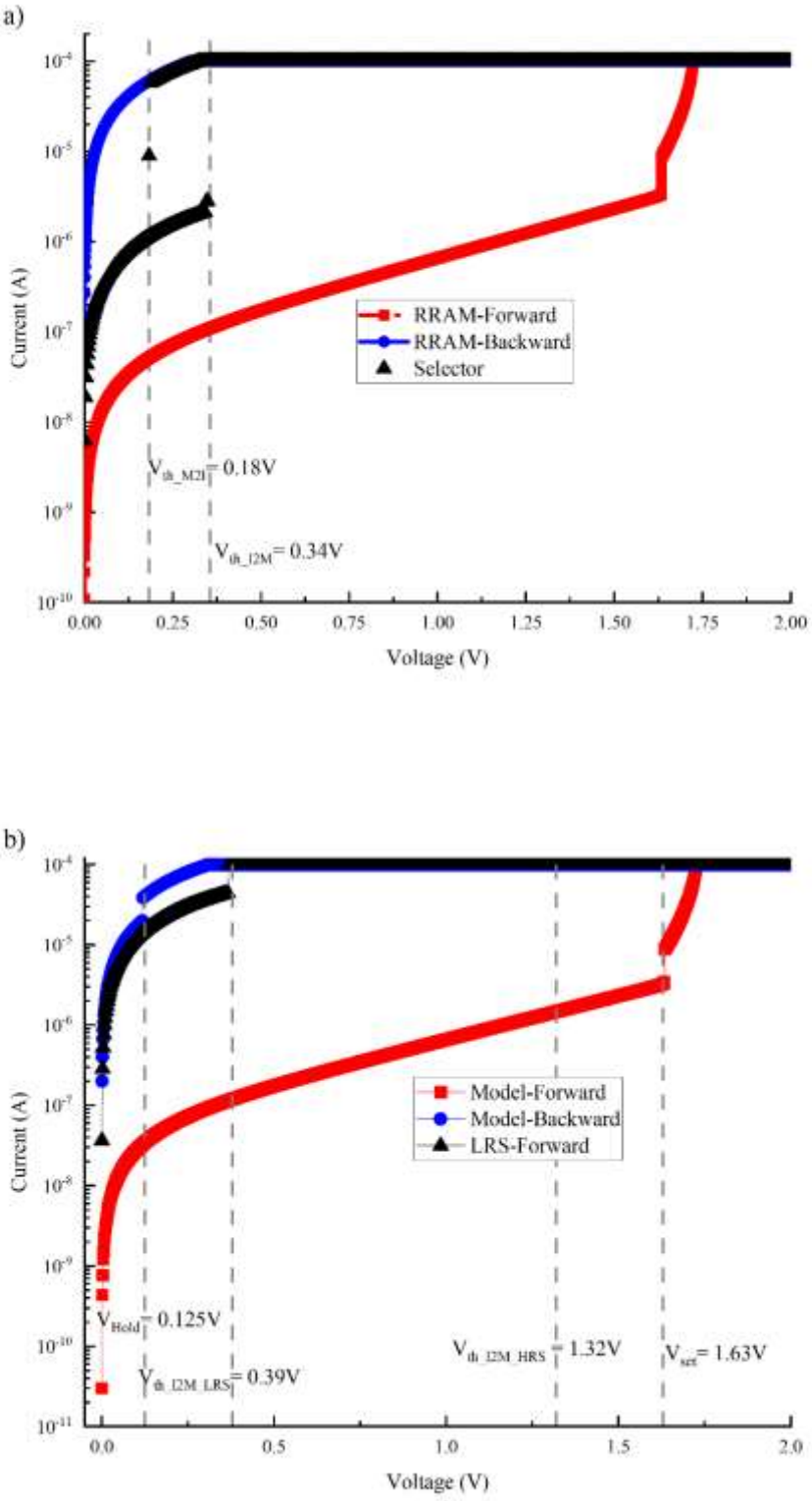

Fig. 5 Results obtained from simulation of "Set" operation for VO_2 selector [26] and ReRAM [18]. (a) I-V characteristics the selector and the ReRAM elements separately (b) I-V characteristics of the 1S1R cell (the selector with the ReRAM). Red squares represent the forward sweep from 0 to 2.0V, and blue circles show the backward sweep from 2.0V to 0. The black triangles represent the forward sweep voltage from 0 to 2V for a cell in LRS mode

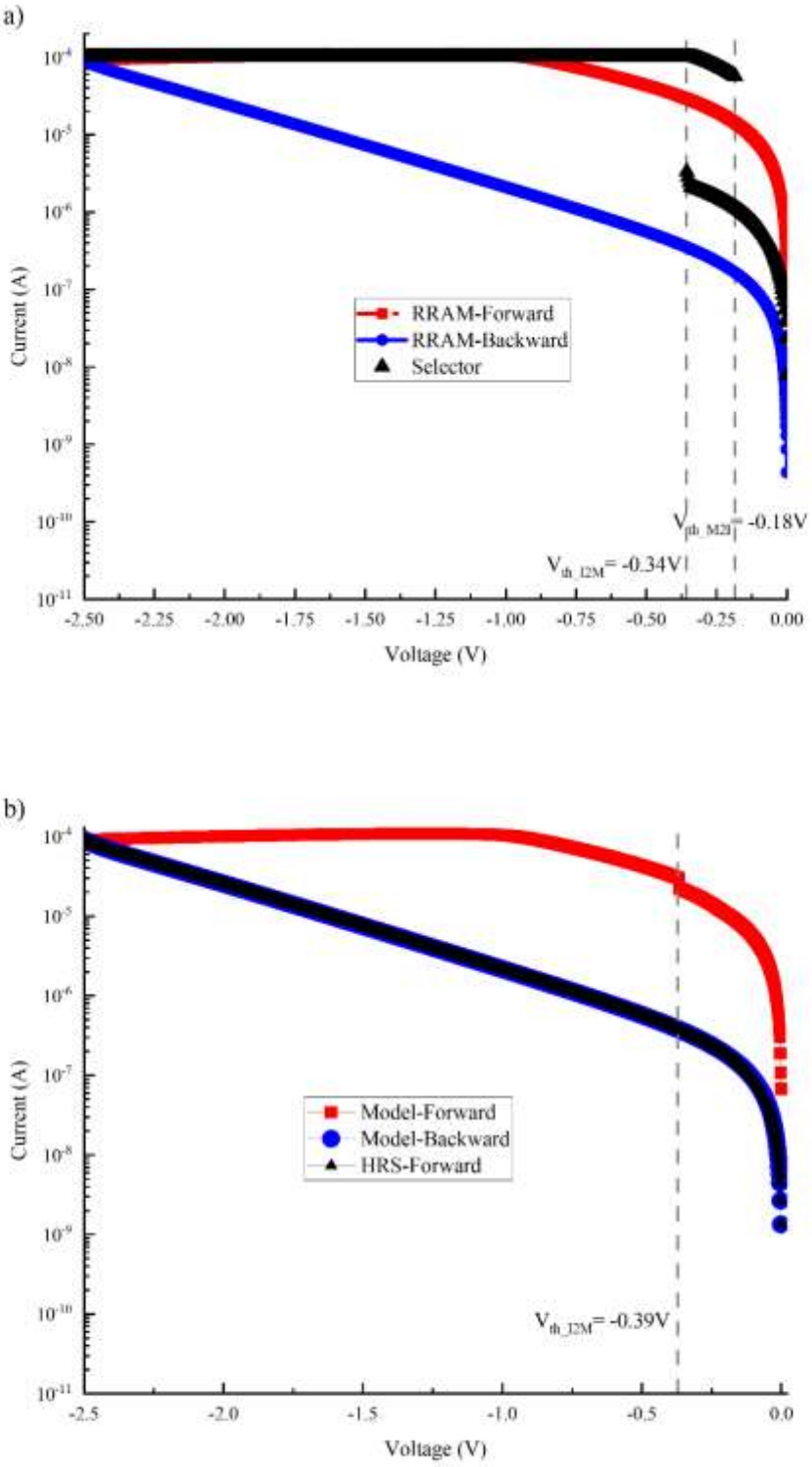

Fig. 6 Results obtained from simulation of "Reset" operation for VO_2 selector [26] and ReRAM [18]. (a) I-V characteristics the selector and the ReRAM elements separately (b) I-V characteristics of the 1S1R cell (the selector with the ReRAM). Red squares represent the forward sweep from 0 to -2.5V, and blue circles show the backward sweep from -2.5V to 0. The black triangles represent the forward sweep voltage from 0 to -2.5V for a cell in HRS mode.

The design requirements for the integrated 1S1R structure are summarized in Table 4. Design requirements are meet for the read operation in both V/2 and V/3 schemes. However, the write and erase requirements are not meet. For a correct write operation, the selector should be OFF in the worst case for the applied $V_{write}/2$ or $V_{write}/3$. But since V_{write}=1.63V. This condition cannot be met by the proposed selector because it turns on at 0.39 V, which leads to the formation of the sneak paths. For erase operation, the situation is even worse because V_{erase}= -2.5V. Consequently, the proposed structure does not work correctly in a crossbar structure, and a modification is required.

Table 4. Design requirement analysis for read, write and erase operations of 1S1R cell with V/2 and V/3 schemes

Scheme	Operation	Condition I	Condition II	Condition III	Operating Voltage Range
V/2	read	V_{read} > 0.39V	0.39V > $V_{read}/2$	**Maximum acceptable current ≤ 135 µA**	**0.4V – 0.65V**
	write	V_{write} > 1.63V	0.39V > $V_{write}/2$		**Not meet**
	erase	$\|V_{erase}\|$ > 2.5V	0.39V > $\|V_{erase}\|$ /2		**Not meet**
V/3	read	V_{read} > 0.39V	0.39V > $V_{read}/3$		**0.4V – 1V**
	write	V_{write} > 1.63V	0.39V > $V_{write}/3$		**Not meet**
	erase	$\|V_{erase}\|$ > 2.5V	0.39V > $\|V_{erase}\|$ /3		**Not meet**

3.2 Modified 1S1R Cell Characteristics

To meet the design requirements for write and erase operations, we propose to modify the selector cell based on our electro-thermal model [25] briefly described in section 2.2. The key idea is to increase the threshold for undesirable turn “ON” of the neighboring cell's selectors. To achieve this, we increase the length of the VO_2 layer (L_{VO2}). This reduces the electric field over to the selector for the same applied voltage. Other parameters are remained unchanged to have a minimum deviation from the reference structure. The length of the VO_2 layer is increased from 20nm to 40nm, 60nm, and 80nm. I-V characteristics of the modified selectors are illustrated in Fig. 7. The IMT threshold voltage is increased from 0.34V to 0.68V, 1.01V, and 1.35V for the samples with L_{VO2} (nm) = (40, 60, and 80), respectively. Furthermore, the MIT switching threshold and the width of the hysteresis loop are also increased with the VO_2 layer length. These results provide a degree of freedom to design the 1S1R cell according to the specified requirements.

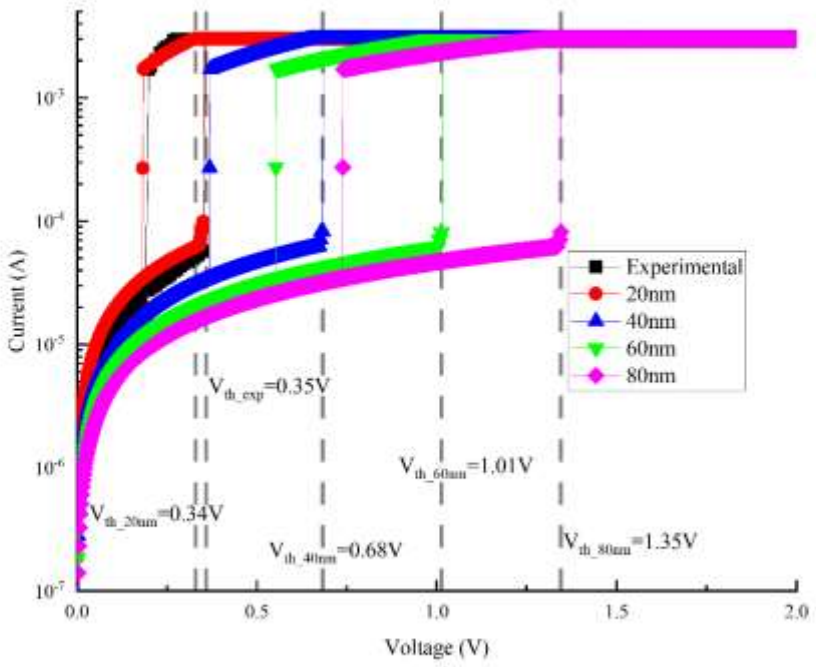

Fig. 7 I-V characteristic of experimental 20nm VO_2 selector [26] compared to the simulation results based on the electro-thermal model [25] for the selector with VO2 length of 20nm, 40nm, 60nm, and 80nm.

The "Set" (write) operation and "Reset" (erase) operation of the modified 1S1R cell for the above-mentioned selector lengths are illustrated in Fig. 8. For a write operation, the ReRAM element is in the HRS at the beginning, and the applied voltage is increased from 0 to 2V. The selector turns on at V_{th-IMT} (V) = (0.39, 0.73, 1.06, 1.37) for the cells with L_{VO2} (nm) = (20, 40, 60, 80) respectively. After selector switching, the cells are almost similar because the conductance of VO_2 layers in the metallic phase is negligible compared to the ReRAM cell, therefore V_{write}=1.63V for all cells. In the backward sweep and when the ReRAM is in LRS, the MIT threshold voltages are increased monotonically V_{hold} (V) = (0.125, 0.30, 0.46, 0.61) for the samples with L_{VO2} (nm) = (20, 40, 60, 80) respectively as shown in Fig. 8(a).

Fig. 8(b) demonstrates the erase operation when the ReRAM is in LRS. The selector's absolute turn-on threshold voltage is increased from 0.39V for the original sample with L_{VO2}=20nm to 0.73V, 1.06V, and 1.37V for the samples with L_{VO2} (nm) = (40, 60, and 80) respectively, while the erase voltage remains -2.5V. The reason is that the voltage drop over the Mott selector in metallic phase is negligible compared to the ReRAM during erase operation.

Table 5, summarize the design requirements for proper read, write and erase operation in all modified 1S1R structures.

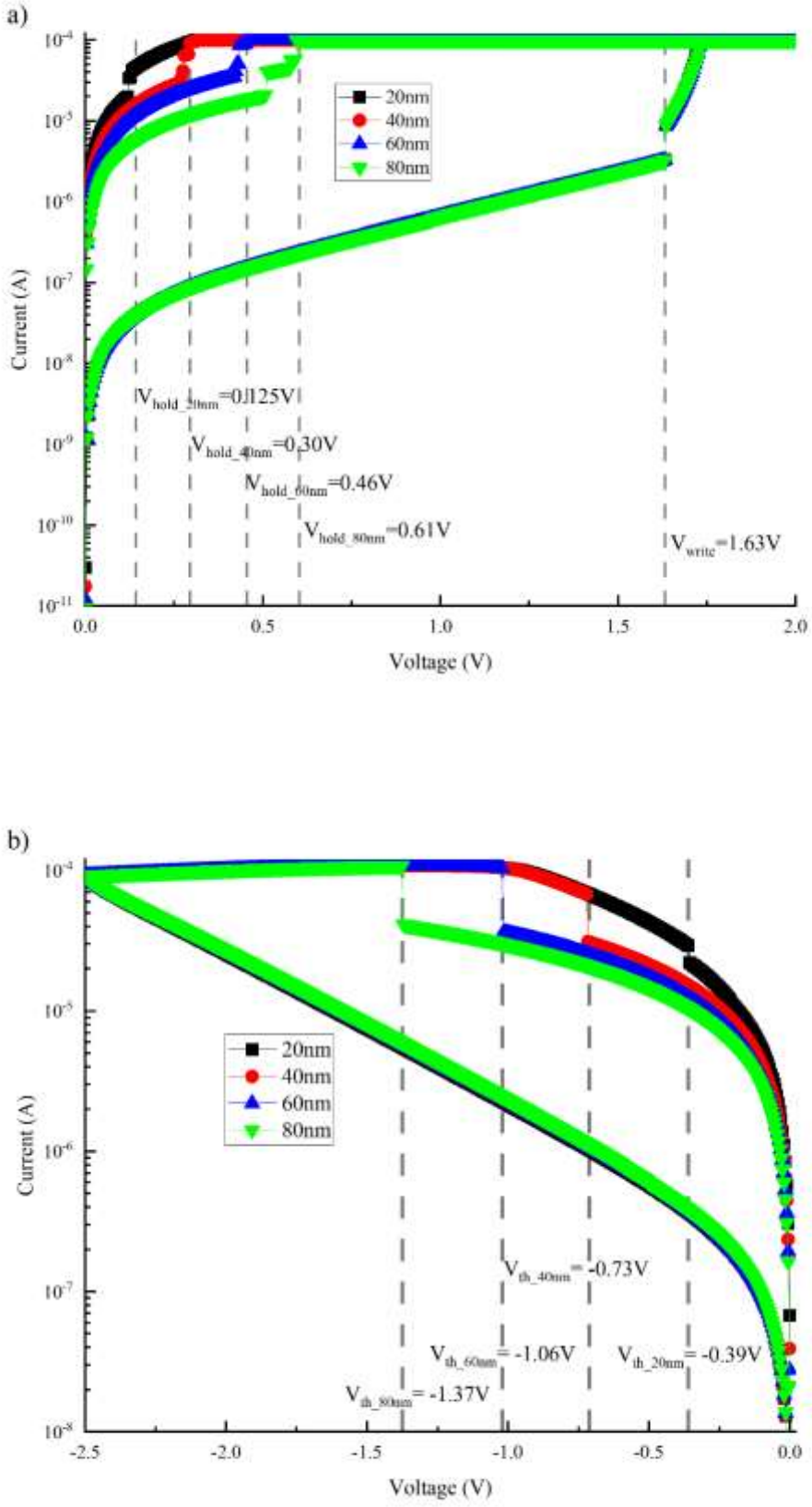

Fig. 8 I-V characteristic of modified 1S1R cells with the selector VO_2 lengths of 20nm, 40nm, 60nm, and 80nm (a) The "Set" or write operation, (b) The "Reset" or erase operation.

Table 5. Design requirement analysis for read, write and erase operations of modified 1S1R cells with the selector length of 40nm, 60nm, and 80nm and for V/2 and V/3 schemes for the modified 1S1R structure in a Crossbar architecture with V/2 and V/3 schemes

VO_2 Length	Scheme	Operation	Condition I	Condition II	Condition III	Defined voltage range (absolute)
40nm	V/2	read	$V_{read} > 0.73V$	$0.73V > V_{read}/2$	**Maximum acceptable current ≤ 135 µA**	**0.75V – 1.3V**
		write	$V_{write} > 1.63V$	$0.73V > V_{write}/2$		**Not meet**
		erase	$\|V_{erase}\| > 2.5V$	$0.73V > \|V_{erase}\|/2$		**Not meet**
	V/3	read	$V_{read} > 0.73V$	$0.73V > V_{read}/3$		**0.7V – 1.9V**
		write	$V_{write} > 1.63V$	$0.73V > V_{write}/3$		**1.7V – 1.9V**
		erase	$\|V_{erase}\| > 2.5V$	$0.73V > \|V_{erase}\|/3$		**Not meet**
60nm	V/2	read	$V_{read} > 1.04V$	$1.06V > V_{read}/2$		**1.1V – 1.9V**
		write	$V_{write} > 1.63V$	$1.06V > V_{write}/2$		**1.7V – 1.9V**
		erase	$\|V_{erase}\| > 2.5V$	$1.06V > \|V_{erase}\|/2$		**Not meet**
	V/3	read	$V_{read} > 1.06V$	$1.06V > V_{read}/3$		**1.1V – 1.4V**
		write	$V_{write} > 1.63V$	$1.06V > V_{write}/3$		**1.7V – 2.2V**
		erase	$\|V_{erase}\| > 2.5V$	$1.06V > \|V_{erase}\|/3$		**2.5V – 2.55V**
80nm	V/2	read	$V_{read} > 1.37V$	$1.37V > V_{read}/2$		**1.4V – 1.55V**
		write	$V_{write} > 1.63V$	$1.37V > V_{write}/2$		**1.7V – 2.2V**
		erase	$\|V_{erase}\| > 2.5V$	$1.37V > \|V_{erase}\|/2$		**Not meet**
	V/3	read	$V_{read} > 1.37V$	$1.37V > V_{read}/3$		**1.4V – 1.55V**
		write	$V_{write} > 1.63V$	$1.37V > V_{write}/3$		**1.7V – 2.2V**
		erase	$\|V_{erase}\| > 2.5V$	$1.37V > \|V_{erase}\|/3$		**2.5V – 2.6V**

Given the V_{write}=1.63V and V_{erase}=-2.5V, the selector with 40nm oxide length does not meet the requirements for proper write and erase operations in the V/2 scheme, and the erase condition is not satisfied even in V/3 schemes. The 80nm selector requires a very large read voltage (V_{read}=1.4 V), which means that the margin between read and write is very small, and it is not acceptable because of the device to device variability and the noise, however, write and erase requirements are meet for this device. The best design option for the selector is the device with a 60nm VO_2 layer. This device meets all the requirements for the V/3 scheme as specified in Table 5. The margin between read and write operations is about 0.6 V which is acceptable. The operating voltage range of the read, write and erase are specified in Table 5. These results demonstrate that the proposed electro-thermal model can be used effectively to analyze and improve the memory cell during the design phase.

3.3 Transient analysis of the cell access time

The access time of memory cells is an important design parameter. Here we neglect the delay related to the interconnects and only take into account the intrinsic delay for set and reset operations of ReRAM along with the response time for IMT / MIT operations. The turn-on time for the selector determines the read access time, and the write/erase time is the sum of selector turn-on time, and ReRAM write/erase time. Consequently, for the transient analysis, the characteristics of ReRAM and selector are studied separately.

Fig. 9 shows the simulated transient characteristics for "Set" and "Reset" operations of the ReRAM cell [18]. The applied voltage for the "Set"/ "Reset" operations is 2V/-2.5V respectively. The voltage is applied in the form of a pulse with the rise time of 10ns, as illustrated in the insets of Fig. 9. The "Set" operation is high-speed (t_{set}= 1.2ns, we supposed the difference between the time that the applied voltage is reached to 2V and the time when the current is reached to its maximum value as "Set time"). The "Reset" operation requires more time as indicated in Fig. 9(b), the time scale for the reset operation is about 6.6ns (~7ns) (the time difference between application of $V_{applied}$=-2.5V and when the current reaches 50% of its final value is considered as "Reset time").

Several studies reported the transient behavior and IMT/MIT switching for VO_2 structure [28]-[33]. Those studies have shown that transition time in VO_2 depends on the length and cross-section of the active layer [30] and [31]. In addition, in [31], the dependency of the transition time to the voltage amplitude and the input pulse width is discussed. The transient response of the selector is studied based on experimental data because first, the proposed model only captures the DC characteristics, and second, we would like our analysis to be based on experimental evidence. The 20nm selector in [26] has a cross-section of $5\times10^4 nm^2$. A similar structure has been reported in [31], with a length of 100 nm and a cross-section of $3\times10^4 nm^2$, and the switching time of 800ps has been reported for IMT and MIT. Another study suggests a 2ns transition time in VO_2 with 100nm length and $1\times10^4 nm^2$ cross-section area [32]. Consequently, we expect the IMT and MIT switching time for the selector to be in the range of 1 to 2ns. A simple RC model is proposed in [29] to approximate the time constant for the transition. After the transitioning to the metallic phase, the electrical resistance of the selector decreases by several orders, but on the other hand, the dielectric constant of VO_2 increases [35]. For example, the relative permittivity of VO_2 is changed from 36 in the insulator phase to 6×10^4 (real part) in the metallic phase at 100 °C [35]. This indicates that the time constants for IMT and MIT are in the same order [29].

Based on the above discussion, there are two scenarios to estimate transition time for the selector. In the optimistic scenario, the resistance of the selector in the insulating phase increases proportionally with the length of the VO_2 layer. While the dominant capacitance is considered the lateral capacitance between the selector and surrounding area, which decreases by increasing L_{VO2}, and the RC model suggests that the time constant remains unchanged, experimental evidence for this scenario is presented in [34]. In this case, we keep the IMT switching time in a range of 1ns for all selectors from 20nm to 80nm VO_2 lengths. In the pessimistic scenario, the dominant capacitance is the intrinsic layer capacitance between the two electrodes and increases with the VO_2 length. Therefore the RC time constant is proportional with the square of the oxide length ($t_{RC} \propto {L_{VO2}}^2$), experimental evidence for this scenario is reported in [35]. Taking the switching time of 1ns for 20nm selector, we obtain the switching time of 4ns, 9ns, and 16ns for selectors with the length of 40nm, 60nm, and 80nm, respectively based on the pessimistic scenario.,

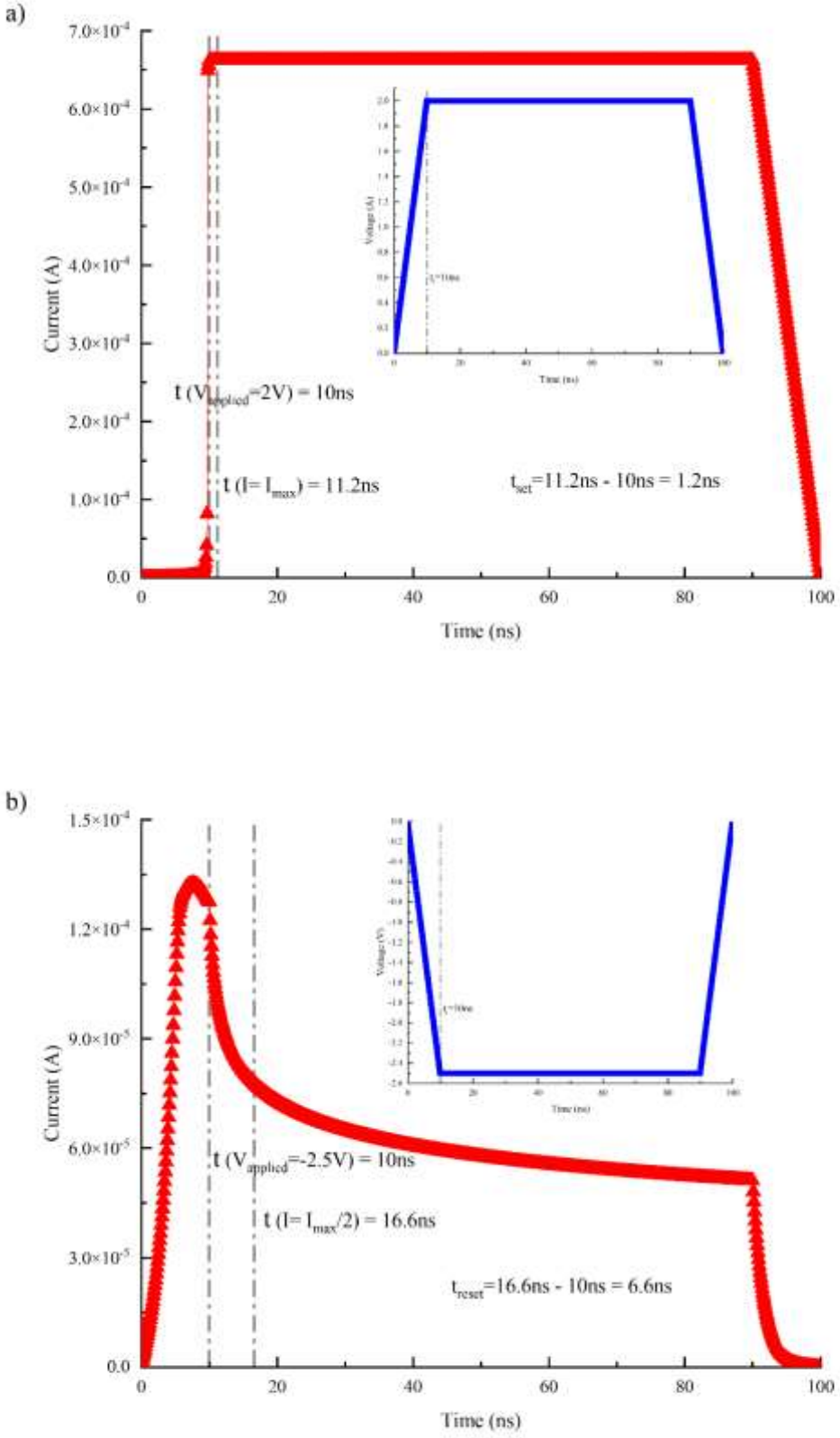

Fig. 9 Transient characteristic of ReRAM device reported in [18] (a) The "Set" operation with the response time of 1.2 ns (inset shows the applied voltage pulse), (b) The "Reset" operation with the time constant of 6.6 ns (inset shows the applied voltage).

Table 6 represents the range of the access times expected for the read, write and erase operations based on the above-mentioned scenarios. This result is especially interesting for the 1S1R cell with 60nm selector length, which meets the design requirements for valid operations, and suggest that the read access time is between 1 to 9ns, write access time is in the range of 2.5 to 10.5ns, and the erase access time is between 8 to 16 ns which are practical values for fast non-volatile memories.

Table 6. Range of expected access times for read, write and erase operations of 1S1R memory cell based on two scenarios

Oxide length	Read access time (ns)	Selector turn OFF (ns)	Erase access time (ns)	Write access time (ns)
20nm	$t_{on} \leq 1$	$t_{off} \leq 1$	$t_{erase} \leq 8$	$t_{write} \leq 2.2$
40nm	$1 \leq t_{on} \leq 4$	$1 \leq t_{off} \leq 4$	$8 \leq t_{erase} \leq 11$	$2.2 \leq t_{write} \leq 5.5$
60nm	$1 \leq t_{on} \leq 9$	$1 \leq t_{off} \leq 9$	$8 \leq t_{erase} \leq 16$	$2.2 \leq t_{write} \leq 10.5$
80nm	$1 \leq t_{on} \leq 16$	$1 \leq t_{off} \leq 16$	$8 \leq t_{erase} \leq 23$	$2.2 \leq t_{write} \leq 17.5$

4- Conclusion

We studied the design of 1S1R memory cells based on the VO_2 Mott selector and TiO_X/HfO_X ReRAM element. The previously developed electro-thermal model for Mott selector and the Stanford PKU model for ReRAM has been used to analyze and study the design requirements of 1S1R cell. Simulation results suggest that the model follows the current-voltage characteristics of experimental devices during read, write and erase operations. We studied the variation of the selector VO_2 length as the design parameter to achieve the design requirements, and simulation results suggest that the selector with the VO_2 layer length of 60nm can meet all design requirements. We further studied the access time for the memory cell based on experimental results and the first-order RC model, and we obtained the worst case access time in the order of 9, 10.5, and 16 ns for read, write, and erase operations, respectively. These results suggest that the proposed IMT model can be used for the design of selector-based non-volatile memory cells.

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