

Design & Development of Laser Etched Porous-Silicon Capacitive Chip for Rapid Sensing of Pesticide Solvents

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Design & Development of Laser Etched Porous-Silicon Capacitive Chip for Rapid Sensing of Pesticide Solvents

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Abstract:

This work presents the development of porous silicon-based electrical sensor for the detection and quantification of organic solvents. The design of silicon chip is modeled as capacitive sensor. Different electrode configurations like coplanar top electrodes, top-bottom, coplanar bottom electrodes were analyzed in order to select optimum chip design for sensing application. The prototype chip was fabricated that used a mechanized pulse fiber laser etching process in order to develop a single-layer silicon structure with uniform porous structures. The fabricated chip was characterized using scanning electron microscopy and it shows an average pore diameter of 55.22 μm and pore depth of 98.9 μm . Organic solvents like ethanol, methanol, acetonitrile were tested and analyzed in order to investigate the performance of the proposed chip. Unlike porous silicon based optical sensors, the proposed sensor exhibited stable results up to 35 days at room temperature. The application of the proposed sensor chip is demonstrated for sensing and for the quantification of Atrazine chemical which is a pesticide solvent which is utilized in farming to control weeds. The sensitivity and the limit of detection was found to be 0.51 nF/ppm and 0.929 ppm respectively. The proposed capacitive-based porous silicon chip is suitable for time-effective and low-cost sensing and detection of organic solvents that are used in food industry.

Keywords: Capacitive Sensing, Chemical Analytes, Field Emission-Scanning Electron Microscopy (FE-SEM), Laser Etching (LE), Porous Structure (PS), Porous Structure Silicon (PSS), Pulsed Fiber Laser (PFL), Sensitivity

1. Introduction

The concept of smart cities and global villages is the buzz word in today's world. This concept cannot become a reality without the use of sensors and sensor-based technologies. These sensors are widely used in aeronautical industries, automotive vehicles, beverages, clinical diagnosis, diamond industries, environmental monitoring system, food, garment industries, oceanic industries, safety and security industries. Therefore, the researchers have continued to research sensor materials on low-cost, easily available material, easily

manufactured, and easily compatible with present (silicon and compound semiconductor) electronics device technologies. In this context, 94% of electronics device technologies are made with silicon [1]. In 1956, Arthur Uhlir Jr. and Ingeborg Uhlir inadvertently found out that the PSS in the bell laboratories and the pioneering research work were done by Leigh Canham [2]. The PSS have large surface to volume ratio, spongy-type skeleton structure, bioactive material, low cost, and easy fabrication. The main advantage of the PSS characteristics changed due to the material inside the pore [2-3]. This makes the PSS more suitable for optical, electrical and thermal sensing application like batteries, drug-delivery system, humidity sensor, solar cell, toxic gas detection, Herbicides and pesticides detection in agriculture, pressure sensor, glucose detection, pathology, and thermal sensing application [3-17]. The optical sensing easily works in hazardous environment, gives fastest output, whereas sensing equipment are costly as well as there is environment interference. Specific training is required for the operator. Electrical sensing is easy to handle as compared to optical sensing mechanism. The fabrication cost is low and it is easily compatible with the present electronics device. No interface is required as is the case with optical sensing.

The fabrication of the PSS was done by etching process [18]. Mainly, the etching process are four types: 1) Electrochemical etching (ECE) process, 2) Inductive Coupled Plasma (ICP) etching process, 3) Reactive Ion etching (RIE) process, and 3) Laser etching (LE) process. In the ECE etching process, the cost of fabrication is low, while in ICP and RIE etching process, the handling of dangerous acids and solvents gets eliminated. Demerits of the top-three etching processes are: 1) It takes more time for fabricating PS in silicon crystal, 2) Harmful chemical and toxic gas used for fabrication, 3) costly instruments are required, and 4) etched rate are low [9]. In a LE process have merits are: speedy, high accuracy, contact less. To fabricate a PS in silicon wafer three types of laser are used. 1) CO₂ ($\lambda=10.64\mu\text{m}$) Laser [19], 2) Nd:YAG ($\lambda=1.064\mu\text{m}$) Laser [20], and 3) PFL ($\lambda=1.064\mu\text{m}$) [3,7]. The main demerit of CO₂ laser wavelength is that it is not absorbed by the silicon wafer. Thus, it requires an additional Pyrex glass which needs to be placed below the silicon wafer in order to promote the wavelength absorption [19]. In Nd:YAG, the cost of instrument is very high. CO₂ and Nd:YAG laser machine require more chiller power and maintenance. Therefore, the cost of instrument is also high [3]. In other paper, we have already discussed that PS can be easily fabricated in silicon wafer using PFL. The pore diameter, depth and porosity can be easily controlled by PFL machine power, speed and pass number [3, 7].

In this work, design, modeling, and prototype development of a porous structured silicon sensor is presented. The sensor chip is inspired by capacitive design in order to perform time-effective and low cost measurements. The design of the porous silicon capacitive chip is investigated using Synopsys Sentaurus TCAD simulation tool. The work aims to demonstrate the potential application of capacitive based silicon sensor chip for sensing application. Thus, different organic solvents were analyzed by comparing the simulation and measured data, and the overall sensor performance was investigated. In Section 2, the simulation model of the porous silicon capacitive chip is presented and the chip configurations are designed and studied. Section 3 discusses the experimental data which includes device fabrication and its characterization results. In Section 4, the sensing principle and measurement technique is explained. The performance of the proposed sensor chip and important sensing results are explained in detail.

2. Design of Porous Si-Chip

The design and simulation of the Porous Silicon (Si) Structure (PSS) for capacitive sensor chip development is performed using Sentaurus Technology Computer-Aided Design (TCAD) tool [21]. The chip design is modeled using a silicon wafer <100> orientation, 10^{18} cm^{-3} concentration doped with boron impurity. The silicon substrate is 1 cm long and $275 \mu\text{m}$ thick with a resistivity between 0.001 to $0.002 \Omega\text{-cm}$. Based on our previous research work and parametric simulation data [19], the pore depth and pore diameter was selected in this Si-chip design. These parameters are illustrated in Table 1. Fig. 1 shows the 2D schematic and perspective view of the PSS modeled in the simulation tool.

Table 1 The material parameters for 2D-TCAD simulation conditions

No.	Parameter	Value
1	Pore Depth	$98.9 \mu\text{m}$
2	Pore Width	$55.22 \mu\text{m}$
3	Pore Separation	$22 \mu\text{m}$

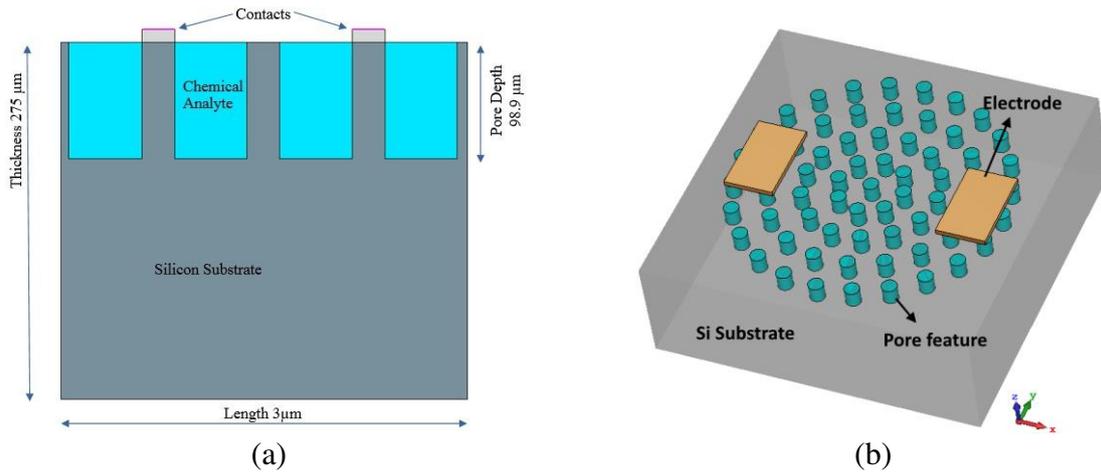
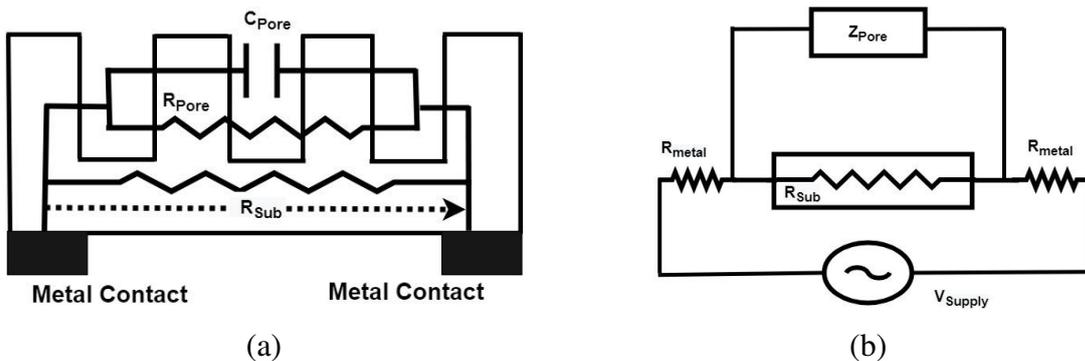


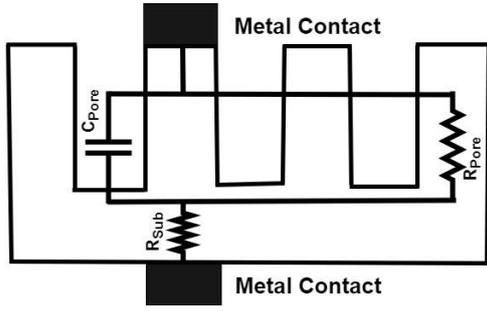
Fig. 1 Cross Section of the implemented of front side contact the PSS capacitive sensor.

In the simulation model, the doping dependency mobility model was selected in order to account for the charge carrier transport phenomenon in the Si-chip. Further, Shockley-Read-Hall physics was used to capture many other changes that occur in charge carriers such as generations and recombination. [1, 21]. The position and configuration of the electrodes are crucial in the capacitive-based PSS device design. The sensitivity and capacitance value depends on the distance between the two plated electrodes and their position with respect to the pores in the silicon wafer. Three different designs of the capacitive PSS are modeled and analyzed for this. These are coplanar bottom electrode (PS1), top-bottom electrode (PS2), and coplanar top electrode (PS3) on the PSS and are shown in Fig. 2 along with their respective equivalent circuit model. In these circuit models, the silicon substrate is modeled with the equivalent resistive and capacitive elements. The impedance is defined in order to represent the pores into the silicon structure.

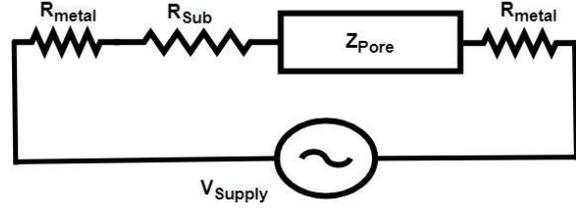
Coplanar Electrode Back Side (PS1)



Top Bottom Electrodes (PS2)

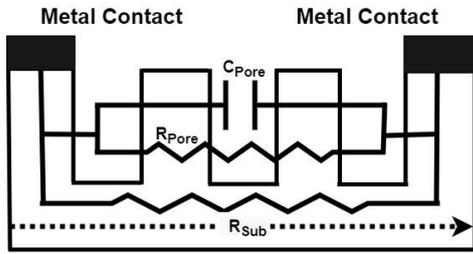


(c)

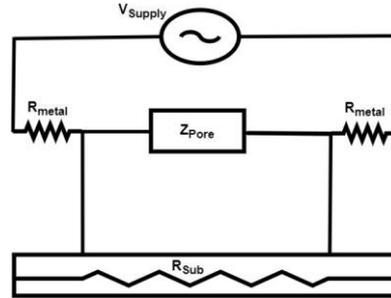


(d)

Coplanar Electrodes Front Side (PS3)



(e)



(f)

Fig. 2 Schematic and equivalent circuit model respectively for (a, b) Coplanar electrode back side of the PSS, (c, d) Top bottom electrode on the PSS, (e, f) Coplanar front side electrode.

It can be observed that the lumped components represented across the sensor structure are different at various junctions. These are R_{metal} , Z_{Pore} , and R_{Sub} , where, R_{metal} is the metal electrode contact resistance, Z_{Pore} represents the impedance across the porous structure junction (i.e. $C_{Pore} || R_{Pore}$), and R_{Sub} is the resistance offered by the silicon substrate. The equivalent impedance of these Si-chip configuration can be calculated as

$$\text{Coplanar back Side Contact} \quad Z_{equivalent} = 2R_{metal} + (R_{Sub} || Z_{Pore}) \quad (1)$$

$$\text{Top-bottom Side Contact} \quad Z_{equivalent} = 2R_{metal} + R_{Sub} + Z_{Pore} \quad (2)$$

$$\text{Coplanar front Side Contact} \quad Z_{equivalent} = 2R_{metal} + (Z_{Pore} || R_{Sub}) \quad (3)$$

Here, the value of C_{Pore} will depend on the dielectric constant of the sensing material inside the pore, whereas, the value of R_{Sub} negligibly affects the overall sensitivity due to high carrier concentration of the silicon wafer. The overall impedance of the porous structure of silicon not

only depends on the dielectric constant of the sensing material, but also the distance between the electrode, area of electrode and resistance of the metal contact. However, the change in capacitive reading from the sensor chip is dominantly contributed by the dielectric constant value inside the pore.

3. Experimental

A. Materials

2” p-type single-sided polished Boron-doped silicon substrate <100>, with a resistivity between 0.01-0.02 Ω -cm, and thickness of 275 μ m was selected. Sulphuric acid (H_2SO_4) 98 wt. % and Hydrogen peroxide (H_2O_2) 38 wt. % reagents were used for cleaning of the Si wafer. Silver (Ag) colloidal conductive paste was purchased from Sigma-Aldrich was used create the electrical contact pads.

B. Fabrication Process of Porous Silicon Chip

The process starts by cleaning the Si- wafer using piranha chemical solution [3-7] in a glass tank. Then silicon substrate was cut into a 1.5 cm² square area. Later, the processed wafer was exposed to pulse fiber laser which created a porous structure in the area of 0.785 cm² as shown in Fig. 3. All the processes were carried out at room temperature. In Table 2, the specifications and operating conditions of the PFL are illustrated for pulsed mode operation.

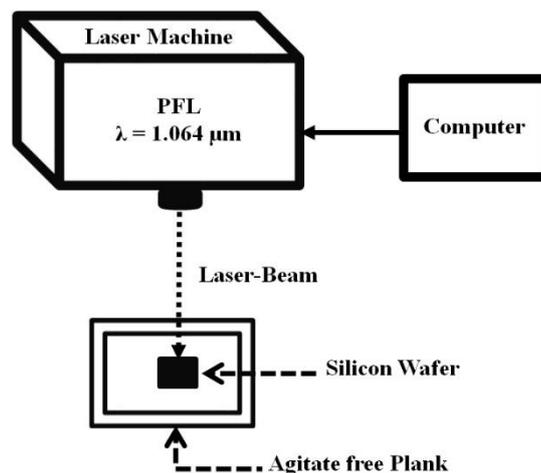


Fig. 3 The schematic representation of the setup for making the PSS using PFL.

Table 2 Specification system and process parameters for etching silicon wafer of the PFL laser

Sr. No.	Parameter	Value
1	Wavelength	1.064 μm
2	Resolution frequency	20,000 Hz
3	Loop Count	1
4	Speed	5 cm/Second
5	Output power	27 watt

Subsequently, the laser etched porous silicon wafer was chemically oxidized by immersion in Hydrogen peroxide (H_2O_2) for 48 hrs. at room temperature. The oxidized porous silicon structure is more suitable [7, 14], wherein, the thin layer of oxide makes the porous structure more hydrophilic and thereby allows the effortless insertion of water-soluble molecules and organic compounds into the pores. The prepared Si-wafer was then rinsed with De-ionized water and was allowed to dry at room temperature. This made the porous silicon capacitive chip ready which can be used for sensing. In Fig. 4, the image of the fabricated Si-wafer and the process steps are presented.

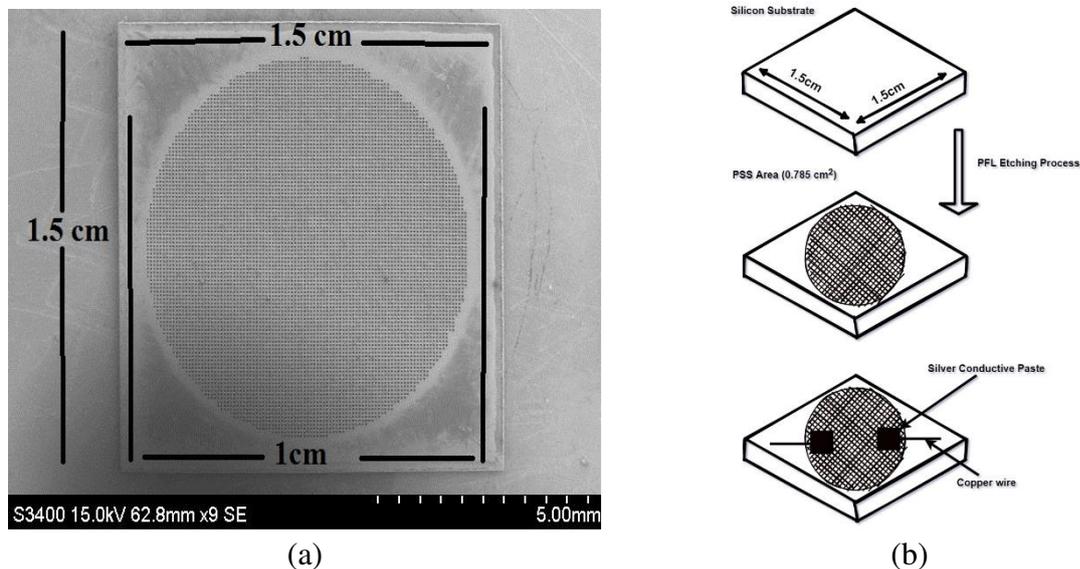


Fig. 4 (a) Processed porous Si-wafer, (b) Schematic of the process-flow



Fig. 5 Si-wafer baking inside muffle furnace for curing colloidal silver paste deposited for electrode pattern and electrical contact.

The deposition of electrode was carried out by using a silver (Ag) paste. For electrical contact, two copper wires were bonded to the Si-wafer in three different electrode configurations as discussed in Section 2. The samples were baked at 100⁰ C for 100 min. in muffle furnace for curing of the conductive silver paste permanently as shown in Fig. 5.

C. Characterization of Porous Si Wafer

Figure 6 shows the Field Emission-Scanning Electron Microscopy (FE-SEM) micrograph images of the top-view and the cross-section view of the fabricated PSS using pulsed fiber laser. The mean pore diameter of 55.22 μm and pore depth of 98.9 μm was observed. It is evident from the FE-SEM image that the etched PFL created uniform pore structures on the silicon wafer area. In our earlier paper [3], the pore size and depth were controlled by applied laser power, pass number and speed.

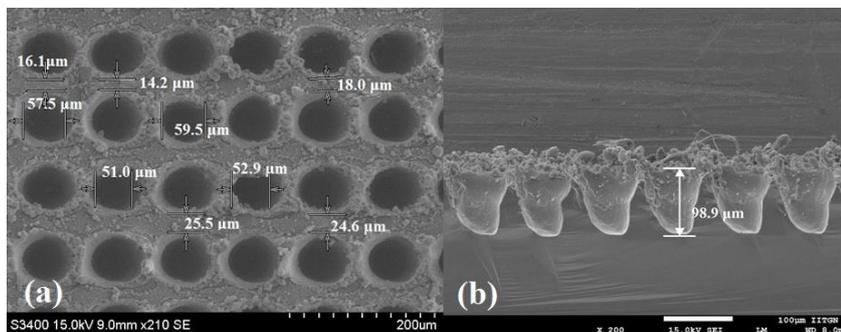


Fig. 6 SEM micrograph analysis of the PSS. (a) top-view (b) cross-sectional view image.

4. Sensing Principle & Measuring Technique

The working principal of the porous silicon capacitive sensor is based on recording the changes in the dielectric constant inside the pores. In the proposed design, 100 % of the target chemical analyte occupies the pores. As a result, ($\epsilon_{\text{chemical analytes}} > \epsilon_{\text{air}}=1.0$) and the PSS effective permittivity changes are then recorded with impedance measurements. In Fig. 7, the schematic for sensing principle of the PSS is depicted.

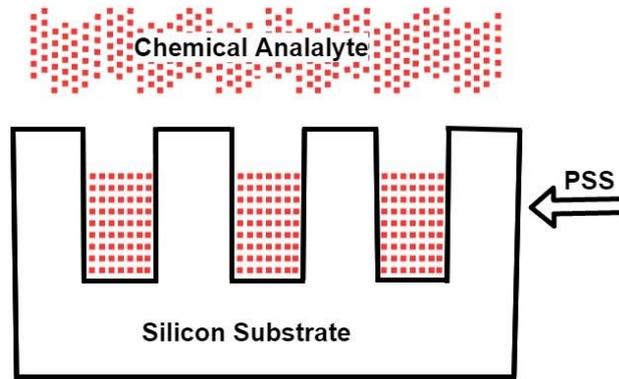


Fig. 7 Schematic showing cross-section of a PSS and its dielectric permittivity changes in the presence of a chemical analyte.

The change in the dielectric constant of the PSS is directly proportional to the concentration of chemical analyte inside the pore. The changes in the capacitance between the silver metal electrodes can be measured by using the following calculation:

$$C = \epsilon \left(\frac{A}{d} \right) \quad (4)$$

where, A - is the area of the PSS, d - is the distance between the electrodes, and ϵ is the relative permittivity of the chemical analyte inside the PSS. As show in Fig. 8, the impedance measurements are recoded using LCR meter for the experimental set-up of PSS capacitive sensor. The test chemical is injected into the pores of the Si-chip using micro-pipette and low loss probes are connected to the metal contacts of the chip. All the measurements were performed at 100 mV AC-signal and operating frequency of 100 kHz [7]. The image of the PSS capacitive chip measurement setup is shown in Fig. 8

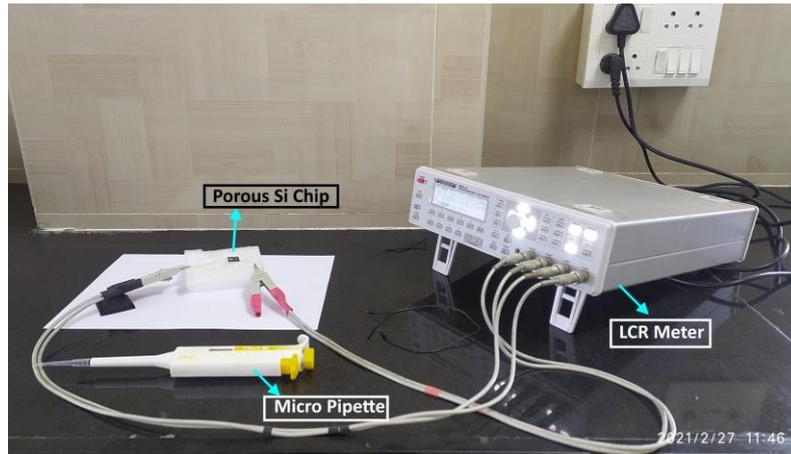


Fig. 8 Image of the measurement setup

5. Experimentation Using Different Chemical Analytes

The fabricated PSS capacitive sensor was first tested on some of the widely used and standard organic solvents such as acetone, ethanol, and methanol. The Si-chip was loaded with 10 μL volume of the sample and it provides enough time before the sample gets fully vaporized. All measurements were recorded by pre-cleaning the PSS capacitive sensor using de-ionized water, followed by the process of drying through nitrogen gas. The PS1, PS2, and PS3 chips were tested with organic solvents and their performance was compared in order to evaluate and select optimum chip configuration for measuring pesticide solvent chemical named ‘Atrazine’. The experimental values of PSS capacitive sensor with air-filled pores for PS1, PS2, and PS3 are 0.022 $\text{fF}/\mu\text{m}^2$, 0.018 $\text{fF}/\mu\text{m}^2$, and 0.228 $\text{fF}/\mu\text{m}^2$ respectively. These values are in close match with the TCAD simulated values that are 0.04 $\text{fF}/\mu\text{m}^2$, 0.03 $\text{fF}/\mu\text{m}^2$, and 0.32 $\text{fF}/\mu\text{m}^2$ respectively. The simulation and measured value of the capacitance per area ($\text{fF}/\mu\text{m}^2$) for different test samples is projected in Fig. 9. It is evident that PS1, PS2 and PS3 chips offer linear performance, wherein the value of capacitance per area increases when dielectric constant inside the pores of the Si-chip increases. It is important for any PSS chip to exhibit higher capacitance, so that other stray capacitance or unwanted dielectric losses don’t mask the dynamic range of the chip.

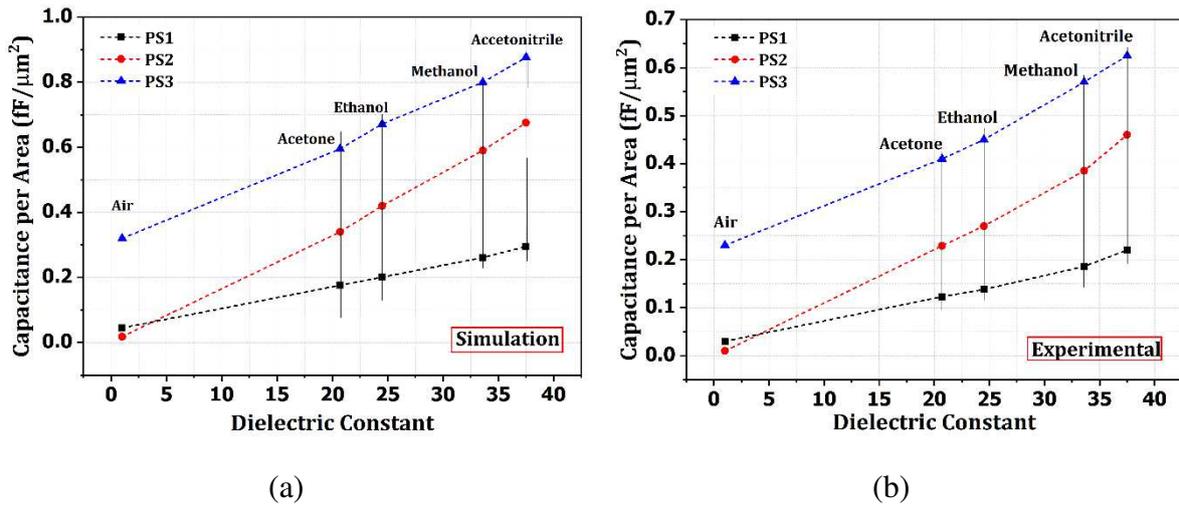


Fig. 9 Comparison of simulated and measured capacitances of the three different PSS capacitive sensor for various chemical analytes with different dielectric constant value.

The measurement data of tested organic solvents are illustrated in Table 3. From the simulation and measurement values, it is confirmed that the value of capacitance per area is for PS3 i.e. $PS2 > PS2 > PS1$. To further understand this, the two coplanar electrodes on the front side of the PS3 configuration provides air fringing field and field linkages coupled through the dielectric of porous silicon. When the analyte is loaded, it directly comes into the contact of these fringing field components. Therefore, higher value and change is observed in the capacitance.

Table 3 Details of simulated and measured normalized capacitance obtained for three different chemical analytes using the proposed PSS capacitive sensor.

Chemical Solvent and their Dielectric constant	Back Side Contact-PS1		Front-Back Side Contact-PS2		Front Side Contact-PS3	
	Normalized Simulated (C/Area) (fF/μm²).	Normalized Experimental (C/Area) (fF/μm²).	Normalized Simulated (C/Area) (fF/μm²).	Normalized Experimental (C/Area) (fF/μm²).	Normalized Simulated (C/Area) (fF/μm²).	Normalized Experimental (C/Area) (fF/μm²).
Air ($\epsilon=1.00$)	0.04	0.03	0.018	0.01	0.32	0.23
Acetone ($\epsilon=20.7$)	0.176	0.123	0.331	0.229	0.595	0.41
Ethanol ($\epsilon=24.5$)	0.201	0.138	0.42	0.274	0.671	0.46
Methanol ($\epsilon=32.7$)	0.261	0.186	0.59	0.385	0.8	0.57
Acetonitrile ($\epsilon=37.5$)	0.295	0.22	0.675	0.46	0.876	0.625

On the other hand, PS1 has coplanar electrodes on the back side of the porous silicon chip and the fringing field linkages don't couple well into the pores. Moreover, when the sample is loaded, it first comes into the contact of pores and provides no direct contact with the electrode. As a result, it leads to lower value of capacitance. A minor deviation can be seen in the simulated and experimental result. This difference is primarily attributed to difference in the pore features of the simulated and fabricated Si chip.

Also, the possibilities for changes in the capacitive response is investigated by using a simplified TCAD model of the proposed PSS chips. As shown in Fig. 10, the pores were filled with analyte and electric field distribution is analyzed. The front side coplanar electrode (PS3) results into the highest electric field value of $1.99 \times 10^5 \text{ V.cm}^{-1}$.

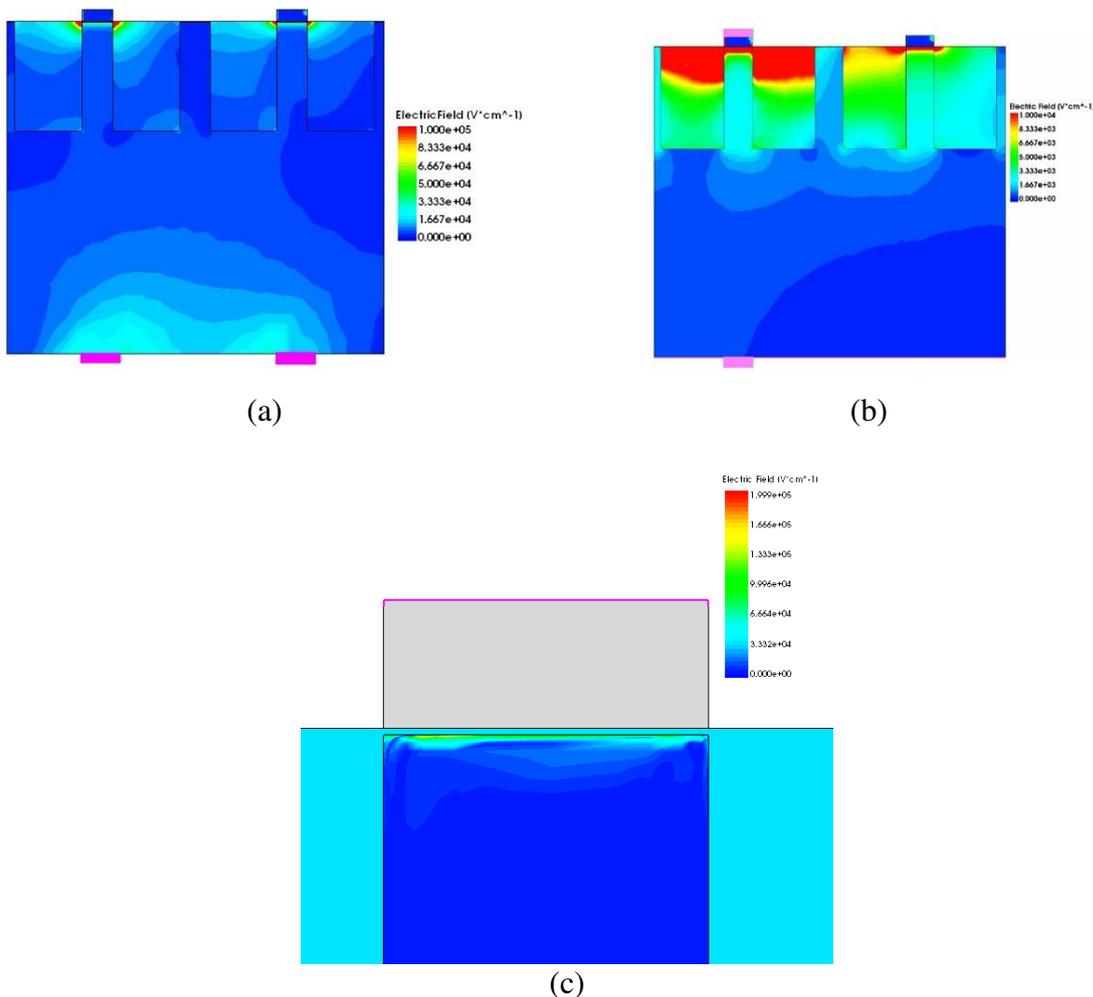


Fig. 10 Electric Field profile for (a) PS1, (b) PS2), (c) PS3 chip configuration

The time-dependent drift in the measurement data of the sensor is another crucial performance parameter which needs to be analyzed. The main reason of the drift is environmental-aging effects that leads to the growth of natural oxide in an uncontrolled manner. As a result, the capacitive response of the chip begins to deviate from the standard mean value. The response of all the three PSS capacitive sensors was tested for the drift analysis and that too for 35 days at room temperature with methanol analyte.

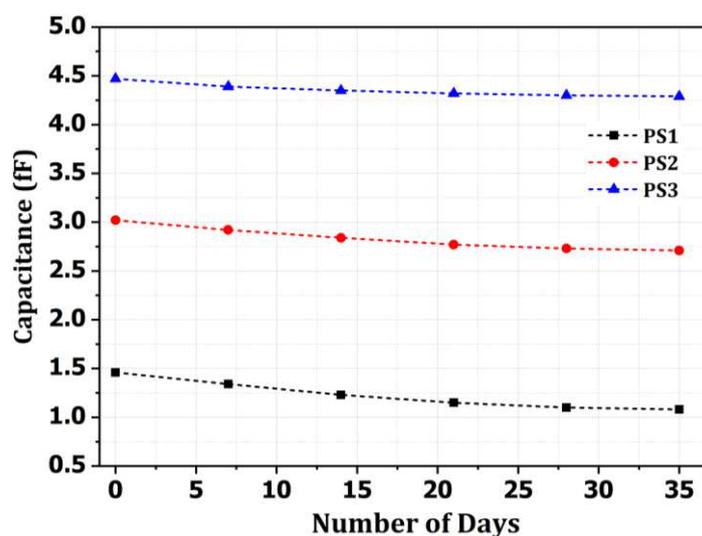


Fig. 11 Drift in Sensor response with time for methanol test sample.

As seen in Fig. 11, the response of the sensor for PS3 is more stable in comparison to PS2 and PS1 chip configuration. In PS1, no electrode pad is deposited on the pore side. Whereas, PS2 has only one electrode place above the front side of the pores. Thus, in PS1 and PS2, greater number of pores are available in comparison to the PS3, and it promotes higher natural growth of oxide. The presence of oxide in PS1 will be higher and it will lead to more drift in the measurements over a period of time. Based on these results, PS3 sensor chip was selected for further application.

6. Application in Sensing & Quantification of Synthetic Herbicide – Atrazine

Pesticides belong to the class of analytes that are frequently tested by sensors due to their growing presence in water or agricultural products as contaminants. Pesticides have been used on various crops worldwide over the past 50 years. Among all the available pesticides, Atrazine is the most widely used herbicide in the entire world to control wide-leaf crops and the grassy weeds.



Fig. 12 Chemical structure of the Atrazine

Atrazine $C_8H_{14}ClN_5$ having an IUPAC name of 2-chloro-4-methylamino-6-isopropylamine-1, 3, 5-triazine, and molecular weight of about 215.68 gmol^{-1} and its chemical structure is represented in Fig. 12. It has properties like being white, stable, colourless, and non-volatile which makes it commonly used herbicides because of its high relative mobility in the soil. It is a putative endocrine disruptor and even at minimal concentrations (parts-per-billion concentration) can cause severe health hazards. Long-term exposure at low levels to humans can cause sub-acute and potentially dangerous bodily functions. A lower concentration of atrazine powder is taken and it is dissolved in the tap water for measuring the atrazine levels in the water. Then a small amount of methanol is added for better solubility and for the preparation of different concentrations of the Atrazine ranging from 1 ppm to 30 ppm. The test sample was loaded into the pores of the Si-chip and capacitance was measured for each of the concentration. Individual measurements were followed by chip-cleaning using de-ionized water and the process of drying through nitrogen gas.

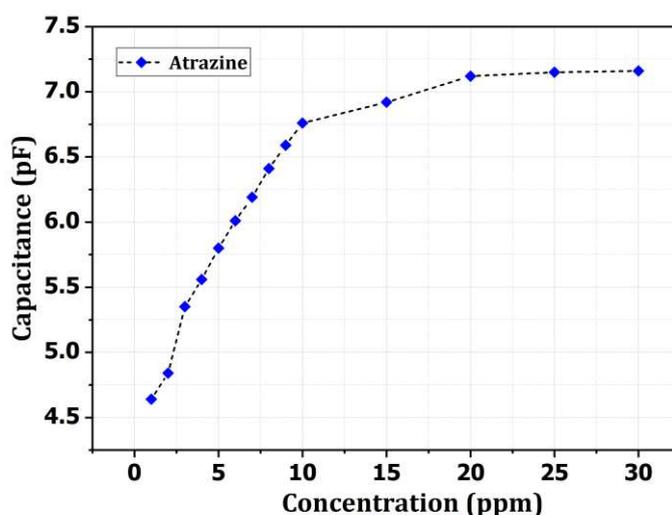


Fig. 13 Plot of capacitance measured for different concentration of Atrazine

Table 4 Capacitance measured from proposed PSS capacitive sensor for different concentration of Atrazine

Volume Concentration (ppm)	Capacitance (nF)	ΔC (nF)
1	4.64	--
2	4.84	0.2
3	5.35	0.51
4	5.56	0.21
5	5.8	0.24
6	6.01	0.21
7	6.19	0.18
8	6.41	0.22
9	6.59	0.18
10	6.76	0.17
15	6.92	0.16
20	7.12	0.2
25	7.15	0.03
30	7.16	0.01

The plot of capacitance for different concentration of the atrazine sample is shown in Fig. 13. In Table 4, all the measured data has been illustrated. It is found that increase in the concentration of atrazine upto 10 ppm causes linearly increases in the capacitance. However, the sensor capacitance tends to saturate for higher concentration of atrazine. This is due to the solubility limit of atrazine in methanol.

The sensitivity of the proposed PSS capacitive sensor chip was calculated using Eq. (5) to determine the performance and its potential usage for real-world sensing application. The sensitivity (S) is calculated as

$$S = \frac{\Delta C}{\Delta \text{Concentration}} \text{ nF/ppm} \quad (5)$$

Where, S is sensitivity, ΔC denotes the change in the capacitance value, and $\Delta \text{Concentrations}$ indicates change in the concentration level of the Atrazine solution. The calculated sensitivity value of the proposed sensor chip is 0.51 nF/ppm. Another important performance parameter is the Limit of Detection (LOD) which was calculated as [7, 23-24],

$$LOD = K \times \left(\frac{SD}{S} \right) \quad (6)$$

Where, SD is the standard deviation, S denotes the measured sensitivity, and $K = 3.3$ is a constant selected with reference to 95% confidence level [7, 23]. The calculated LOD is 0.929. Even though the LOD of the propose sensor is on a bit higher end in comparison to the other reported mentioned in Table 5 that are based on nanotechnology and optical sensing, the sensor shows potential capability for improved sensitivity, linear performance, time effective measurements and low cost design solution.

Table 5 LOD performance comparison of the proposed PSS capacitive sensor with other reported work

Reference Number, Year	Method of Detection	LOD (ppm)
[25], 2005	Optical micro-sensors based on multi-layered Porous Silicon technology	0.17
[26], 2018	Nano Porous Silicon based multi-layered Photonic Sensors	0.0000014
Proposed work	Single-layered Porous Silicon based Capacitive Sensors	0.929

7. Conclusion

This paper shows prototyping of a laser etched porous silicon structure for the development of a capacitive sensor device. The realized porous silicon chip was tested with various standard organic solvents and it demonstrated the linear performance of the sensor. The proposed sensor chip was found stable up to 35 days which shows its improved usage in comparison to the chemically etched porous silicon chips. The fabricated porous silicon chip with uniform pore features allowed sensing for organic solvents, and it has been demonstrated by using Atrazine pesticide as an analyte. The sensitivity of the sensor chip is 0.51 nF/ppm, and it shows that very low concentration of such pesticides can be easily detected from water near the soil. The porous

silicon capacitive sensor chip can be used as a potential candidate for low-cost sensing as well as for the quantification and detection of chemicals in industrial applications.

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