Study And Investigation of Silicon Extended Source Vertical Double Gate Tunnel Transistor For Analog/RF Performance

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Study and Investigation of Silicon Extended Source Vertical Double Gate Tunnel Transistor for Analog/RF Performance

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Abstract In this paper, a Silicon Double Gate tunnel field-effect transistor with Extended Source (ESVDG-TFET) is disclosed while addressing the need for dc/switching and analog/RF applications using Silvaco-Atlas simulator which is used to examine and explore the performance of the proposed device. The mechanics of band-to-band tunnelling and accompanying carrier injection are used to illustrate the operation of the proposed silicon ESVDG-TFET device. The gate is designed to overlap with extended source region along with N+ pockets and channel in order to facilitate both the lateral and vertical tunnelling . The silicon ESVDG-TFET provide lower subthreshold swing of 10.1 mV/decade that allow higher ratio of $I_{ON}/I_{OFF} \simeq 10^{13}$ for optimized device structural parameters with threshold voltage of 0.35 V. Moreover, peak transconductance of 800 uS/ um, cutoff frequency of 82 GHz, gain bandwidth product of 16.8 GHz and transit time of 1p sec is obtained by proposed device.

Keywords Band-to-Band Tunneling (BTBT) · Subthreshold Swing (SS) · Tunnel Field-Effect Transistor (TFET) · Analog/RF performance · Cutoff Frequency · Energy Band

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1 Introduction

Tunnel field-effect transistors (TFETs) have been considered as an alternatives to traditional metal oxide semiconductor FETs because of the beauty of this novel transistor as it deliver steeper switching characteristics (SS is not limted to 60 mV/dec) and has a wide scope for low power SOC design (allow voltage scaling). The physics of TFET is based on BTBT imparting immunity against various short channel effect.[3] Although the ON-state current of the TFETs is low due to the lack of BTBT (band-to-band tunnelling) probability at the source/channel junction. The probability of tunnelling is proportional to the energy band, charge carrier effective mass, gate oxide thickness and tunnelling barrier width[1][2]. Many studies have been published in recent years to improve the TFET's performance[6] -[18] Although the majority of researchers has focused on TFETs for low-power switching applications. Many efforts are being made around the world to improve ION, including the use of: 1) a low-bandgap material in the tunneling region[5]; 2) a double-gate architecture[6]; 3)Pocket doped double gate structure[7]; 4) a high-k gate dielectric[6]; 5) hetero gate dielectric[1][8]. Low subthreshold swing (SS), low threshold voltage (Vt) and a high ON-state current (I_{ON}) to OFF-state current (I_{OFF}) ratio are all desirable performance parameters for low-power switching and analog/RF circuits including high transconductance (g_m) and high cutoff frequency(f_T)

Various efforts are made by researchers as reported in the literature to enhance the dc and analog/RF performance parameters. Wei Li et al.[9] the author proposed HTG-TFET (Heterojunction TFET with a T-Shaped Gate) having following performance index I_{on} as 7.02A/m and SSavg = 44.64 mV/dec. The author addressed the problem of miller capacitance with the help of Si/SiGe hetero-junction with different doping composition and gate overlap structures. B. S. Reniwal et al.[10] impact of device engineering on DGT-

FET with gate underlap and different dielectric spacer material concept used to enhance dc and ac characteristics for SOC application. The author has reported g_m as 4.4 uS and f_T as 5 GHz and GBP of 1.8 GHz for UL-LKHG DG-TFET. T. Joshi et al.[11] presented a Extended source DG-TFET in which entire source in placed in the channel only by varying S_W an improvement in DC/RF parameter is reported. SSavg of 12.24 mV/dec, $I_{ON}/\ I_{OFF}$ ratio of $2.5 * 10^{12}$, g_m as 238 uS/um, f_T of 37.7 GHz and GBP as 3.4 GHz. Jang Hyum et al.[12] reported VS-TFET with vertical channel sandwiched by doped Si facilitating perpendicular tunnelling and gradual doping profile to address I_{AMB}, $I_{ON}/\ I_{OFF}$ as 10^4 and SS-min of 17 mV/dec.In comparison to the traditional counterpart, X.Zhao et al.[13] informed an L-shaped TFET to improve the BTBT rate and I_{ON}. LDD combined with HGD structure to reduce ambipolarity. Shupang CHen. et al.[14] suggested a silicon T-shape TFET (TG-TFET) with an SS of 24.4 mV/decade and an $I_{ON}/\ I_{OFF}$ of $6.7 * 10^{10}$. The TG-TFET has a g_m of 232 uS/m and a f_T of 11.9 GHz, as investigated by the authors.In various other reported literature, researchers proposed advantage of vertical TFET over planer structure and its fabrication ease[15]. P. Wang et al.[16] improve average SS by suppressing low electric field with epitaxial tunnel layer in TFET structure. Exhaustive use of Si/Ge epitaxial layer in the channel have been reported. [20]

In this article, extended p+ source is made to overlap with gate electrode and 2nm silicon epitaxial layer to facilitate both vertical and lateral tunnelling to improve dc and analog/RF performance. The ESVDG-TFET improves I_{ON} and as a result, I_{ON}/I_{OFF}, SS, and V_t significantly improve. Furthermore, double gates and scaled device dimensions allow better gate control of drain current, resulting in a higher g_m , which improves the device's high-frequency characteristics. 2-D commercially available TCAD tool, Silvaco ATLAS device simulator is used to examine and explore the performance of the proposed device. The proposed Silicon ESVDG-TFET achieves an I_{ON}/I_{OFF} of 1×10^{13} with an SS of 10.1 mV/decade, according to simulation results. The device has a peak g_m of 800 uS/m, f_T of 82 GHz and Gain bandwidth product of 16.8 GHz respectively.

2 Device structure, Fabrication steps and Simulation

The cross sectional schematic of Silicon ESVDG-TFET is shown in fig Fig. 1 and the parameters associated with proposed device are listed in the Table I as shown. The silicon ESVDG-TFET is a symmetrical typed double gate structure made up of a silicon substrate with a thickness of 10 nm (T_{Si}). The gate electrode is made to overlap with p+ source $10^{20}\ cm^{-3}$ of doping concentration and 2nm silicon epitaxial layer (T_{epi}) of $10^{17}\ cm^{-3}$ doping concentration below gate contact. The n+ pocket and n-channel region is doped with

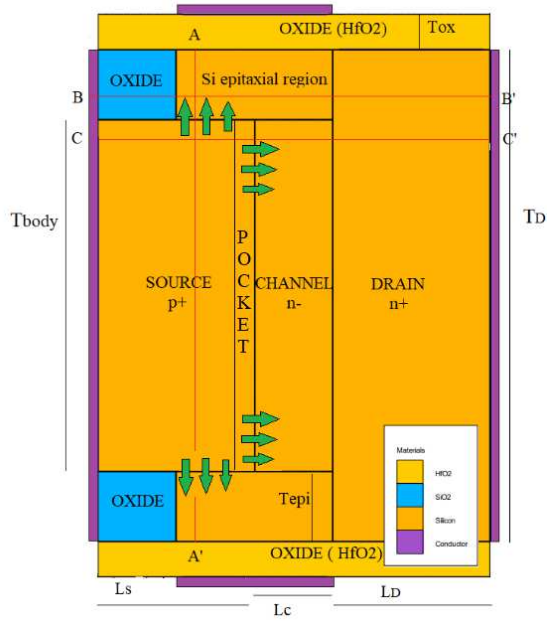

Fig. 1 Schematic of the device structure (not to be scaled).

concentration of $10^{19}\ cm^{-3}$ and $10^{17}\ cm^{-3}$ respectively . T_{body} and L_s represent the height and length of the source, respectively. Similarly L_c for channel length which is choosen to be 20nm. The doping concentration in the n+ drain region is $10^{19}\ cm^{-3}$. A stacked gate oxide near source region (2-nm SiO2 and 1-nm HfO2) and as one reaches near the 2nm epitaxial layer oxide thickness (T_{ox}) of HfO2 reduces to 1nm upto drain end with a gate work function of 4.2 eV. The proposed device has a part of source p+ extended into channel under the gate which is differ from recently reported ESDG TFET in this entire source is grown under channel.

The proposed silicon ESVDG-TFET structure can be fabricated in the same way as reported[19][23]. In Fig. 2 the proposed ESVDG TFET's fabrication steps are depicted. The source region is defined using a photoresist mask, and then P+ implantation is performed followed by oxidation which is used to grow 2-nm SiO2. After that, rotate the structure at right angle epitaxial growth of 2 nm silicon with doping type and concentration similar to the intrinsic channel is carried out[5]. In similar fashion N+ is implanted to form drain region with defined doping concentration. In the succeeding step, oxidation is done to form gate oxide layer of 1-nm HfO2 then metallization and patterning are carried out to form the front and back gate of the ESVDG-TFET then source and drain contacts.

In order to study various physical phenomena and its effects in a TFET, relevant models are included in the ATLAS device simulator [27]. To study the recombination phenomenon Shockley–Read–Hall (SRH) with concentration depend life-time model is included. The non-local BTBT tunneling model is taken into account to analyze quantum tun-

Table 1 Device parameter description for simulation

Parameter	Symbol	VSiDMG[19]	ESVDG-TFET
Source doping ($/cm^3$)	N_A	10^{20}	10^{20}
Drain doping ($/cm^3$)	N_D	10^{18}	10^{19}
Pocket doping($/cm^3$)	N_P	-	$2*10^{19}$
Channel doping($/cm^3$))	N_C	10^{16}	10^{17}
Channel length (nm)	L_C	20	20
Source length (nm)	L_S	80	22
Gate length (nm)	L_G	30	30
Drain length (nm)	L_D	50	15
Gate oxide thickness (nm)	T_{OX}	2	1
Pocket thickness(nm)	T_P	-	3
Silicon thickness (nm)	T_{Si}/T_{body}	10	10
Epi-layer thickness (nm)	T_{epi}	2	2
Gate work function (eV)	ϕ_m	4.0 - 4.5	4.2
Drain bias (V)	V_{DS}	1.5	1.5

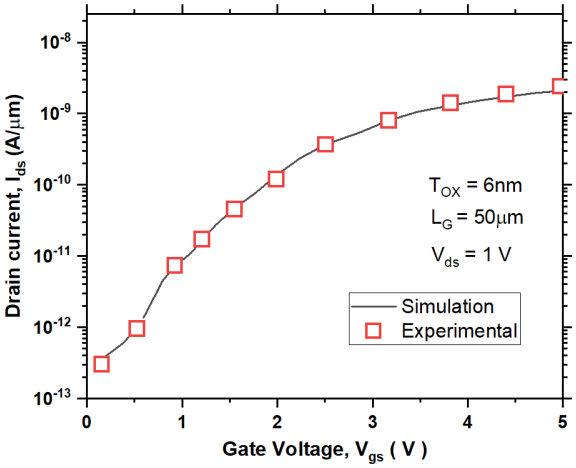

Fig. 3 Simulation model calibration using prefabricated TFET[28]

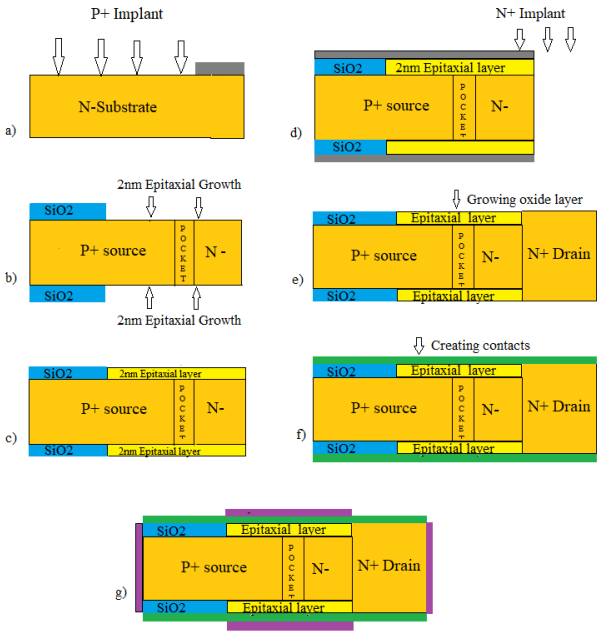

Fig. 2 Fabrication steps of proposed device structure

neling in the device. The traps and dislocations at the interface of epitaxial layer are studied using the non-local trap-assisted tunneling model, which is based on the Wentzel Kramer Brillouin (WKB) transmission coefficient [1],[2]. To account for the effect of heavy doping, a band-gap narrowing model and Fermi–Dirac statistics were used. The simulation setup's accuracy is validated in the simulator by implementing a fabricated TFET [28]. We exhibit a comparison of simulated data and measured value transfer properties of a manufactured TFET. The experimental results are substantially identical to the simulated data plot as shown in Fig. 3.

3 Results and Discussion

3.1 DC Analysis

Using energy band diagrams, BTBT tunnelling and electric field distribution enhancement in on current can be better described with the help of Transfer characteristics within the framework.In non-local models, the most widely used method to calculate tunnelling probability is the WKB approximation based on charge carrier transmission probability (TWKB) function of tunneling barrier width is formulated as[1]

$$T_{WKB} \propto \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(E_g+\Delta\Phi)}\sqrt{\frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}}t_{\mathrm{ox}}t_{\mathrm{Si}}}\right) \quad (1)$$

where E_g is the bandgap, m^* is the effective carrier mass, ε_{ox}, t_{ox} are dielectric constants and oxide thickness. Also, ε_{Si} and t_{Si} are the silicon dielectric constants and body thickness and $\Delta\phi$ is the energy range over which tunneling can take place.

In Fig. 4 the device's transfer characteristics is presented for varying Vgs at Vds = 1.0 V, as indicated in plot. When energy band are not aligned at Vgs = 0 V a weak off current flows of order $1*10^{-16}$. The drain current found to be independent of gate voltage in OFF-state. This region is marked by generation and recombination current (temperature dependent) dominates I_{OFF}. In subthreshold region that is near threshold voltage at Vgs = Vth = 0.35 (corresponding I_d = 10^{-7}) as determined by constant current method[1] and reduction in SS. Further increase in Vgs I_d is primarily governed by BTBT hence becomes less temperature-sensitive. I_{on} of order 10^{-3} with I_{on} / I_{off} ratio 10^{13} in case of proposed silicon ESVDG TFET which is significantly higher when compared to simulated reference device vertical Si/Ge dual material gate TFET I_{on} / I_{off} ratio $4.8*10^{12}$ and I_{on} / I_{off} ratio $4.8*10^{11}$.

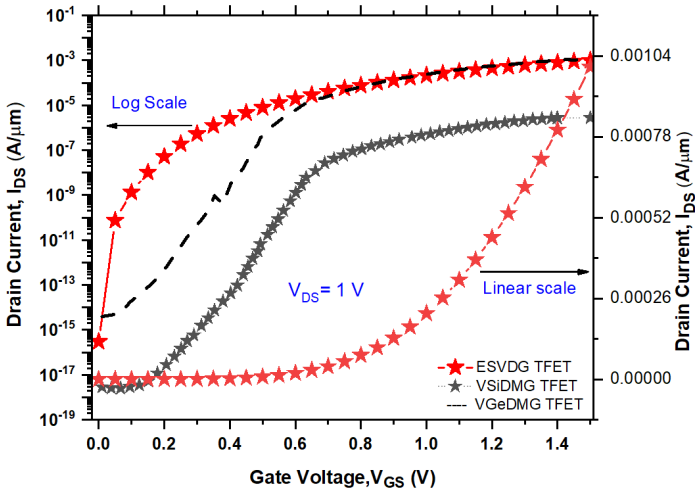

Fig. 4 Transfer characteristics curve for proposed Silicon ESVDG TFET at Vds = 1V

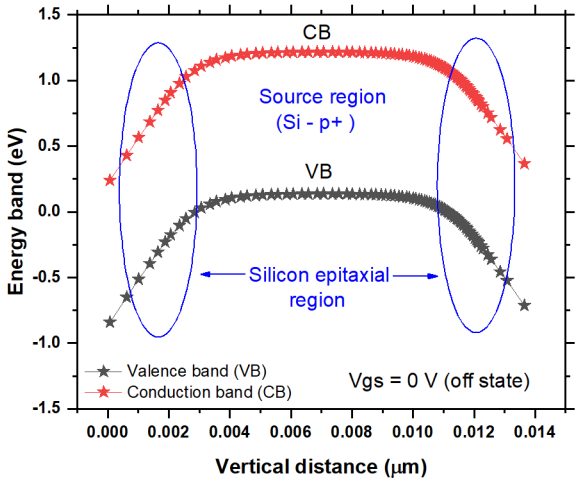

Fig. 5 Energy band plot along the cutline A-A' in OFF state at Vgs = 0 V and Vds = 1 V)

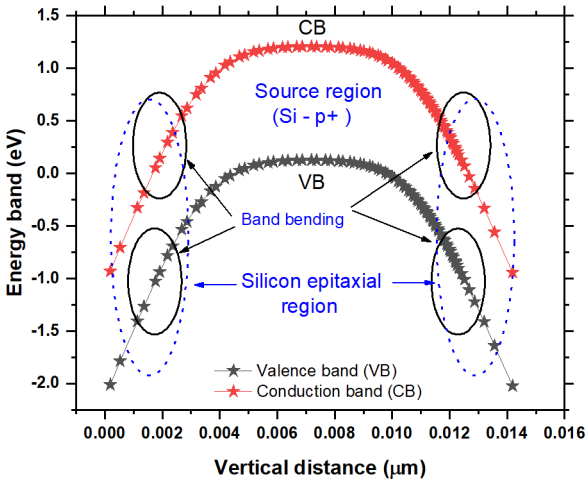

Fig. 6 Energy band plot plot along the cutline A-A' in ON state at Vgs = 1 V and Vds = 1 V

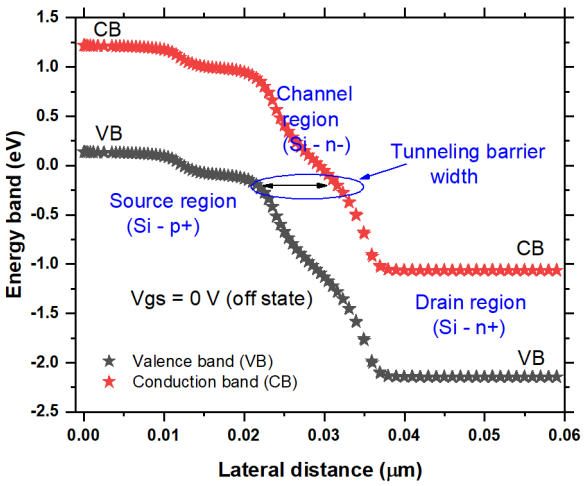

Fig. 7 Energy band plot along the cutline C-C' in OFF state at Vgs = 0 V and Vds = 1 V)

Tunnelling enhances at source-channel junction and source-si epitaxial layer as it behave as channel for electrons tunneling vertically and then drifted toward the drain under the influence of drain voltage. In order to fully comprehend the working operation the energy band diagrams of proposed device along the cut-line AA' is displayed in Fig. 5. It is clear from figure the source region's valence band is unable to align with conduction band of Si-epitaxial layer when Vgs = 0 V , so the off-state current is very low as device is in OFF-state. Now as the gate to source voltage is increased band bending along band lowering take place and at a certain gate voltage the source region's valence band gets align with conduction band of Si-epitaxial layer. This leads to steep increases in the current. In addition increase in the gate bias leads to reduction in tunneling barrier length and further increase in the current as illustrated in Fig. 6. giving the confirmation of line tunneling.

Further, Fig. 7 and Fig. 8 illustrates the energy band diagram along cut-line CC' at OFF-state (Vds = 1 V, Vgs = 0 V) and at On-state (Vds = 1 V, Vgs = 1 V). On increasing the gate potential energy barrier height and tunnelling width λ decreases giving rise to point to point tunnelling. Similarly, Fig. 9 shows the energy band in ON and OFF-state when a lateral cut-line along BB' is made. It is observed a large band gap toward the left most end due to presence of SiO2 oxide layer. A narrow energy band of Si-epitaxial layer and drain region is present owning to silicon material. Increase in gate bias voltage leads to band lowering providing a channel for tunnelled electron.

Fig. 10 shows the variation in carrier concentration (electron and hole) along the cut-line C-C' as marked in the device near off state(Vgs = 0 V and Vds = 0.1 V) and in on state (Vgs = Vds = 1V). It can be seen that large carrier concentration exist at the source-pocket-channel interface. Fig. 11 is plot of I_{ON} and I_{OFF} with source length.

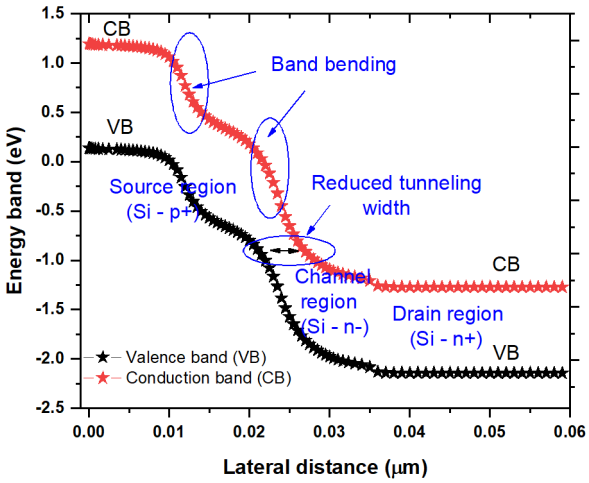

Fig. 8 Energy band plot along the cutline C-C' in ON state at Vgs = 1 V and Vds = 1 V)

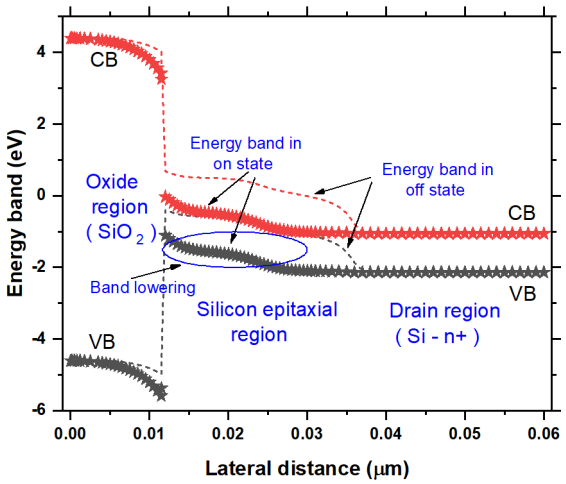

Fig. 9 Energy band plot along the cutline B-B' in OFF and ON state at varying Vgs and Vds = 1 V)

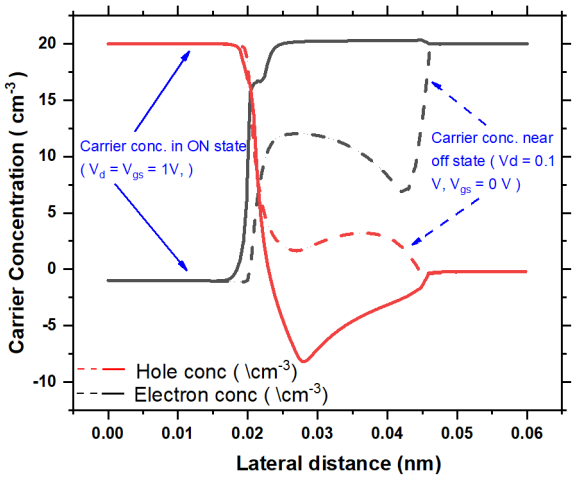

Fig. 10 Variation in carrier concentration along cutline C-C' in OFF and ON state.

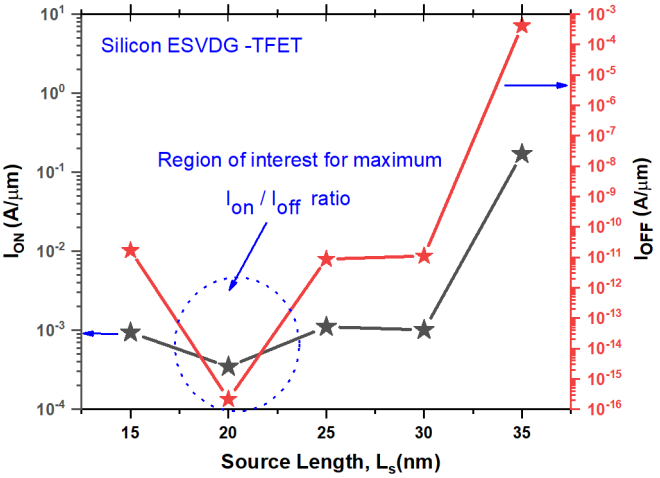

Fig. 11 Variation of Ion and Ioff current with source length.

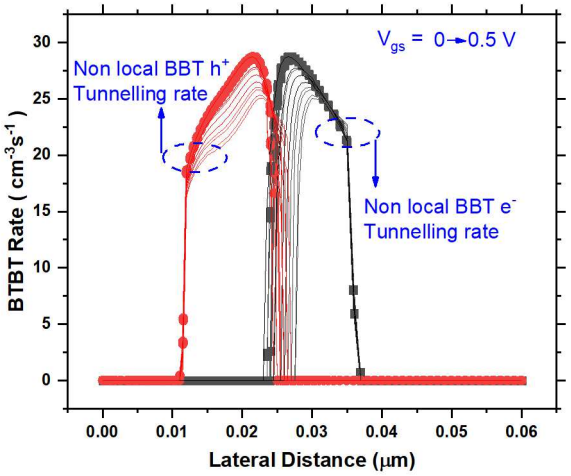

Fig. 12 Non-local BTBT tunnelling rate for varying Vgs (0 to 0.5 V)

It is seen that increase in the source length results in more tunnelling area availability, thus increase I_{ds}, however at the same time degradation in off current also follow thus a need for choosing optimum L_S is necessary which is 22nm for silicon ESVDG TFET at which max I_{ON} / I_{OFF} is obtained while keeping L_G = 20 nm. Fig. 12 illustrate non-local band to band tunnelling for hole and electron for V_{gs} ranging from 0V to 0.5 V for better understanding of proposed Silicon ESVDG TFET.

Fig. 13 shows the electric filed variation along the cutline CC' as marked in the device. As it can be seen the peak electric field exist at the source-pocket-channel interface. It is also worth noting that the peak of the electric field of 5.15 MV/cm at pocket doping concentration of 10^{18} cm^{-3} which is higher than the peak 4.6 MV/cm in the absence of pocket that to say channel doping concentration of 10^{17} cm^{-3}. Lateral tunnelling width λ which decrease with gate bias can be seen in energy band diagram.

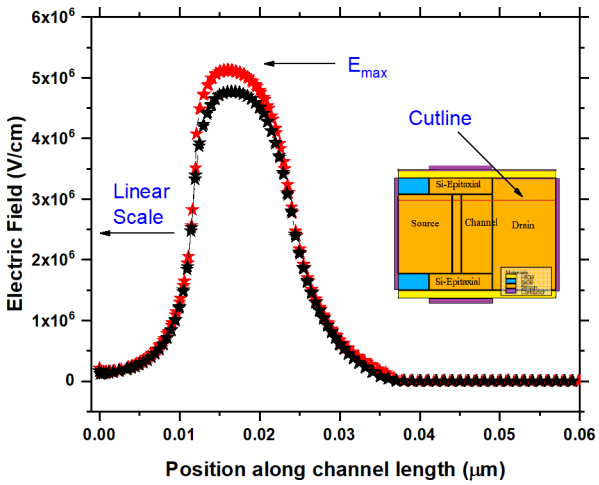

Fig. 13 Electric field plot along the cutline C-C' at Vgs = 1.5 V and Vds = 1 V)

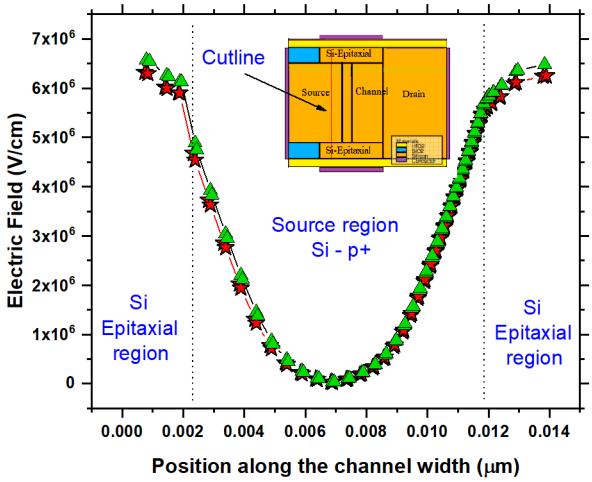

Fig. 14 Electric field plot along the cutline A-A' at Vgs = 1.5 V and Vds = 1 V)

Fig. 14 depicts electric field variation along the cut-line AA' as marked in the proposed device. The maximum electric field value lies at the interface of source - silicon epitaxial of value 6.5 MV/cm for doping concentration of 10^{17} cm^{-3} which is higher than 6.3 MV/cm for doping concentration of 10^{16} cm^{-3}. The increase in electric field with increase in doping concentration values establish direct dependency of electric field on doping thus helps in increasing the value of current within the channel doping parameter limit of International Technology Roadmap for Semiconductors(ITRS). Further, minimum electric field value of 0.02 MV/cm illustrating that mostly tunnelling take source-channel and epitaxial interface and least in the middle of proposed device body and significantly higher drain current flows as a result of line tunnelling. Fig. 15 depicts on current variation for different pocket doping concentration along the cut-line C-C' also schematic of device includes net doping concentration in all the region. It can be inferred as doping concentration increase electric field gets intensified near junction. Hence I_{ON} current increase but this increase in doping must follow International Technology Roadmap for Semiconductors(ITRS)[33]. However in our case pocket doping of $2 * 10^(19)$ is chosen as improvement in current and Sub-threshold-swing is noticed.

Fig. 16 From the output characteristics it can be seen that at low Vds channel potential grows as the drain potential rises, resulting in a significant increase in current. Once drain voltage exceed gate voltage channel potential turn to be independent of drain potential thus a good saturation value off drain current (0.325 mA/um at Vgs = Vds = 1.4 V) for proposed silicon ESVDG TFET and value of 4.5 uA/um at Vgs = Vds = 1.4 V for simulated reference device vertical Si dual material gate TFET. Thus ESVDG TFET outperforms with other two structures.

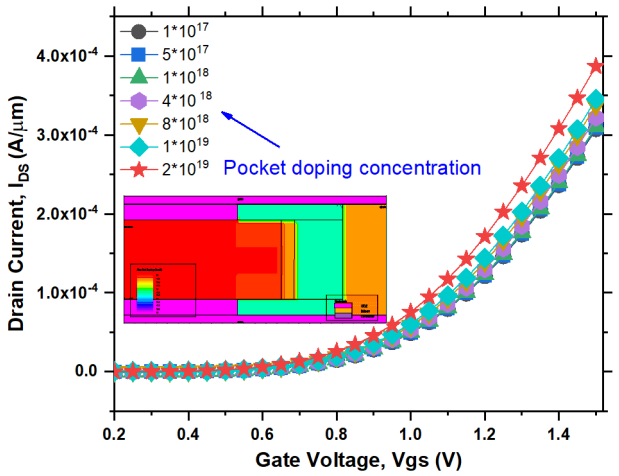

Fig. 15 Effect of change in pocket doping concentration on drain current.

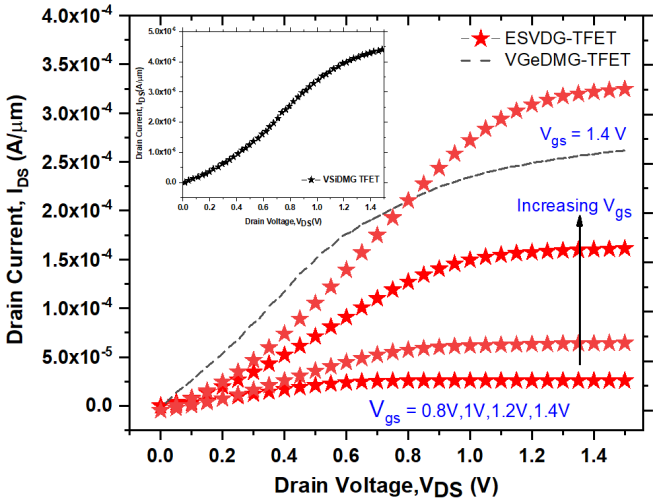

Fig. 16 Output characteristics plot of proposed silicon ESDG TFET at varying Vgs at Vds = 1 V)

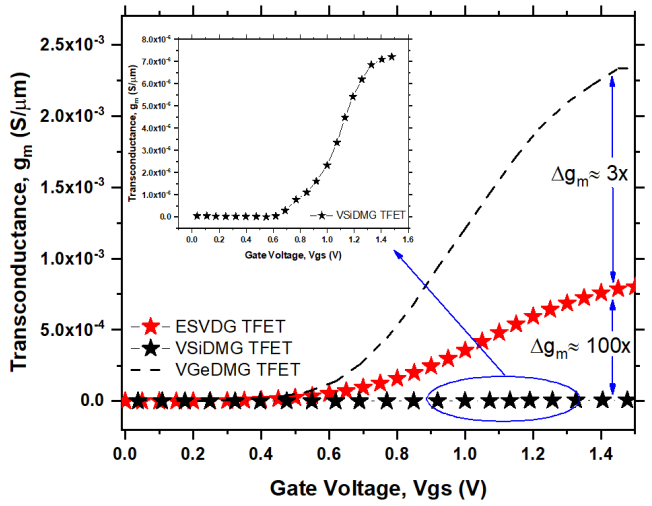

Fig. 17 Transconductance plot with varying Vgs at Vds = 1 V

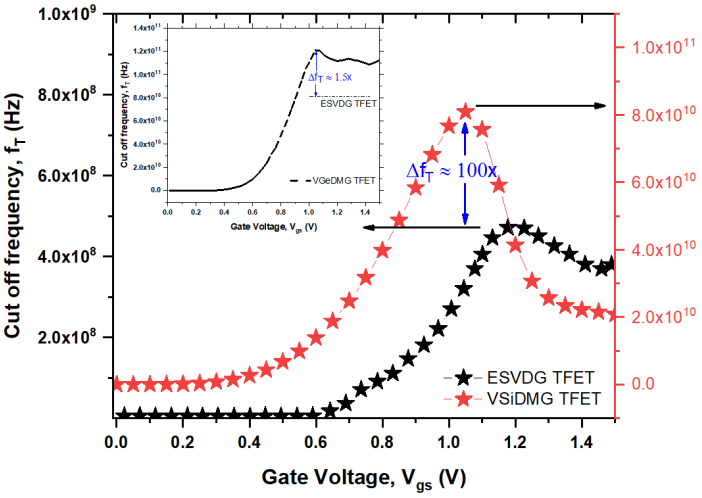

Fig. 19 Cut-off frequency (f_T) variation with Vgs at Vds = 1 V

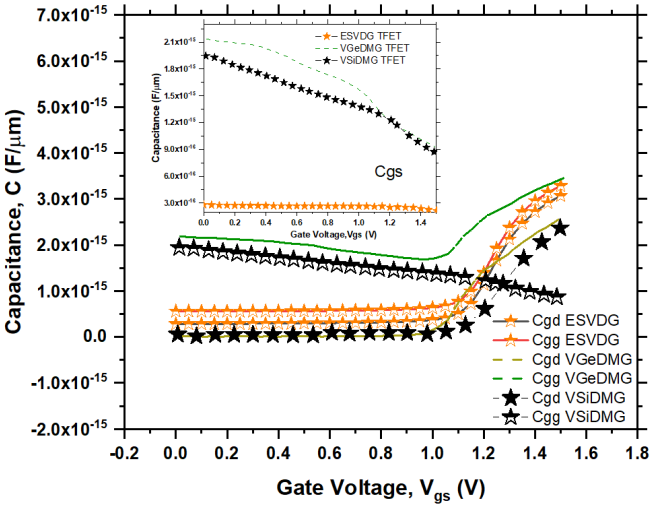

Fig. 18 Variation in capacitance's (Cgs, Cgd and Cgg) with increasing Vgs at vds = 1 V

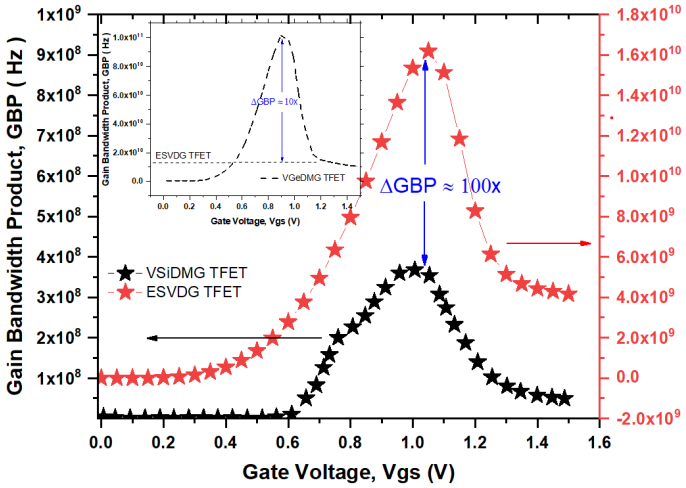

Fig. 20 GBP variation with Vgs at Vds = 1 V

Fig. 17 is a transconductance variation plot which is pivotal parameter for analog application. The amplification potential of a device is divulge by its transconductance that is more is the elevation, better is the input voltage conversion to current output as formulated in equation

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{2}$$

It can be seen from above figure improvement in transconductance ($\triangle g_m$) is in order of two decade between proposed device (silicon) and VSiDMG TFET and VGeDMG TFET shows only 3x improvement with ESVDG TFET.

3.2 AC analysis

The suggested device's suitability for RF applications is discussed next. The parasitic capacitance exploration is vital to study ac behaviour at high frequencies. The extraction of capacitance in the simulator is done though small signal analysis at frequency 1MHz. Response at high frequency is mainly governed by gm and total capacitance (Cgg). As it can be seen from Fig. 18 ESVDG TFET cgs value ranges from 0.279 fF to 0.215 fF which can be considered to have almost a constant value. At higher voltage (beyond 1V) slight decrements in the value of cgs occur due to reduction in gate to source coupling while cgd ranges from 0.28 fF to 3.15 fF and a significant increase in its value beyond 1V is observed due to accumulation of more no of carrier (electron) at the gate interface in the channel. Total capacitance (cgg) is determined by additive sum of cgs and cgd. Cgg below 1V is contributed by cgs and at higher voltage cgg follows cgd. It is evident from the figure, at high Vgs value ESVDG TFET shows higher Cgg value than simulated reference device vertical Si dual material gate TFET.

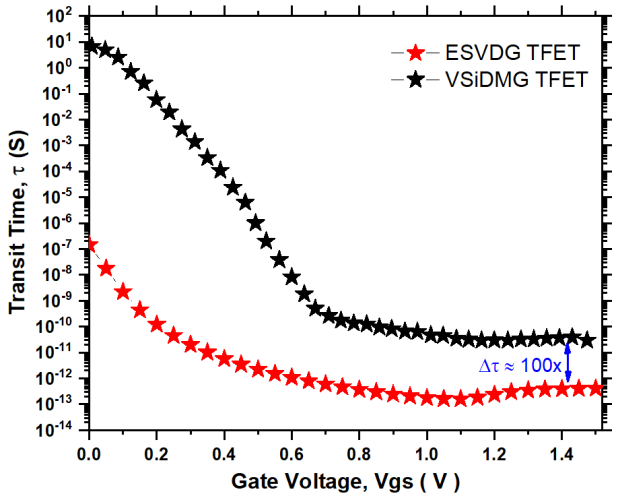

Fig. 21 Transit time variation with increasing vgs and constant Vds at 1 V for proposed silicon ESVDG TFET and simulated reference VSiDMG TFET

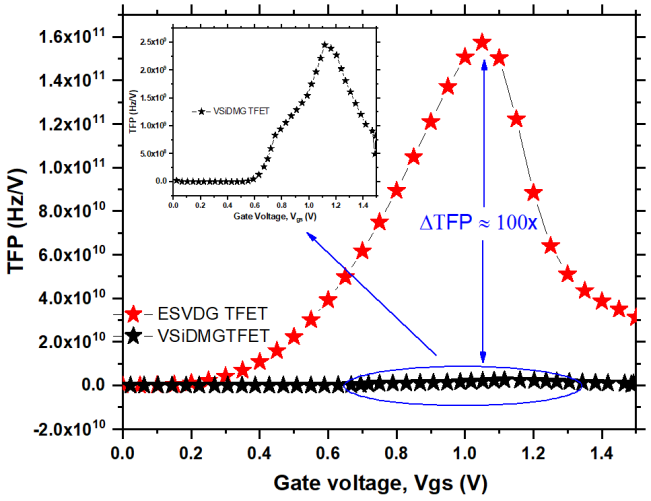

Fig. 22 Plot of TFP parameter variation with Vgs at Vds = 1 V

f_T, GBP and transit time, at high frequency are important parameter of concern. Higher the value of first two parameter of the device more suitable for numerous analog applications. The device cutoff frequency (f_T) is determined by gm and Cgg which can be formulated as

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1+2\frac{C_{gd}}{C_{gs}}}} \approx \frac{g_m}{2\pi C_{gg}} \tag{3}$$

From Fig. 19 it can be observed f_T increases with Vgs due to direct dependency on gm but as soon as it attains a peak value of 82GHz near 1V, it begins to decline due to rapid increase in the value of Cgg. However, An improvement of nearly two decade can be seen when compared with silicon ESVDG TFET and simulated reference device VSiDMG TEFT. Similarly it can be observed from Fig. 20 GBP increases with Vgs due to direct dependency on gm and inversely on Cgd but as soon as it attains a peak value of 16.8GHz near 1V, it begins to decline due to rapid increase in the value of Cgd. However, An improvement of nearly two order of magnitude can be seen when compared with silicon ESVDG TFET and simulated reference device VSiDMG TEFT. The device GBP which can be formulated as

Table 2 : Comparison table for analog/RF performance

Parameter	I_{on} / I_{off}	SS(mV/dec)	g_m (uA/um)	f_T (GHz)	GBP (GHz)	$\tau(psec)$
T-TFET[14]	10^7	14.07	-	-	-	-
VS TFET[12]	10^{11}	-	25	13	-	-
TGTFET[9]	10^{10}	24.4	232	11.9	2.3	-
VSiDMG[19]	10^{12}	37	7.37	0.482	0.376	0.448
ES TFET[11]	10^{12}	12.24	238	37.7	3.4	-
Proposed Work	10^{13}	10.1	800	82	16.8	1

$$GBP = \frac{g_m}{20\pi(C_{gd})} \tag{4}$$

In Fig. 21 the device's transit time is presented for varying Vgs at Vds = 1.0 V, as indicated in plot. In general higher switching speed (lower transit time) is the desirable characteristics for a device which can be formulated as

$$\tau = \frac{1}{20\pi * f_T} \tag{5}$$

At lower gate to source voltage τ seems to high due to low value cut-off frequency and decline with increase in Vgs. An overall improvement in silicon ESVDG TFET of nearly two order of magnitude can be observed when compared with simulated reference device VSiDMG TEFT. From Fig. 22 Similar observation in case of TFP parameter exist TFP expressed as $(g_m * f_T)/I_d$

4 Conclusion

The Silicon ESVDG-TFET is demonstrated with the source extended into the pocket followed by channel. The structural dimension of silicon ESDG-TFET have been optimised in order to increase line and point tunnelling. Atlas 2-D simulations are used to examine the proposed device's analog/RF performance parameters. The silicon ESVDG-TFET improves metrics like V_t, SS, I_{on} / I_{off}, g_m, f_T, and GBP significantly. Double gates structure have superior control over the tunnelling barrier at optimum dimensions, resulting in higher g_m, improved f_T, GBP, τ and TFP of order of two decade when compared with silicon based other vertical DG-TFET. Hence, Silicon ESVDG-TFET is a better candidate for low power switching and analog/RF performance applications.

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Consent for publication

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Author's contributions

O.K.Singh puts forward innovative results in this manuscript, completed the simulation work and article writing - Original draft preparation. D.Vaithiyanathan and B. Kaur participated in visualization, investigation, supervision, writing - review, and editing.

Competing interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Ethical approval and consent to participate

The authors declare that they have consent for participation.

Availability of data and materials

Not applicable

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