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Performance Evaluation of Epitaxial Layer Based Gate Modulated TFET (GM-TFET)

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Abstract: This paper reports the performance of an epitaxial layer (ETL) based gate modulated (GM-TFET) through 3D Technology Computer Aided Design (TCAD) simulations. The architecture utilizes effects of both vertical tunneling and lateral tunneling phenomena to improve the device performance. Attributes of the ETL, its thickness (t_{epi}) and doping concentration (N_{epi}) are varied and their impact on device electrical parameters such as transfer characteristic, output performance, subthreshold swing (SS), and threshold voltage (V_T) is highlighted. It is observed that both t_{epi} and N_{epi} significantly influence the different electrical parameters of the ETL based TFET architecture.

Keywords— *Electrical Characteristics, Epitaxial layer, Gate Modulated TFET, TFET, TCAD.*

1. Introduction

Over the year, extensive research is carried out to control the various restrictions of short channel effects (SCEs) of MOSFET [1]. In this aspect, novel devices with different operation mechanism is proposed in the literature. Tunnel Field Effect Transistor (TFET) which operates on band to band tunneling (BTBT) mechanism instead of thermionic emission and it has subthreshold swing (SS) below 60 mV/dec. at 300 K [2-3]. One of the foremost disadvantage of TFET is its low ON state current [4-5]. Various research have been presented through structural engineering to enhanced the ON current of TFET like silicon on insulator (SOI) TFET [6], heterojunction TFET (HJ-TFET) [7], circular gate TFET (CG-TFET) [8], double gate (DG) TFET [9], dual material gate (DMG) TFET [10] and many more. Also, epitaxial layer (ETL) based TFET architecture is proposed to make TFET suitable for low power applications [11-12]. The gate overlapped on the source and drain regions is one popular approach to enhance the performance of TFETs with high tunneling at ON state [13]. Furthermore, source pocket doped with line tunneling TFET has been highlighted to improve the conduction of TFET [14]. The ETL based TFET provide the vertical tunneling along with lateral tunneling, which improves the tunneling probability and enhanced the ON current [15]. Such ETL based TFET is a potential candidate to boost the performance of TFET. A gate modulated (GM)-TFET having ETL with improved ON current for the variation in gate and drain bias is reported [16]. The source/drain lateral straggle (σ) influence on analog and high frequency performance of GM-TFET is investigated in literature

[17]. Also, the linearity performance of GM-TFET for the variation of σ parameter is highlighted [16]. However, the performance of GM-TFET is not evaluated for various ETL thickness and doping concentration of the ETL.

In this work, the effect of ETL thickness (t_{epi}) on transfer characteristic, output characteristic, SS and threshold voltage (V_T) of GM-TFET is reported at fixed value of doping concentration of the ETL (N_{epi}) through Technology Computer Aided Design (TCAD) device simulator. We also highlighted the effect of N_{epi} on these electrical parameters of GM-TFET at fixed value of t_{epi} .

The organization of the paper is as follows: Section II describes the device architecture along with simulation methodology. Section III provides the simulation results obtained from simulator and the same is discussed here. This work is summarized in Section IV.

2. Device structure and Simulation descriptions

Fig. 1. Schematic of GM-TFET with ETL.

The 2D representation of the GM-TFET with ETL is shown in Fig. 1. The epitaxial layer of the ETL GM-TFET is placed over the source and channel portions i.e. under the gate dielectric layer. In conventional TFET structure only lateral tunneling is present at tunnel junction perpendicular to gate field. In ETL GM-TFET, the vertical tunneling along with lateral tunneling improves the conduction mechanism of TFET [14]. Here, source, drain, channel as well as the epitaxial layer (ETL) is made of Silicon. SiO_2 having dielectric constant of 3.9 is taken as buried oxide, whereas, HfO_2 having dielectric constant of 22 is considered as gate dielectric. Metal having work function (ϕ_M) = 4.02 eV is taken as gate material. The uniform doping concentration is considered for all regions. The p^+ source doping concentration of (N_S) = 10^{20} cm^{-3} is considered as greater than n^+ drain doping concentration (N_D) = $5 \times 10^{18} \text{ cm}^{-3}$ to minimize the ambipolar

current [18]. The intrinsic channel has doping concentration (N_{ch}) = 10^{15} cm^{-3} , whereas, doping of epitaxial layer (N_{epi}) is varied, otherwise mentioned. The various dimensions of the parameters as shown in Fig. 1 are listed in Table 1.

TABLE I
VARIOUS DEVICE DIMENSIONS OF ETL GM-TFET

Parameter	Value (nm)
Length of source region (L_{S1})	75
Length of intrinsic region (L_{int})	25
Length of drain region (L_D)	30
Length of gate region (L_G)	100
Silicon layer thickness (t_{Si})	20
Height of BOX (t_{box})	145
Height of bulk (t_{bulk})	10
Oxide thickness (t_{ox})	3
Epitaxial layer thickness (t_{epi})	varies

Sentaurus TCAD tool is used for the simulation of the device [20]. Masetti mobility model is considered to study impact of doping concentration on charge carriers and Fermi Dirac distribution is enabled due to presence of degenerate source/drain regions. As tunneling probability is dependent on energy bandgap and thus bandgap narrowing model is adopted. The recombination of the carriers is considered by enabling SRH model in simulator. The transport of the carriers in simulator is activated by considering non-local BTBT Kane's model in simulator, which captures BTBT at the required junction. The experimentally calibrated fitting parameters of BTBT is chosen in simulator are: $A_{path} = 1.63 \times 10^{14} \text{ cm}^{-3} \text{ s}^{-1}$, $B_{path} = 1.47 \times 10^7 \text{ V cm}^{-1}$, $P_{path1} = 0.0567 \text{ eV}$ [21].

3. Results and Discussion

This section described the influence of epitaxial layer thickness (t_{epi}) and doping concentration of ETL (N_{epi}) on transfer characteristic, output characteristic, SS, and V_T of ETL based GM-TFET through device simulator. The drain to source bias (V_{DS}) = 0.5 V is taken. The threshold voltage reading is taken from simulator through maximum transconductance method.

3.1 Influence of Epitaxial Layer Thickness (t_{epi})

Here, the analysis is presented for $t_{epi} = 4, 6, 8$, and 10 nm at fixed $N_{epi} = 10^{15} \text{ cm}^{-3}$.

The effect of t_{epi} on transfer characteristic by varying t_{epi} from 4 to 10 nm with step of 2 nm, while keeping all other dimensions fixed, in linear and log scale are presented in Figs. 2 (a) and

(b), respectively. It is seen that ON current increases significantly, whereas, OFF current degrades insignificantly, with the decrease in t_{epi} . This improvement in ON current can be better explained from Fig. 3, where we have plotted eBTBT rate at source-channel junction for $V_G = 1.5$ V and $V_{\text{DS}} = 0.5$ V, taking t_{epi} as parameter. It is perceived from Fig. 3 that the BTBT rate increases for lower value of t_{epi} which signifies improvement on ON current of the device as summarized in Fig. 2(a).

The effect of t_{epi} on output characteristic for $V_G = 0.5$ V, of ETL based GM-TFET is portrayed in Fig. 4. It is perceived (Fig. 3) that eBTBT rate rises with reduction in t_{epi} , which indicates carrier can easily flow from source to drain as t_{epi} changed from 10 to 4 nm. Thus, the drain current saturation occurs at large V_{DS} for high value of t_{epi} , whereas, for low value of t_{epi} saturation occurs at low value V_{DS} .

Fig. 2. Effect of t_{epi} on transfer characteristic in
a) Linear and b) Log scale.

Fig. 3. Effect of t_{epi} on eBTBT rate.

The variation in SS and V_T taking t_{epi} as parameter is shown in Fig. 5. As the subthreshold characteristic improves with rise in t_{epi} , which leads to improvement in switching performance

and accordingly, SS value decreases. The reduction in t_{epi} increases ON current, which in turn reduces the threshold voltage to turn on the device.

Fig. 4. Effect of t_{epi} on output characteristic.

Fig. 5. Effect of t_{epi} on SS and V_T .

3.2 Influence of Epitaxial Layer Doping Concentration (N_{epi})

This section discussed the electrical parameters by changing N_{epi} from 10^{15} to 10^{18} cm^{-3} while keeping other design parameter constant at fixed $t_{\text{epi}} = 8 \text{ nm}$.

Fig. 6. Effect of N_{epi} on transfer characteristic in

a) Linear and b) Log scale.

The influence of N_{epi} on input characteristic in linear and log scale are presented in Figs. 6(a) and (b), respectively. It is seen that with increased N_{epi} , there is improvement in ON current as well as minute degradation in OFF current. As concentration of epitaxial layer increases, which enhanced the BTBT rate at tunnel junction and accordingly, improves the ON current.

The output performance as a function of N_{epi} is portrayed in Fig. 7. It can be summarized that electrons can travel fast from source to drain regions with increased in N_{epi} , which indicates the drain current saturates at large drain bias as N_{epi} is changed from 10^{15} to 10^{18} cm^{-3} .

Fig. 7. Effect of N_{epi} on output characteristic.

Fig. 8. Effect of N_{epi} on SS and V_T .

SS of MOSFET can be expressed as [22]:

$$SS = \ln_{10} 10 \left(\partial V_{GS} / \partial \ln(n_m) \right) \quad (1)$$

The minimum concentration is expressed as

$$n_m = n_i^2 / N_{\text{epi}} \exp(\phi_{S,\text{min}} / \phi_t) \quad (2)$$

The inversion charge carriers Q_{inv} of MOSFET is given by [23].

$$Q_{inv} = \int_0^w \left(\frac{qn_i^2}{N_{epi}} \right) \exp(\phi_{s,min} / \phi_t) dy \quad (3)$$

where, n_i is the intrinsic concentration, q is the electronic charge, $\phi_{s,min}$ is the minimum potential, and ϕ_t is the thermal voltage. This Q_{inv} is related charge is directly related with the threshold voltage.

The influence of N_{epi} on both SS and V_T is summarized in Fig. 8. As OFF current of ETL based GM-TFET increases with rise in N_{epi} , which degrade the corresponding SS value. It is examined also from (1) and (2), the SS is inversely related with N_{epi} , which leads to degradation in SS value with increased N_{epi} .

Also, less V_T is needed to make the device on with increased N_{epi} and this is primarily due to enhanced ON current with rise in N_{epi} . It is also observed from (3) that Q_{inv} reduces with the increased in N_{epi} and this decreases the required gate bias to activate the channel.

4. Conclusion

We have elaborated the performance of ETL based GM-TFET for the variation of ETL thickness (t_{epi}) and doping concentration of ETL (N_{epi}). Simulation results reported that the increased in t_{epi} degrades the ON current and improves SS of GM-TFET. The roll-off in threshold voltage (V_T) is observed when t_{epi} decreases from 10 to 4 nm. Furthermore, the increase in N_{epi} , enhanced the ON current, whereas, degrade the SS of GM-TFET. It is also analyzed that upto $N_{epi} = 10^{17} \text{ cm}^{-3}$ the roll-off of V_T is lesser and when N_{epi} increases to 10^{18} cm^{-3} the V_T falls by significant amount. The output current improves for low (high) values of t_{epi} (N_{epi}) in GM-TFET. Therefore, lower value of t_{epi} with heavily doped ETL (N_{epi}) can boost the performance of GM-TFET.

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Compliance with ethical standards:

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