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Article

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All-solid-state Ion Synaptic Transistor for Wafer-scale Integration with Electrolyte of a Nanoscale Thickness

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Abstract

Neuromorphic hardware computing is a promising alternative to von Neumann computing by virtue of its parallel computation, and low power consumption. To implement neuromorphic hardware based on deep neural network (DNN), a number of synaptic devices should be interconnected with neuron devices. For ideal hardware DNN, not only scalability and low power consumption, but also a linear and symmetric conductance change with the large number of conductance levels are required. Here an all-solid-state polymer electrolyte-gated synaptic transistor (pEGST) was fabricated on an entire silicon wafer with CMOS microfabrication and initiated chemical vapor deposition (iCVD) process. The pEGST showed good linearity as well as symmetry in potentiation and depression, conductance levels up to 8,192, and low switching energy smaller than 20 fJ/pulse. Selected 128 levels from 8,192 used to identify handwritten digits in the MNIST database with the aid of a multilayer perceptron, resulting in a recognition rate of 91.7 %.

Keywords: all-solid-state, artificial neural network (ANN), deep neural network (DNN), electrolyte-gated synaptic transistor (EGST), initiated chemical vapor deposition (iCVD), neuromorphic system, polyethylene glycol di-methacrylate (pEGDMA), synapse device, wafer-scale

Introduction

Artificial neural networks (ANN), have been intensively explored with the requirements of many applications[1–5]. Among various kinds of ANN, the deep neural network (DNN) is a well-studied training method, and hardware electronic devices have been actively investigated in efforts to realize DNN with low-power consumption. In the hardware DNN, a number of synaptic devices need to be interconnected with multiple neuron devices, to process cognitive tasks such as image[6,7] and speech recognition[8]. Therefore, mass production of synaptic device at wafer-scale fabrication is inevitable. Concurrently, to achieve high performance, linear and symmetric conductance changes are required[9–11].

Emerging 2-terminal devices are promising candidates due to cost-efficiency, and scalability[12–15]. However, they suffer from non-linear and asymmetric conductance changes. In addition, additional selector components are needed to pick up the target cell, without a sneak-path[15,16]. Alternatively, 3-terminal synaptic transistors have attracted interests to resolve the aforementioned problems. They have advantages of low power consumption without a sneak-path by gate modulation, and improved controllability of the synaptic weight[17–19]. It also provides a parallel 'write' and 'read' operations[20]. However, a synaptic transistor that shows excellent linearity, symmetry with a high dynamic range (HDR), and sufficiently low energy consumption, is still missing.

The electrolyte-gated transistor (EGT) may be an advanced candidate to address these issues. The EGT is controlled by ions in an electrolyte-gate. The approach has attracted considerable attention because of its similarity to an actual biological system, where the membrane potential is governed by ions such as Ca^{2+}, Na^{+}, and K^{+} [21–23]. In EGTs, a gate dielectric in a conventional MOSFET is replaced by electrolytes with movable ions (*e.g.*, H^{+}, Li^{+}, O^{2-})[24–30]. When gate voltage is applied, movable ions form an electric double layer (EDL). It causes hysteresis, and adjusts the synaptic weight. EGT-based synapses have shown a relatively linear conductance

change because of continuous ion migration inside the electrolyte[28]. However, scalability, wafer-scale microfabrication, and reliability have been issues, because of their reliance on a liquid-based electrolyte and mechanical exfoliated channels. Such Limitation affects the power consumption and switching speed[20], and wafer-scale fabrication of EGTs is essential for the architecture of neuromorphic systems where more than 10^{15} synapses may be used to mimic a human brain[31].

In this work, we demonstrate a polymer electrolyte-gated synaptic transistor (pEGST) composed of an all-solid-state polymer electrolyte and a silicon-channel. For the fabrication of the pEGST, an ultra-thin electrolyte was deposited by vapor phase using the initiated chemical vapor deposition (iCVD). This is a solvent-free, one-step polymerization for generating high-performance polymer electrolyte films[32]. Protons (H^+) incorporated in the polymer electrolyte were selected for CMOS compatibility. Unlike previous EGTs using an ionic liquid or ionic gel, the pEGST is scalable to nanoscale thickness with the aid of iCVD. While previous EGSTs have been fabricated in a single device, the pEGST was manufactured in wafer-scale. The pEGST showed high-performance, with linear and symmetric weight update consuming low energy, less than 20 fJ/pulse. Remarkably, the multi-levels of conductance were achieved, up to 13 bits. The attained MNIST recognition rate was 91.7%.

Results and discussion

Structure and fabrication of pEGST

Figure 1a provides a schematic of the proposed pEGST and depicts the chemical structure of polyethylene glycol di-methacrylate (pEGDMA), which was used as a solid-state gate dielectric to harness the electrolyte's properties. **Figure 1b** shows a transmission electron microscopy (TEM) image of the cross-sectional structure, to identify each layer of the fabricated pEGST. The gate dielectrics are composed of three layers: formed aluminum oxide of 3 nm on top, pEGDMA of 20 nm in the middle, and thermally grown SiO_2 of 2 nm on the bottom, as shown in a cross-sectional TEM image in **Figure 3a**. The gate electrode is made of aluminum and its thickness is 300 nm. The nominal gate length (L_G) of the pEGST was 7 μm and its channel width (W_{ch}) was 50 μm. It was presumed that the 3 nm of aluminum oxide between the Al gate and the pEGDMA was formed by aluminum anodizing during ion migration when gate bias was applied. An interfacial layer of the SiO_2 between the pEGDMA and the silicon channel, was intentionally grown with thermal oxidation to minimize interface trap density, and to suppress gate leakage current during switching to control synaptic weights.

Figure 1c shows the key fabrication steps for the pEGST, which was fabricated on a p-type (100) 4-inch silicon wafer. For device-to-device isolation, SiO_2 of 1 μm served as a field oxide was thermally grown. For gate-last process, source and drain (S/D) were formed by high dose phosphorous implantation with a dummy gate. Rapid thermal annealing (RTA) in N_2 ambient was employed to activate the dopant. Gate dielectrics composed of the interfacial thermal oxide and the pEGDMA were sequentially stacked after the removal of dummy gate. The Al gate was deposited with the aid of DC magnetron sputter. The gate electrode was patterned by conventional photo-lithography and subsequent etching. Details of the step-by-step fabrication and iCVD processes are described in Supplementary Information 1 and 2.

To ensure highly uniform pEGDMA, vapor-phase iCVD was employed[33,34]. Unlike the liquid

or ionic gel-type electrolyte typically used in conventional EGST, the wafer-scale pEGDMA deposited via the iCVD process can be fully realized with matured complementary metal-oxide-semiconductor (CMOS) technology. **Figure 1d** shows a schematic of the iCVD chamber used for the polymerization of the ultra-thin polymer films. The iCVD process is a solvent-free vapor-phase process for depositing various kinds of high-purity polymer films with outstanding uniformity, and conformality. The iCVD polymerization process can be briefly summarized as follows: i) injection of monomer and initiator, ii) thermal decomposition of the initiator to form radicals, iii) collision between radicals and monomers, and iv) free radical formation of the polymer thin films. The effectiveness of surface-growing mechanism was demonstrated on an 8-inch wafer via at low temperature (~ 40 °C)[35]. A chemical structure of the deposited pEGDMA film was analyzed by Fourier transform infrared (FT-IR) spectroscopy, as described in the Supplementary Information 3[36].

Figure 1e shows the fabricated 4-inch Si wafer demonstrating the wafer-scale manufacturability of the pEGSTs, containing 30 dies. The die size is 1×1 cm^2, as shown in the inset in **Figure 1e**. CMOS compatibility and the iCVD electrolyte deposition method also leave plenty of room for down-scaling with future structural innovation (See Supplementary Information 4).

Electrical characterization of the pEGST

Figure 2a shows the measured I_D-V_G curve of the pEGST at a drain voltage (V_D) of 50 mV. The counter-clockwise hysteresis of protons in the pEGDMA was observed with double sweeps of the V_G from -6 V to +6 V forward and from +6 V to -6 V backward. The counter-clockwise direction of the hysteresis, electrolyte characteristics, and ion mass spectrometry supports the conclusion that the closed loop is not produce by electrons tunneling through the gate dielectrics, as is usually observed in a conventional charge-trap memory-based synaptic device,

147 but by positive ions in the electrolyte-based synaptic device.

148 This movement of positive ions in the solid-phase electrolyte of the pEGST, exhibits
149 horizontally wide hysteresis of back-sweep current (BSC) with a vertical ratio of on-state
150 current (I_{ON}) to off-state current (I_{OFF}) of 10^4 at $V_G = 0$ V in the I_D-V_G curve. It should be noted
151 that a wide voltage window of hysteresis is preferred for multiple-level synaptic functionality,
152 because it allows a broad range of channel conductance (G_{DS}) changes across the source (S)
153 and drain (D) with an applied gate electric field.

154 Note that wafer-scale fabrication is essential for chip-based neuromorphic systems where
155 more than a thousand synaptic devices need to be connected to one neuron device. Unlike
156 previously reported EGST that could not be fabricated at wafer-scale owing to liquid processes
157 that use ion gel and ionic liquid electrolytes, the reliable wafer-scale pEGSTs could be
158 fabricated as an all-solid-state thin film using the iCVD and CMOS-compatible
159 microfabrication (See Supplementary Information 5).

160 It is particularly essential that the chip-level system is capable of *in situ* on-chip learning via
161 weight update with on-the-fly training. **Figure 2b** shows the device-to-device variability of the
162 fabricated pEGSTs across the 4-inch silicon wafer. The averaged threshold voltage $V_{T,forward}$ of
163 1.25 V and $V_{T,backward}$ of −1.24 V is uniform. The averaged hysteresis window of 2.49 V, which
164 is defined as $\Delta V_T = V_{T,forward} - V_{T,backward}$, is also uniform. In both figures, error bars represent
165 standard deviations. These data were extracted from four randomly selected devices from 15
166 chips (for a total 60 pEGSTs) across the entire 4-inch wafer. As shown in **Figure 2c** and **d**, each
167 I_D is modulated by the number of identical pulse widths applied to the gate electrode, which
168 are distinctive for potentiation and depression (P/D), respectively. Each distinguishable I_D
169 corresponds to a weighting state during the P/D in the multi-level states for synaptic operations.

170

171 **Electrolyte characteristics of pEGDMA**

To clarify the origin of the counter-clockwise hysteresis in the pEGST, the dynamic behaviors of the pEGDMA used as the electrolyte gate dielectric were analyzed by gate capacitance-frequency (*C-f*) and phase angle-frequency (θ-*f*) characterization. As shown in **Figure 3b**, a bell-shaped profile of θ was measured[37]. In general, θ in an ionic relaxation dominant region is known to be larger than - 45°, however, it was smaller than that in the pEGST. This was caused by the thermally grown interfacial SiO_2 layer. SiO_2 is an excellent insulator, which causes the capacitive dominance from the dipole relaxation to competed with the resistive dominance from the ionic relaxation. The anodized aluminum oxide can additionally minimize the θ value because of its dielectric characteristics[38].

Figure 3c shows a schematic of the ion distribution under equilibrium without applied gate voltage. When a positive voltage is applied to the gate, H^+ in the pEGDMA move closer to the channel, as shown in **Figure 3d**. When negative voltage is applied to the gate, it moves farther from the channel, as shown in **Figure 3e**. A depth profile of protons from the Si-channel via the interfacial SiO_2 to inside the pEGDMA, was analyzed using time-of-flight secondary ion mass spectrometry (ToF SIMS). It confirmed that the concentration of protons in the doped sample was larger than in the undoped one, and the proton concentration becomes higher toward the gate electrode after applying negative voltage at the gate electrode. Other relevant ion concentrations were also analyzed and compared with the proton concentration, as shown in Supplementary Information 6. The bias dependent mobile ions in the polymer electrolyte properly modulate the G_{DS} by controlling the density of carriers in the silicon channel. In addition, the pEGDMA including protons induce a wide enough hysteresis to realize synaptic characteristics in the hardware-based analog DNN.

The I_D-V_G characteristics of the pEGST were also investigated at high temperature (T) over the range of 25 °C to 180 °C (see Supplementary Information 3). Hysteresis voltage (ΔV_T) increased as T increased (**Figure S5**). This tendency is caused by accelerated ion migration in

the polymer electrolyte at high *T*. In addition, it was confirmed by FT-IR spectroscopy that the chemical structures in the polymer electrolyte film were not changed even after high temperature treatment at 180 ºC (**Figure S6**).

Synapse characteristics of pEGST for analog deep neural networks

In the pEGST, the G_{DS} change with each update in synaptic weight was characterized to estimate the linearity and asymmetric ratio (AR), which are important metrics for evaluating the accuracy of a pattern recognition rate in neural network simulations. **Figure 4a** shows the identical pulse scheme used, with constant voltage amplitude and time duration, to control P/D and read operations. An optimal pulse scheme is V_{pot} = + 4 V with 10 ms for the potentiation and V_{dep} = - 5.3 V with 10 ms for the depression. The read voltage used to measure the G_{DS} between each P/D pulse was set to 0.1 V, which was small enough to minimize the effect of ion drift in the pEGDMA. Thus, the reading operation did not influence on the G_{DS} determined by the programming and the erasing. Energy consumption for the potentiation and depression was less than 20 fJ/pulse (See Supplementary Information 7). This is comparable to the energy consumption of a biological synapse in the human brain (10 fJ/spike)[39], and it is advantageous in terms of energy consumption in on-chip learning.

A G_{DS} of 8192 (=2^{13}, 13 bits) levels was achieved for each P/D. This is the largest number of multi-levels reported with HDR ever reported, as shown in **Figure 4b**. Here the dynamic range is a conductance window in between the minimum and the maximum conductance. A silicon channel MOSFET with a well-controlled off current can achieve high on/off switching characteristics. Such more than thousands of multi-states conductances are the result of harmonizing the continuous distribution of protons inside the polymer electrolyte with the characteristics of the silicon channel MOSFET. Note that its nominal ratio of on-state I_D to off-state I_D is larger than 10^5. This feature of the HDR is one of the reasons why the ion

222 incorporated solid-state electrolyte needs to be implemented on the silicon channel MOSFET.

223 This HDR is attractive for improving the recognition rate by selecting highly linearized
224 fraction of conductance changes from the entire P/D region. It is also preferable for customizing
225 energy consumption to be adjustable to a target application and for providing a degree of
226 freedom in circuit design. In this work, conductance levels of 128 (=2^7; 7 bits) were selected
227 from those of 8,192 (=2^{13}; 13 bits) uniformly distributed in the entire P/D region for evaluating
228 a rate of pattern recognition, because they are high enough to acquire it in MNIST recognition.
229 **Figure 4c** shows the extracted 128 conductance levels obtained by applying an identical
230 training pulse, without the aid of external circuits.

231 In order to quantitatively evaluate the linearity of the G_{DS} change, a non-linearity parameter
232 α was calculated using the following equation[11]:

233 $$G = \begin{cases} ((G_{max}^{\alpha} - G_{min}^{\alpha}) \times w + G_{min}^{\alpha})^{1/\alpha} & if\ \alpha \neq 0, \\ G_{min}^{\alpha} \times (G_{max}/G_{min})^{w} & if\ \alpha = 0. \end{cases} \quad (1)$$

234 , where G_{max} and G_{min} are the maximum and minimum channel conductance, α is a parameter
235 that controls potentiation (α_{pot}) or depression (α_{dep}), and w is an internal variable which ranges
236 from 0 to 1. α_{pot} and α_{dep} close to one is ideal for linear and symmetric conductance change, to
237 improve MNIST classification accuracy in the DNN. In the pEGST, the extracted α_{pot} and α_{dep}
238 under the identical gate pulse amplitude and width were 1.51 and 0.38, respectively. They were
239 affected by the magnitude of the gate pulse amplitude and width (see Supplementary
240 Information 8). In addition, the measured G_{DS} was slightly deviated from the linearly fitted line
241 with α_{pot} and α_{dep}. This regression error (e_{reg}) was very small, *i.e.*, $e_{reg,pot}$ = 0.007 and $e_{reg,dep}$ =
242 0.006. This feature is attractive not only for avoiding unstable operation induced by device
243 variability, but to improve the accuracy of pattern recognition while saving energy. It is well
244 known that the smaller regression error for the weight update can induce high learning accuracy
245 as the number of training epochs increase[40–42].

On the other hand, the aforementioned asymmetric ratio (AR) can reflect how much the potentiation slope differs from the depression slope. The AR was also assessed using the following equation[25]:

$$AR = \frac{\max|G_p(n) - G_d(n)|}{G_p(128) - G_d(128)} \quad \text{for } n = 1 \text{ to } 128 \qquad (2)$$

, where $G_p(n)$ and $G_d(n)$ are the channel conductance values after the n^{th} potentiation and depression pulses, respectively. For ideal symmetry, the AR should be 0. The pEGST in this work showed a small AR of 0.29, which indicates good symmetry. Whereas the AR is in a range of 0.43 to 0.83 for two-terminal based devices with identical pulses, it is in the range of 0.19 to 0.31 for other liquid based EGTs[23–26] (see Table 1 and Table S1).

Figure 4 d shows the cyclic endurance after more than 100,000 operations, updating the synaptic weight. The G_{max} decreased to less than 12 % after 10^5 cycles with the same pulse scheme described above. Moreover, the cycle-to-cycle variation induced by the iterative operations was smaller than those in other types of silicon based synaptic devices, such as ferroelectric FETs, and charge-trap based memories[43–46]. **Figure 4e** and **f** show the retention characteristics of the pEGST after each step in the conductance update.

Schematic of the array and neural network simulation

Figure 5a shows a schematic of a feasible 3-terminal based pEGST array for an analog neural network system. In the neural network system, the crossbar array architecture has two key kernels: for parallel weight updates and the vector-matrix multiply-accumulate operation (*e.g.*, MAC)[31]. Reflecting a 3-terminal MOSFET structure, these can be realized because the weight update is enabled via the gate, the simultaneous reading of conductance is allowed via the drain, and the accumulation of signals is accomplished via the source.

A 3-terminal synaptic device was previously developed to demonstrate the potential of

parallel programming, which can update synaptic weight during supervised learning (*e.g.*, backpropagation)[47,48]. In a feasible synapse array, a 'write' pulse denoted by the green line on the left side of **Fig. 5a,** is independently applied to each synaptic device to carry out the weight updates, and a 'read' pulse, marked with a yellow line on the right side of **Fig. 5a,** is applied to the drain electrode to read out the level of weighted analog conductance. As a result, the writing and reading operations can be concurrently performed by the 3-terminal structure, which is superior to a conventional 2-terminal based synaptic device for efficient neural network. The accumulated voltage, which is multiplied by the read-out current and synaptic weight conductance, is transmitted to a postsynaptic neuron via a source in order to perform the vector-matrix MAC operations. A feasible procedure for fabricating a high-density pEGST array with a vertical pillar structure is shown in the Supplementary Information (see Supplementary Information 4).

To evaluate the functionality of the fabricated pEGST for pattern recognition, a hand-written dataset (Modified National Institute of Standards and Technology (MNIST)) was used, and supervised learning with backpropagation was carried out. Multi-layer perceptron (MLP) was composed of 24 × 22 input neurons cropped from 28 × 28 pixels, 250 and 125 neurons for the 1st and 2nd hidden layers, and 10 output neurons for the neural network simulations, as shown in **Figure 5b** (see Supplementary Information 9 for details pertaining to the neural network system)[49]. Recognition accuracy after each training epoch is shown in **Figure 5c.** In the simulations, the fabricated pEGST achieved a recognition accuracy of 91.7 % after 30 training epochs, which is comparable to the 92.7 % that was obtained from an ideal synapse. Here the ideal synapse is a device which has 128-levels of multi-states, perfect linearity (α=1), and complete symmetry (AR=0) in conductance change. In this study, the high level of the recognition accuracy is attributed to the number of multi-states more than 128-levels, good linearity (α_{pot}=1.51 and α_{dep}=- 0.38), and reasonable symmetry (AR=0.29) in conductance

change.

Figure 5d shows the recognition accuracy for the MNIST dataset according to the number of conductance levels. To exclude side effects arising from other factors that can influence the accuracy of the recognition, other parameters such as G_{max}, G_{min} and linearity were fixed. As previously mentioned, the 128 extracted conductance levels were enough to achieve highly accurate the pattern recognition. Note that there was no notable increase in the recognition accuracy with more than 128 extracted conductance levels. **Table 1** compares the intraspecific structures of various electrolyte-gated FETs and their synaptic properties with the pEGST. In addition, other interspecific synaptic devices are compared with the pEGST in Supplementary Information 10.

Conclusion

An all-solid-state polymer electrolyte-gated synaptic transistor (pEGST) was implemented on a silicon channel, and demonstrated high performance in an analog deep neural network. As the solid-state electrolyte, pEGDMA including protons (H^+) was used for the first time. Unlike liquid or ionic gel-type electrolytes that have been used in a conventional EGSTs, the pEGDMA deposited via the iCVD process at a wafer-scale allows the full utilization of mature CMOS microfabrication technology. This reduces process-induced variability across the wafer. The pEGST showed conductance control with bidirectional analog, linear and symmetric synapse behavior. It achieved notable performance as a synapse device with weight updates of more than 8,192-levels with fine conductance control. The pEGST also demonstrated an excellent recognition accuracy of 91.7 % for the MNIST dataset. The pEGST provides a feasible pathway to realize a bio-inspired electrolyte synapse for chip-level integration thanks to its wafer-scale CMOS-compatibility.

Methods

Device fabrication: See Supplementary Information 2 for details of the fabrication process.

iCVD process: To deposit the conformal and uniform thin polymer electrolyte film, vaporized ethylene glycol dimethacrylate (EGDMA) monomer was flowed into a pressure-controlled vacuum chamber with a tert-butyl peroxide (TBPO) initiator. The ratio of the flow rate between the monomer and initiator was 1:1, and a proportional-integral-derivative (PID) controller kept the chamber pressure at approximately 60 mTorr. In the vacuum chamber, a heated filament thermally decomposes the initiator and produces the radical, which activates the vinyl group in the monomer. The polymerization reaction and adsorption occur simultaneously on the surface of the samples, with a substrate temperature of 40 °C.

Device characterization: Electrical characteristics of the fabricated pEGST were measured using a B1500 semiconductor parameter analyzer with PMU module (Agilent Technologies) using optimized pulse schemes. Each I_D–V_G curve was obtained by sweeping the applied voltage from 0 V to less than ±6 V with a 0.05 V step. '+' indicates forward sweep and '-' is backward sweep. Capacitance-frequency (*C-f*) and phase angle-frequency (θ-*f*) measurements were also carried out using a E4980A LCR meter (Agilent Technologies) at a frequency range of 1 kHz to 1 MHz with a small AC signal voltage of 30 mV. And DC 2 V were was superimposed to the AC signal to make channel inversion. To get measurable capacitance, a large-sized pEGST with an L_G of 50 μm and W_{ch} of 50 μm was selected.

TEM analysis: TEM images were taken using high-resolution corrected scanning transmission electron microscopy (JEM-ARM200F) with EDS mapping (Bruker Quantax 400).

FT-IR analysis: To confirm the chemical structure and heat resistance of the pEGDMA thin film, FT-IR spectroscopy (Nicolet iN10MX) was used.

ToF-SIMS analysis: To confirm the ion mass in the pEGDMA film, time of flight secondary ion mass spectrometry (ToF-SIMS) from Ion-ToF GmbH was used. Each 400 μm × 400 μm

sample was comprised of a silicon channel, interfacial silicon dioxide and pEGDMA.

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Author Contributions

J.-M. Yu, J. Hur and Y.-K. Choi conceived the idea and designed the experiments. J.-M. Yu, C. Lee, D.-J. Kim, H.-G. Park, M.-S. Kim, and M. Seo fabricated the devices. J.-M. Yu, D.-J. Kim and J.-K. Han performed the experiments and data analysis. J.-K. Kim performed the neural network simulation. J.-M. Yu wrote the manuscript. S.G. Im and Y.-K. Choi supervised the project on the relevant portions of the research. All authors discussed the results and commented on the manuscript.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Code availability

The codes used for plotting the deep neural network simulation data are available from the corresponding author on reasonable request.

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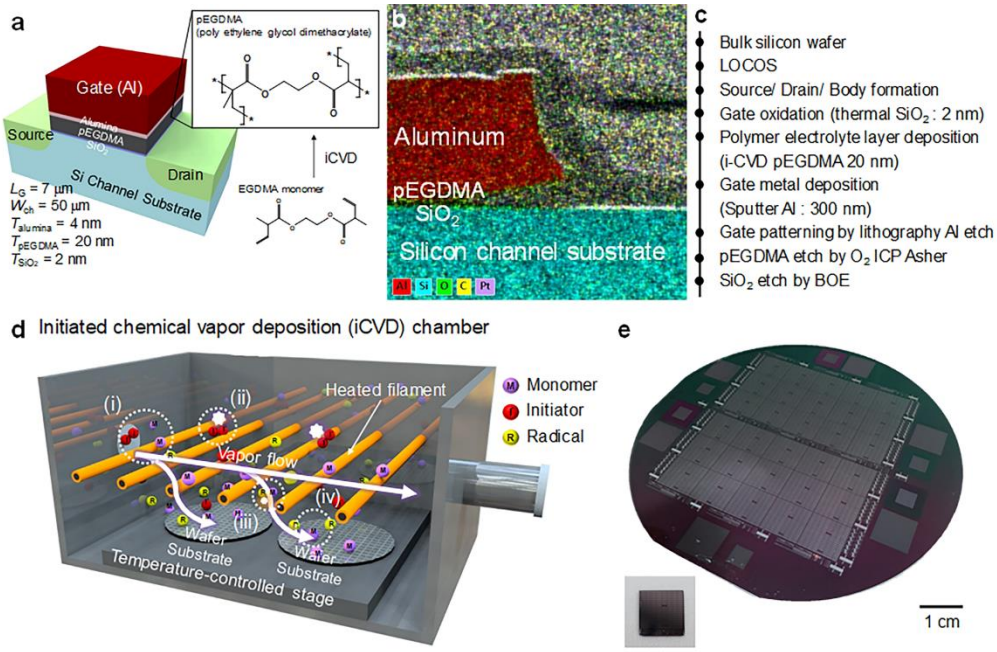

Fig. 1| Schematic and TEM image of pEGST with microfabrication procedures, iCVD process, and photographic image of a fabricated wafer. a, Schematic illustration of the pEGST and chemical structure of the EGDMA and pEGDMA. **b,** Cross-sectional TEM image of the gate stack. The iCVD method permits the conformal formation of thin polymer film across the wafer **c,** Key fabrication processes of the pEGST. **d,** Schematic of the iCVD chamber for the pEGDMA electrolyte deposition **e,** Optical photograph of a 4-inch silicon wafer and a single chip after the fabrication of the pEGST.

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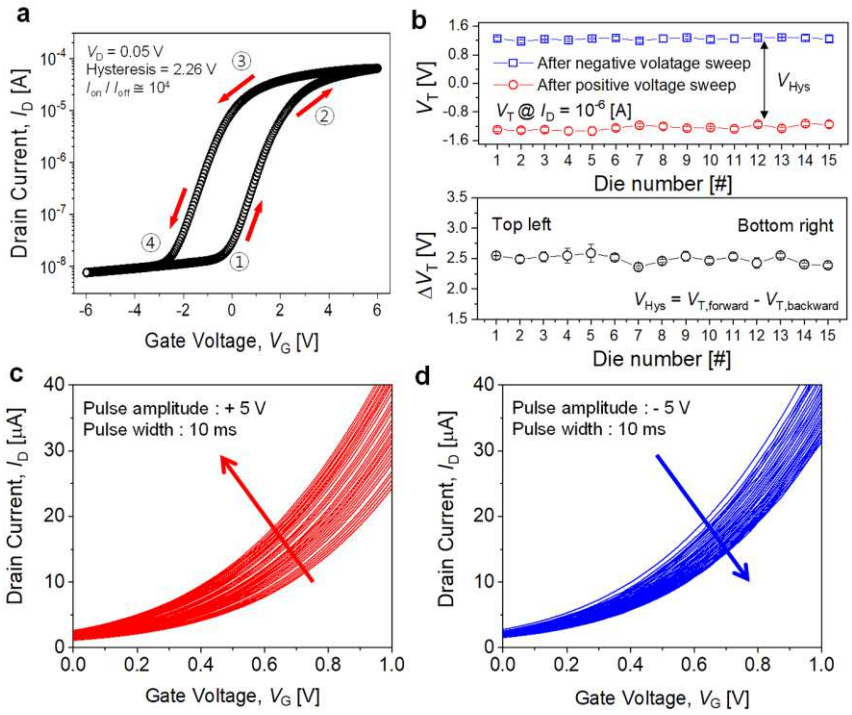

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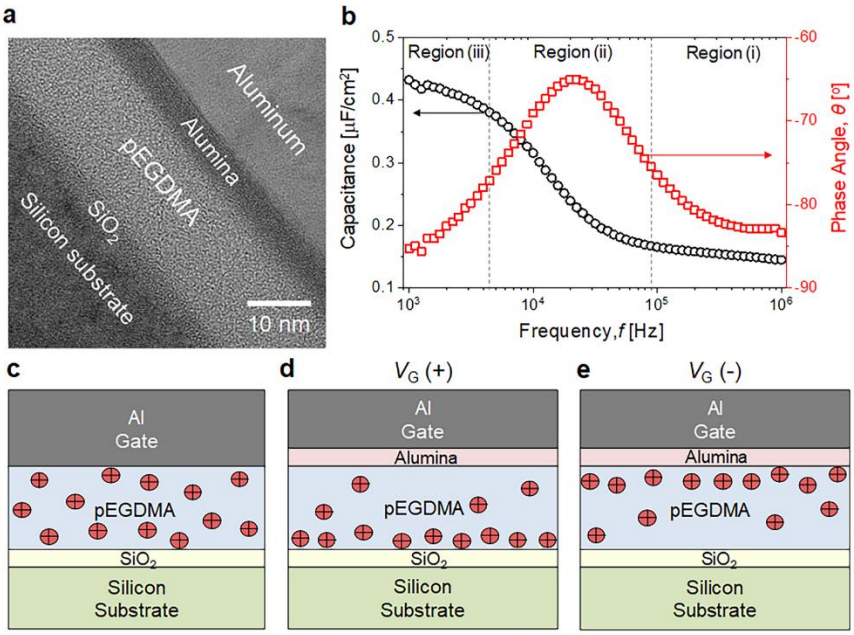

Fig. 3| TEM image of solid-state gate dielectrics and their ultra-thin electrolyte characteristics. a, TEM image of the gate dielectrics composed of SiO_2, pEGDMA and Al_2O_3. **b,** Measured capacitance per unit area and phase angle as a function of applied frequency. They are categorized as three regions: (i) dipole relaxation, (ii) ionic relaxation, and (iii) electric double layer formation. **c,** Distribution profile of H^+ (ρ_{H+}) under equilibrium without V_G. **d,** ρ_{H+} with positive V_G(+). and **e,** ρ_{H+} with negative V_G(-). The ρ_{H+} is redistributed according to the polarity of the V_G that causes hysteresis in the pEGST.

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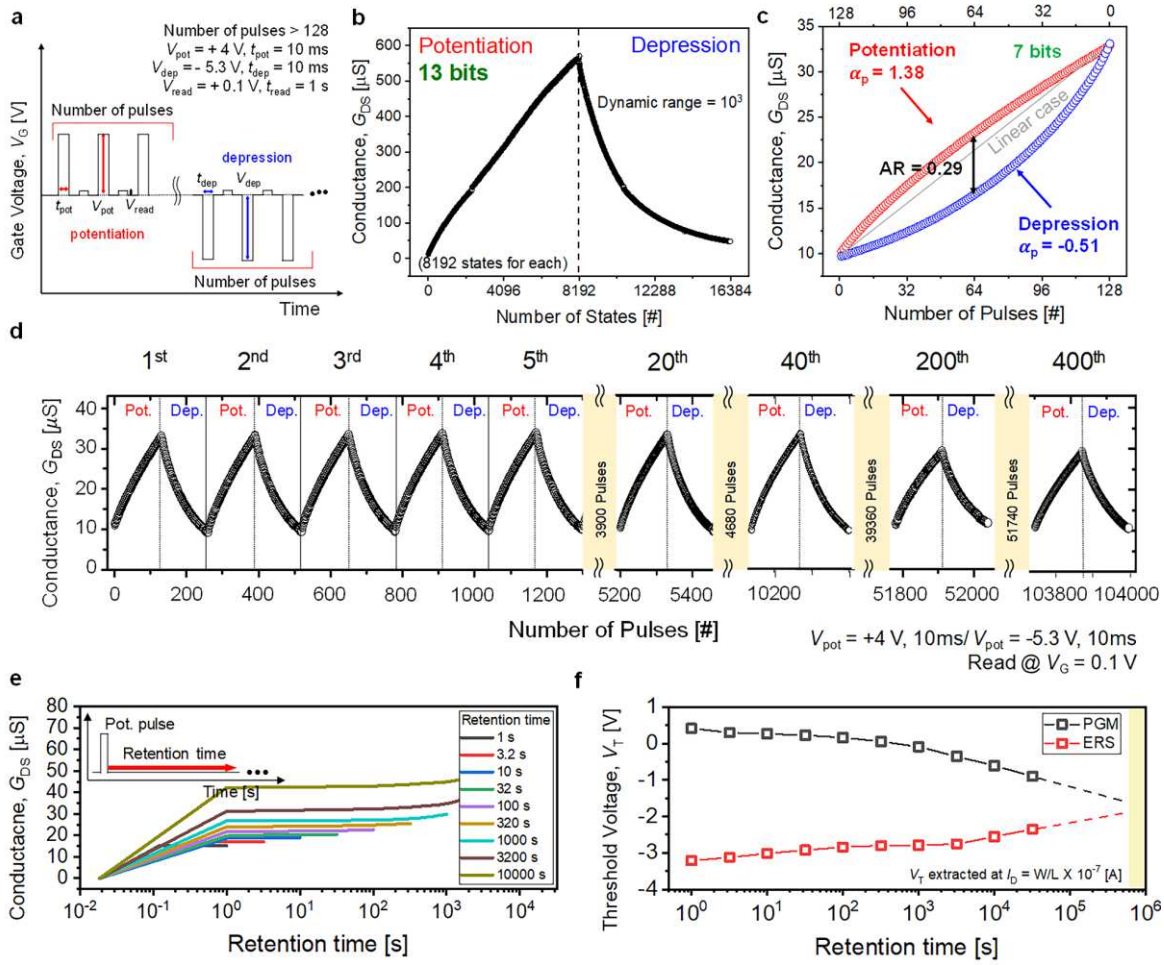

Fig. 4| Synapse characteristics for analog deep neural network of pEGST. a, Specific pulse scheme of potentiation (+4 V, 10 ms), depression (-5.3 V, 10 ms), and read operation (0.1 V). **b,** Measured multi-level channel conductance (G_{DS}) of 8,192 (13 bits) according to the number of pulses with a high current ratio of I_{ON} to I_{OFF} (>10^3). **c,** Good linearity (α_{pot} = 1.38 and α_{dep} = - 0.51) with asymmetric ratio of 0.29 in the selected range of conductance updating. **d,** Endurance characteristic of the pEGST more than 100,000 cycles. **e,** G_{DS} change by conductance retention time after applying potentiation pulses. **f,** Non-volatile retention characteristic of the pEGST by evaluation of a threshold voltage (V_T) shift after the pulse application.

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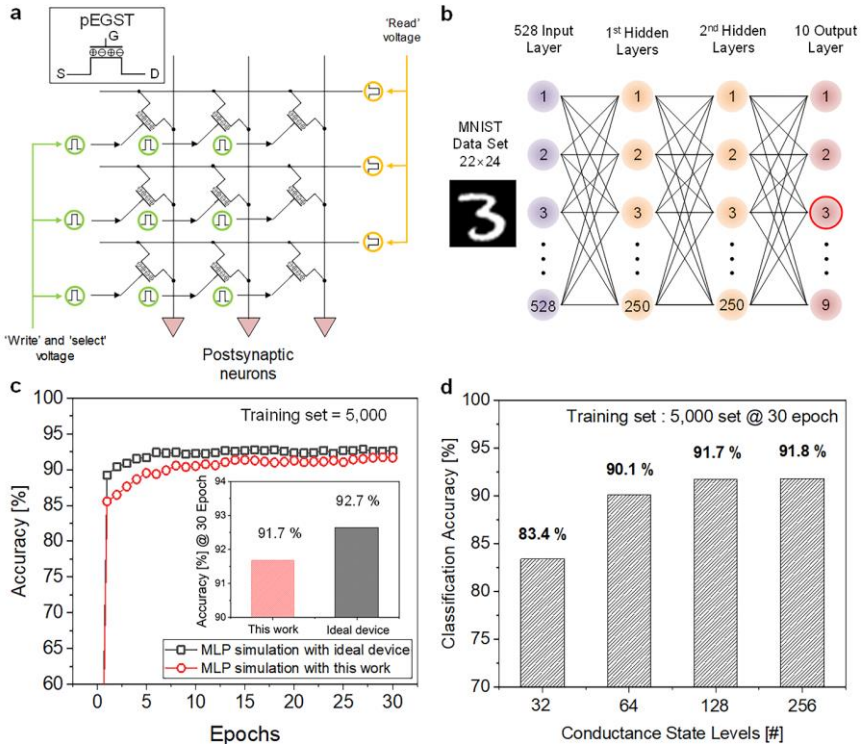

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Table. 1| Comparison of electrolyte-gated FET based artificial synaptic devices

	Electrolyte-gated FET based artificial synaptic devices						
Reference number	[24]	[25]	[26]	[27]	[28]	[29]	**This work**
Constitution	1T	1T	1T	1T	1T	1T	1T
Fabrication scale	Device-scale	Device-scale	Device-scale	Device-scale	Device-scale	Device-scale or Wafer-scale	**Wafer-scale**
CMOS compatible	No	No	No	No	No	Yes	Yes
Electrolyte	Ion gel ($LiClO_4$/PEO)	Ion gel ($LiClO_4$/PEO)	All-solid-state polymer (PEG)	Ionic liquid	Ionic liquid	Metallic oxide (WO_{3-x})	**All-solid-state polymer (PEGDMA)**
Deposition method of electrolyte	Mixture drop	Dip-coating	Spin-coating	Liquid drop	Liquid drop	Sputtering	**Initiated CVD**
Thickness of electrolyte	-	-	90 nm	-	-	80 nm	**20 nm**
Active ion	Li^+	Li^+	H^+	H^+	O^{2-}	O^{2-}	H^+
Channel	WSe_2	α-MoO_3	Single-walled CNTs	α-MoO_3	SmNiO3	W	**Silicon**
Channel formation	Mechanical exfoliation	Mechanical exfoliation	CNT solution dipping	Mechanical exfoliation	Sputtering	Sputtering	**Commercial silicon wafer**
# of bits	6 (60)	5 (50)	6 (100)	5 (50)	>7	6	**>13**
Conductance change linearity (α_{pot}/α_{dep})	1.9/0.5	2.6/-0.4	Poor	1.7/0.4	1.3/0.9	1.3/-0.3	**1.51/-0.38**
Asymmetry ratio	0.19	0.31	-	0.2	-	-	0.29
Pulse width	50 ms	10 ms	1 ms	1 ms	10 ms	10 ms	10 ms
Switching energy	~30 fJ	0.16 pJ	~7.5 pJ	500 fJ	-	-	< **20 fJ**

* 1T = Single transistor

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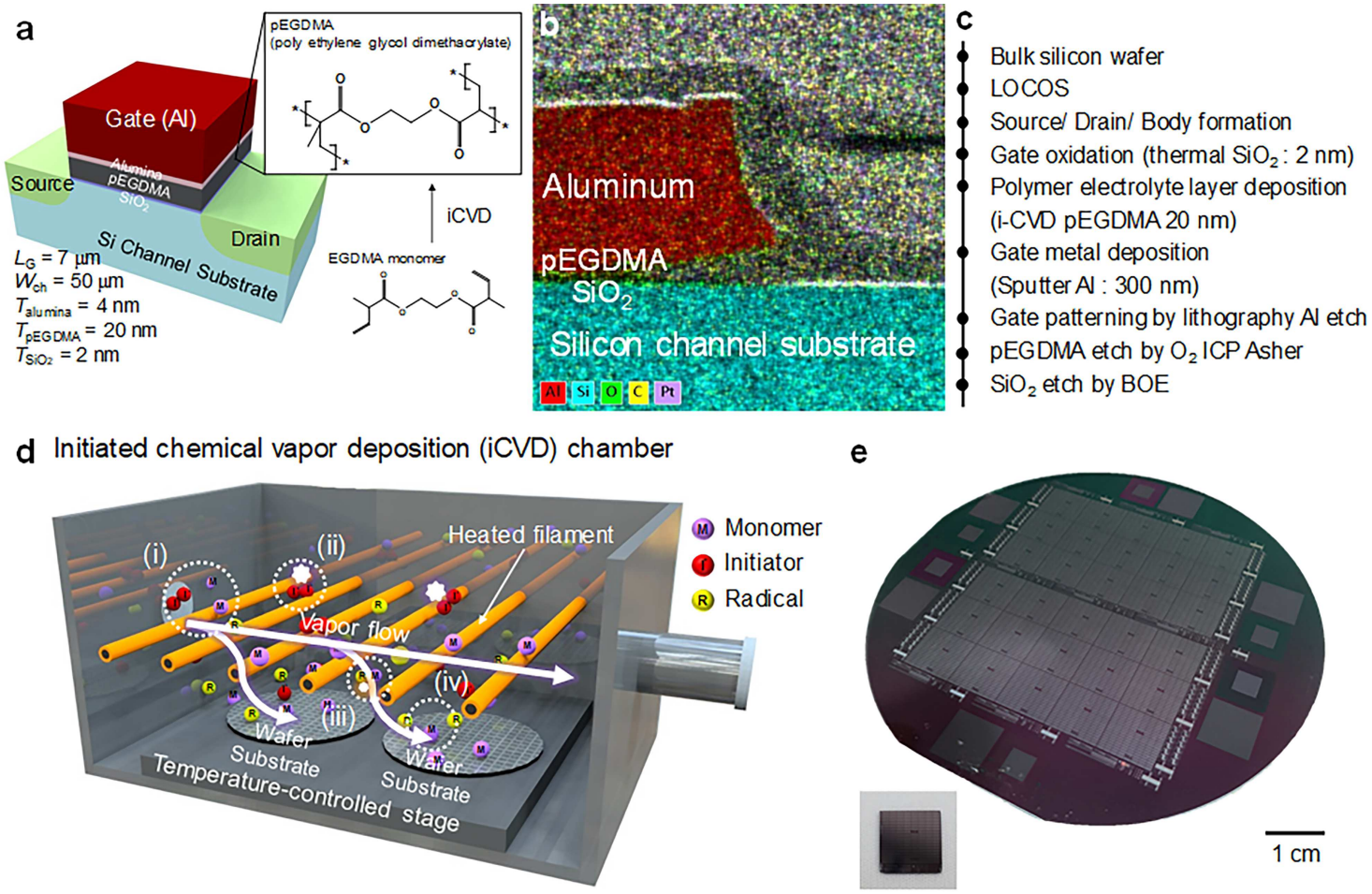
Figures



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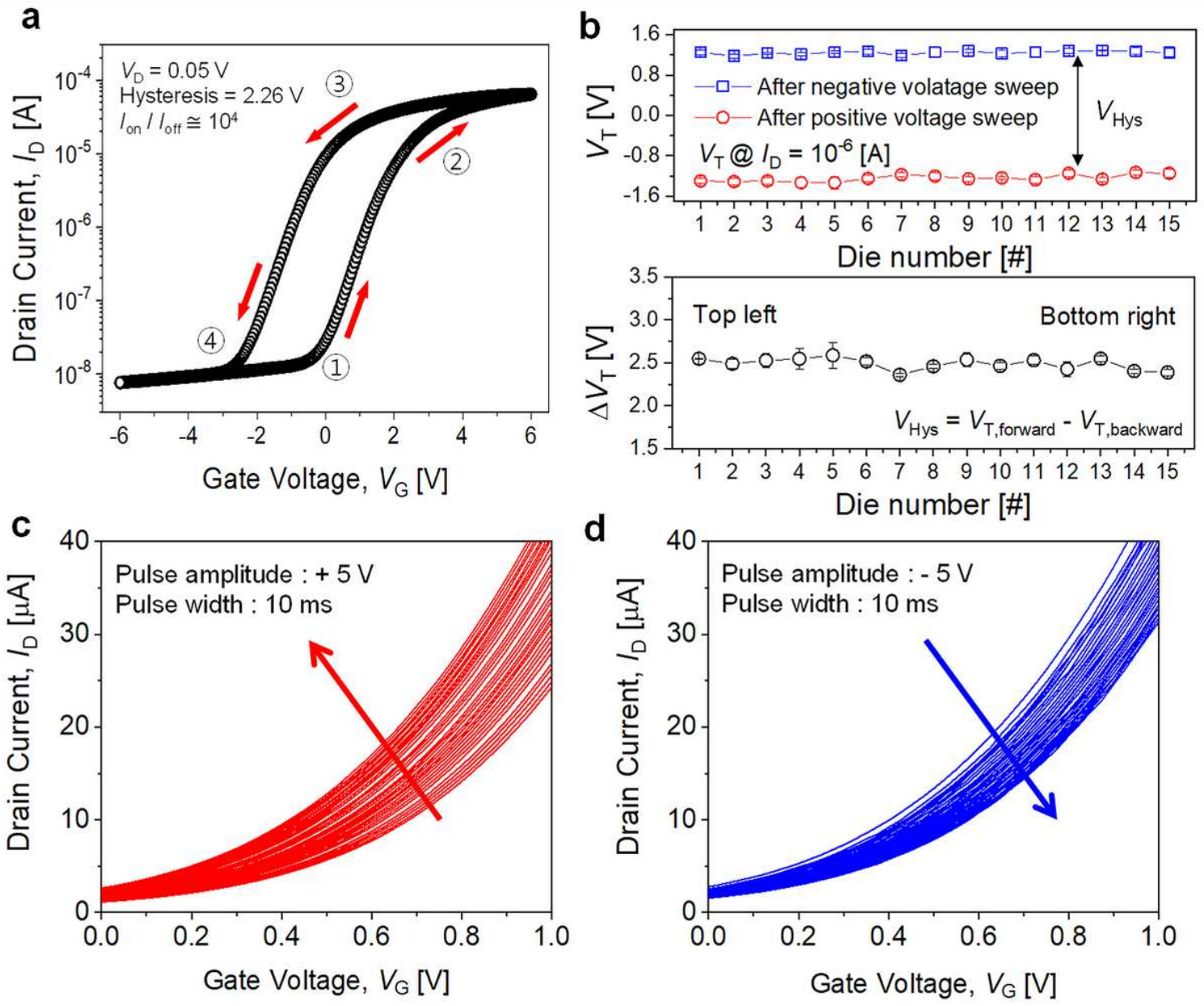

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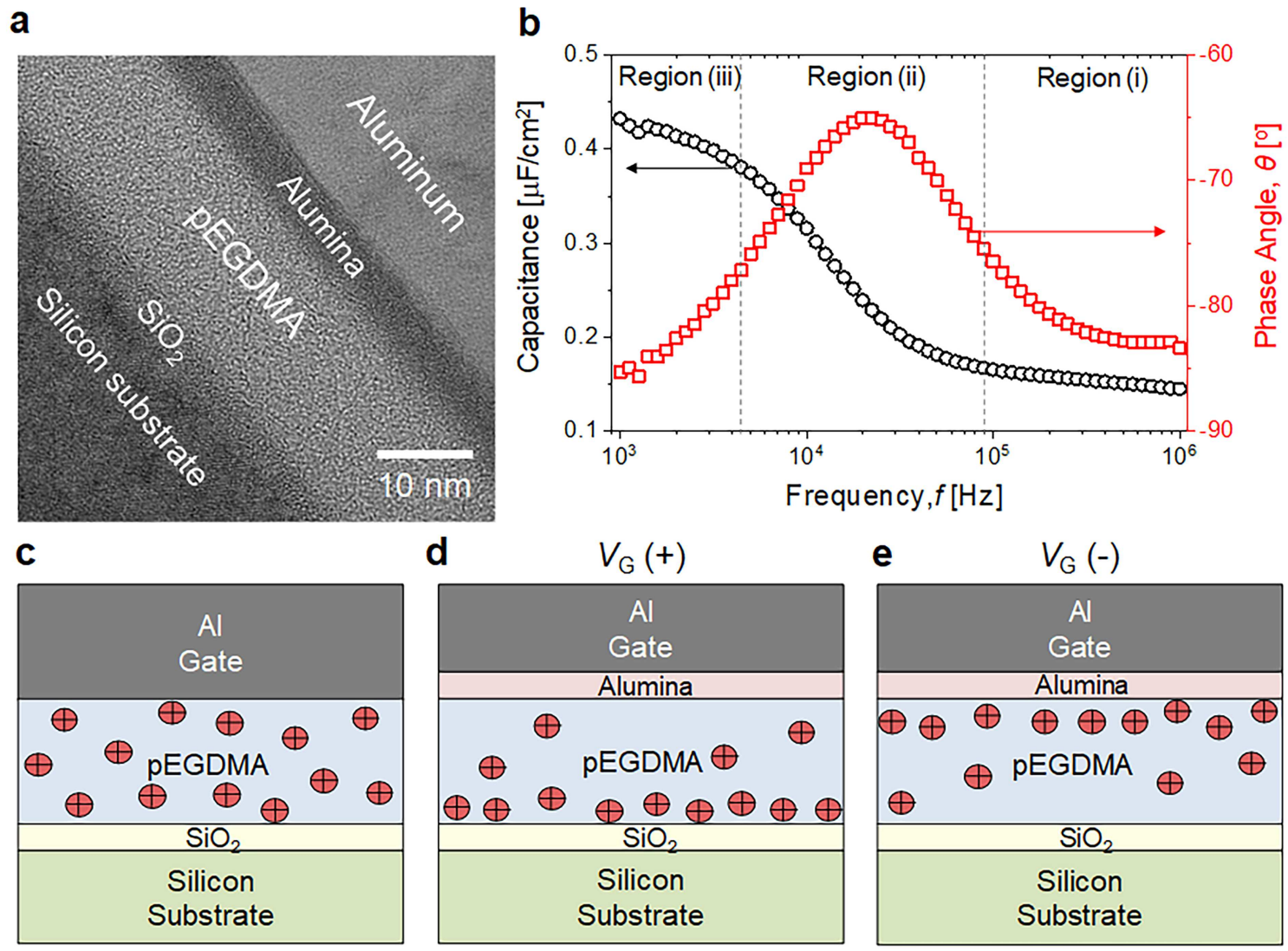

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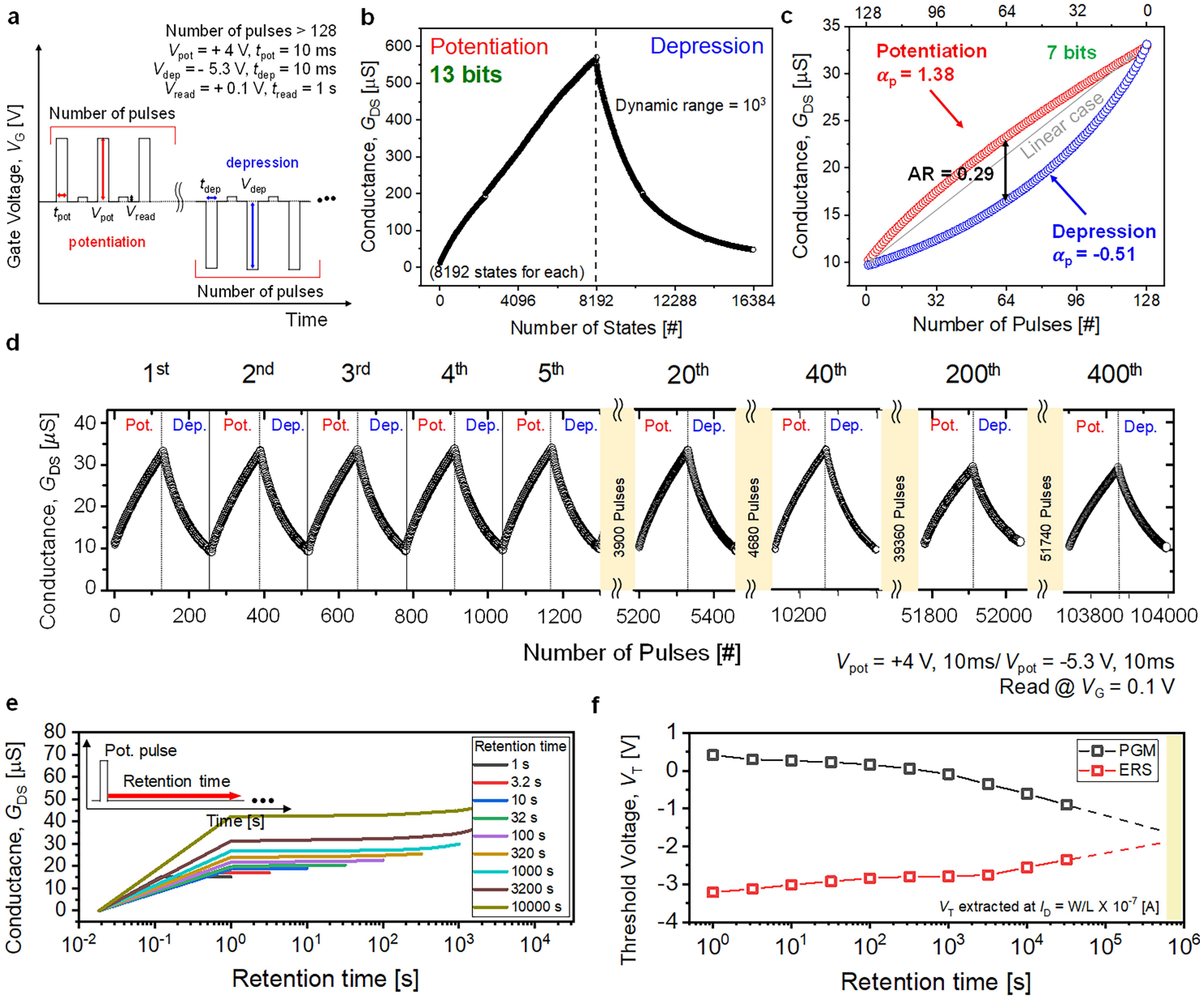

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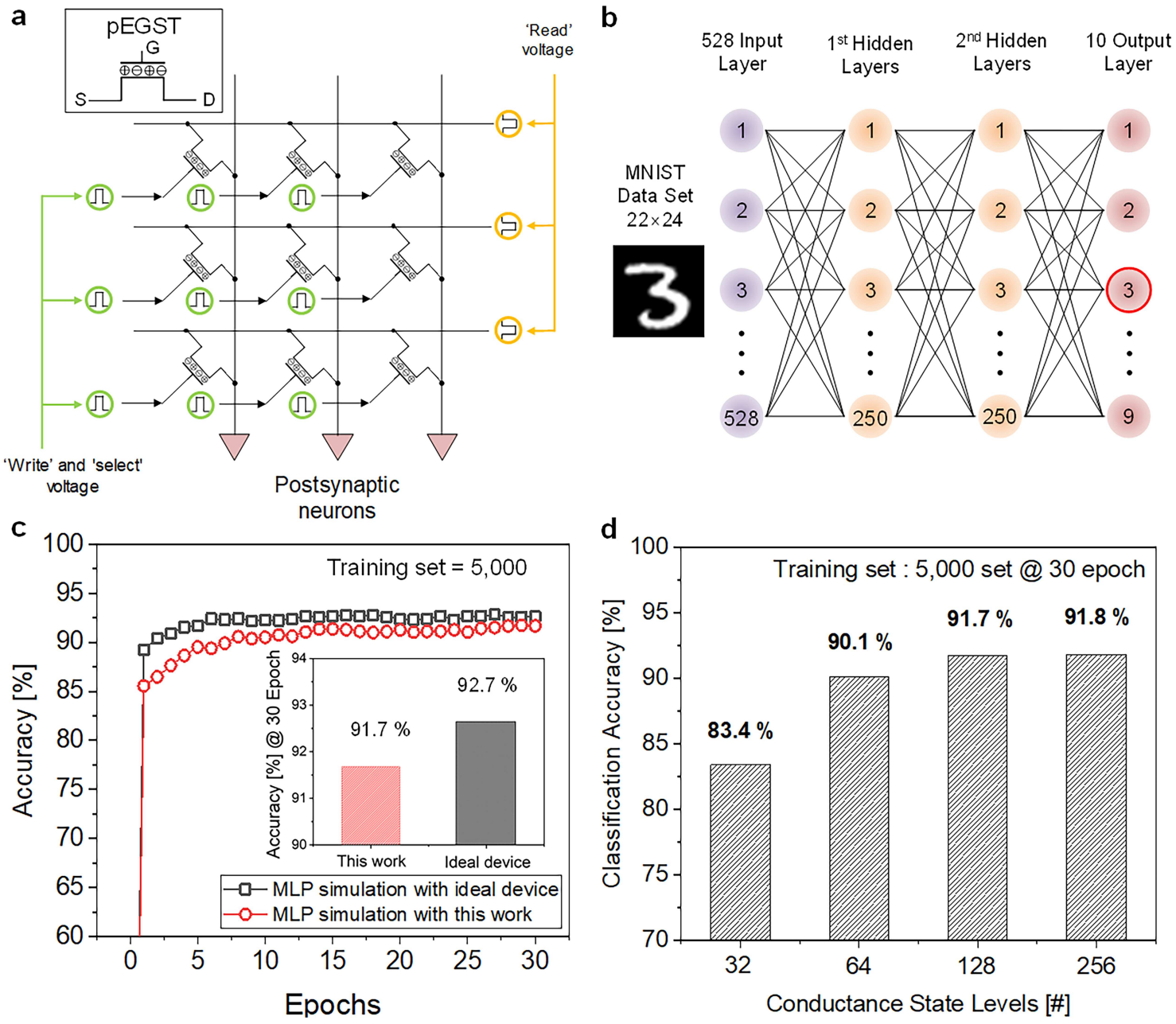

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Supplementary Files

This is a list of supplementary files associated with this preprint. Click to download.

- SupplementaryInformation.pdf

- TableI.tif