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Mohammad Abdul Alim (✉ mohammadabdulalim@cu.ac.bd)

University of Chittagong <https://orcid.org/0000-0002-3984-0176>

Anwar Jarndal

University of Sharjah

Christophe Gaquiere

University of Lille: Universite de Lille

Giovanni Crupi

University of Messina: Universita degli Studi di Messina

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Measurement-based investigation of the DC and RF transconductance for various HEMT technologies in high-and low-temperature conditions

Mohammad Abdul Alim^{1*}, Anwar Jarndal², Christophe Gaquiere³ and Giovanni Crupi⁴

¹ Department of Electrical and Electronic Engineering, University of Chittagong, Chittagong 4331, Bangladesh; mohammadabdulalim@cu.ac.bd

² Department of Electrical Engineering, University of Sharjah, Sharjah, 27272 Sharjah, UAE; ajarndal@sharjah.ac.ae

³ Institute of Electronic, Microelectronic and Nanotechnology (IEMN), The University of Lille, F-59000 Lille, France; christophe.gaquiere@iemn.univ-lille1.fr

⁴ Department of Biomedical and Dental Sciences and Morphofunctional Imaging, University of Messina, Messina 98125, Italy; crupig@unime.it

* Correspondence: mohammadabdulalim@cu.ac.bd

Abstract: The purpose of this experimental study is to evaluate quantitatively the impact of the temperature on the behavior of various high electron-mobility transistor (HEMT) technologies through the analysis of the DC and RF transconductance. The experimental data are reported for six different HEMT devices, in order to develop a comparative analysis based on various technologies, including gallium arsenide (GaAs) and gallium nitride (GaN) materials, matched and pseudomorphic HEMTs, single- (S-H) and double-heterojunction (D-H) HEMTs, and both virgin and multi-layer devices. The reported findings show that the impact of the ambient temperature on the HEMT behavior strongly depend on the tested technology and operating conditions. As a matter of fact, a higher temperature can lead to increased or degraded transconductance, depending on the device technologies and bias point. In the GaAs-based devices, an operating bias condition at which the DC and RF transconductance are temperature insensitive can be defined, owing to two-opposite temperature-dependent effects counteracting with each other.

Keywords: GaAs; GaN; HEMT; multi-bias; multi-finger, multi-layer; pHEMT; scattering-parameter measurements, temperature, transconductance

1. Introduction

The high electron-mobility transistor (HEMT) was introduced in the early 1980s [1, 2] and, over the years, has continuously evolved to meet the steadily increasing demanding requirements of the ever-expanding microwave applications. The evolution of this type of transistor has been accomplished through the use of different materials, such as gallium arsenide (GaAs) and gallium nitride (GaN), different structure designs, such as conventional lattice-matched HEMTs and pseudomorphic HEMTs (pHEMTs), multiple two-dimensional electron gas (2-DEG) channels, such as using a double heterojunction (D-H) rather than the conventional single heterojunction (S-H) in order to have two channels, different geometrical parameters, such as gate length (L_g) and width (W), and different operating conditions, such as bias point and frequency band. To improve device performance, HEMT devices are typically based on using the multi-finger layout, which consists of placing many gate fingers in parallel [3-5]. Therefore, the total gate width of multi-finger devices is given by the product of the number of fingers and their length. To develop highly integrated monolithic microwave integrated circuits (MMICs), HEMT devices might be realized using the multi-layer three-dimensional (3-D) technology [6-8].

Many studies have been devoted to the analysis of the temperature effects on the performance of the HEMT devices, focusing on both GaAs [9-18] and GaN [18-31] semiconductor technologies. The present article is aimed at an experimental investigation of the behavior of various HEMT technologies in high- and low-temperature conditions. Six different HEMT devices are studied: $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$ S-H GaAs HEMT, $0.5 \mu\text{m} \times (2 \times 75) \mu\text{m}$ S-H GaAs HEMT, $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$ virgin D-H GaAs pHEMT, $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$ multi-layer D-H GaAs pHEMT, $0.25 \mu\text{m} \times (2 \times 100) \mu\text{m}$ GaN HEMT, and $0.15 \mu\text{m} \times (4 \times 50) \mu\text{m}$ GaN HEMT. The devices under test (DUTs) are characterized in terms of both DC and scattering (S-) parameter measurements at three different ambient temperatures (T_a): -40°C , 25°C , and 150°C . The experimental data are used to investigate the effects of the temperature on the DC and RF values of the transconductance, which is a key figure of merit for determining low-noise and high-power performance of the HEMT devices that are widely used in the design of both low-noise [32-35] and high-power [35-38] amplifiers. The analysis is focused on the impact of the temperature on the DC transconductance (g_m) that is determined from the measured DC transcharacteristics, the RF transconductance that is estimated as the real part of the measured short-circuit forward transfer admittance (Y_{21}) at low low-frequency, and the intrinsic RF transconductance (g_{m0}) of the small-signal equivalent-circuit model that is extracted from the S-parameter measurements. The experiments show that the temperature effects can strongly depend on the selected technology and bias condition. It should be underlined that in the four investigated GaAs-based devices there is an operating bias point at which the transconductance is temperature insensitive, the so called transconductance zero temperature coefficient (GZTC) point [17], whereas a significant degradation of the transconductance is observed for the two investigated GaN-based HEMTs at all studied values of the gate-source voltage.

The article is organized with the following sections. Section II describes the investigated devices and the experimental characterization, Section III reports and discusses the achieved experimental findings, and Section IV draws the main conclusions.

2. Devices Under Test and Measurement Process

Figure 1 shows the photographs of the six tested on-wafer devices: $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$ S-H GaAs HEMT, $0.5 \mu\text{m} \times (2 \times 75) \mu\text{m}$ S-H GaAs HEMT, $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$ virgin D-H GaAs pHEMT, $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$ multi-layer D-H GaAs pHEMT, $0.25 \mu\text{m} \times (2 \times 100) \mu\text{m}$ GaN HEMT, and $0.15 \mu\text{m} \times (4 \times 50) \mu\text{m}$ GaN HEMT.

The two S-H devices investigated in this work are AlGaAs/GaAs HEMTs grown by molecular beam epitaxy (MBE) on a $600\text{-}\mu\text{m}$ -thick semi-insulating undoped GaAs substrate. Both devices have the same gate length of $0.5 \mu\text{m}$ but differ in the gate widths, which are $200 \mu\text{m}$ and $150 \mu\text{m}$. The interdigitated layout of both devices is based on the parallel connection of two fingers but the two devices differ in the finger length: $100 \mu\text{m}$ and $75 \mu\text{m}$. Further fabrication details of these two S-H GaAs HEMTs can be found elsewhere [39].

The two investigated D-H pHEMTs are based on using the lattice mismatched AlGaAs/InGaAs/GaAs system grown by MBE on a $600\text{-}\mu\text{m}$ -thick semi-insulating undoped GaAs substrate. The two devices have a gate length of $0.5 \mu\text{m}$ and a gate width of $200 \mu\text{m}$. The interdigitated layout consists of two fingers, each being $100\text{-}\mu\text{m}$ long. These two pHEMTs differ only because one of the two devices is made utilizing the multi-layer 3-D MMIC technology. The complete MMIC integration method consists of opening a Si_3N_4 window using buffered oxide etch (HF, hydrofluoric acid) and lithography on a wafer containing pre-fabricated pHEMTs and other passive components in a vertical plane. On top of the pre-fabricated pHEMTs, a conductor layer is placed to allow other passive components to be connected together; while providing also a track for probing the devices. Further fabrication details of these two D-H GaAs pHEMTs can be found elsewhere [40].

The two GaN HEMTs are based on an $\text{Al}_{0.253}\text{Ga}_{0.747}\text{N}/\text{GaN}$ heterostructure grown by metal organic chemical vapor deposition (MOCVD) on a $400\text{-}\mu\text{m}$ -thick SiC substrate. The two devices differ in both gate length and width: $0.25 \mu\text{m} \times (2 \times 100) \mu\text{m}$ and $0.15 \mu\text{m} \times (4 \times 50) \mu\text{m}$. The GaN devices were fabricated at the University of Lille, France and further fabrication details can be found elsewhere [41].

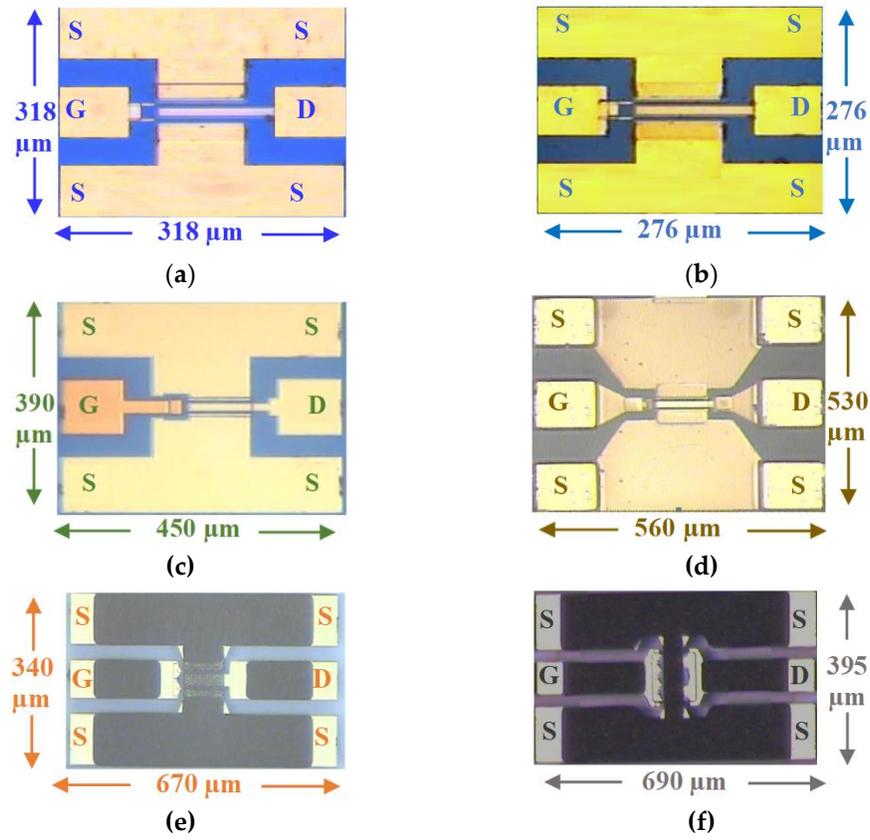


Figure 1. Photographs of the tested on-wafer devices: (a) $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$ S-H GaAs HEMT, (b) $0.5 \mu\text{m} \times (2 \times 75) \mu\text{m}$ S-H GaAs HEMT, (c) $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$ virgin D-H GaAs pHEMT, (d) $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$ multi-layer D-H GaAs pHEMT, (e) $0.25 \mu\text{m} \times (2 \times 100) \mu\text{m}$ GaN HEMT, and (f) $0.15 \mu\text{m} \times (4 \times 50) \mu\text{m}$ GaN HEMT.

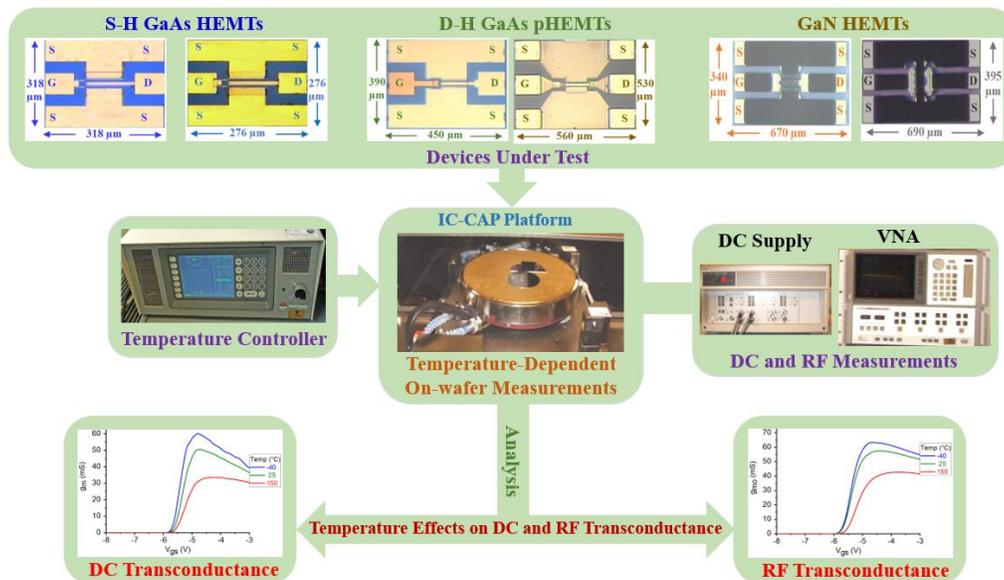


Figure 2. The flow diagram of the temperature-dependent measurement process and investigation of the temperature effects on the DC and RF transconductance for the tested on-wafer HEMT devices.

Figure 2 illustrates the flow diagram of the temperature-dependent on-wafer measurement process and the subsequent analysis of the impact of the ambient temperature on the DC and RF transconductance. The microwave experiments consist of DC and S-parameters measured from 45 MHz to 50 GHz at -40°C , 25°C , and 150°C . The analysis is performed using the DC characteristics and the S-parameters measured in the saturation region: V_{gs} was varied from -1 V to 0.8 V at $V_{ds} = 3$ V for the S-H GaAs HEMTs, V_{gs} was varied from -1.5 V to 0.6 V at $V_{ds} = 3$ V for the D-H GaAs pHEMTs, and V_{gs} was varied from -8 V to -3 V at $V_{ds} = 15$ V for the GaN HEMTs. The analysis is focused on using the experimental data for developing an accurate study of the DC and RF transconductance.

To ensure that the data were free of human error, the device parameters were measured with a thermal probe station coupled to an HP4142B DC source and an HP8510C vector network analyzer (VNA) by using Keysight's IC-CAP, which is a powerful commercial software for DC and RF semiconductor device characterization and modelling. After the sample reached uniform steady-state temperature, DC and frequency-dependent measurements were carried out at each temperature.

3. Experimental Results and Discussion

The DC transconductance at three different ambient temperatures ($T_a = -40^{\circ}\text{C}$, 25°C , and 150°C) for the studied S-H GaAs HEMTs, D-H GaAs pHEMTs, and GaN HEMTs are given in Figures 3-5, respectively. As can be observed in Figure 3, the DC transconductance of the two studied S-H GaAs HEMTs at $V_{ds} = 3$ V may increase or decrease depending on the selected value of the input voltage. This is due to two temperature-dependent effects contributing in opposite ways to the resultant behavior of the DC transconductance with increasing temperature: the degradation of the electron transport properties and the shift of the threshold voltage (V_{TH}) towards more negative values. The former effect is predominant at higher V_{gs} , whereas the latter effect is predominant at lower V_{gs} . It should be mentioned that the shift of V_{TH} can be compensated by the bias circuitry by biasing the device at fixed output voltage and current rather than at fixed output and input voltages [17]. It is worth pointing out that both devices exhibit the zero temperature coefficient point in the DC transconductance behaviour. The two devices show different values of the input voltage for the GZTC point: $V_{gs} = -0.47$ V for $W = 200$ μm and $V_{gs} = -0.35$ V for $W = 150$ μm . This result indicates that, by increasing the gate width of the tested devices, the GZTC point shifts towards a more negative value of V_{gs} . Both devices show a peak in g_m that decreases with increasing temperature and occurs at about $V_{gs} = 0.3$ V. By selecting the bias condition $V_{ds} = 3$ V and $V_{gs} = 0.3$ V, we obtain the following values of g_m for the two devices at the three different ambient temperatures: 35 mS (-40°C), 32 mS (25°C), and 26 mS (150°C) for the larger-width device (see Figure 3(a)) and 30 mS (-40°C), 28.6 mS (25°C), and 24 mS (150°C) for the narrower-width device (see Figure 3(b)). As expected, the values of g_m are higher for the device with a larger gate width.

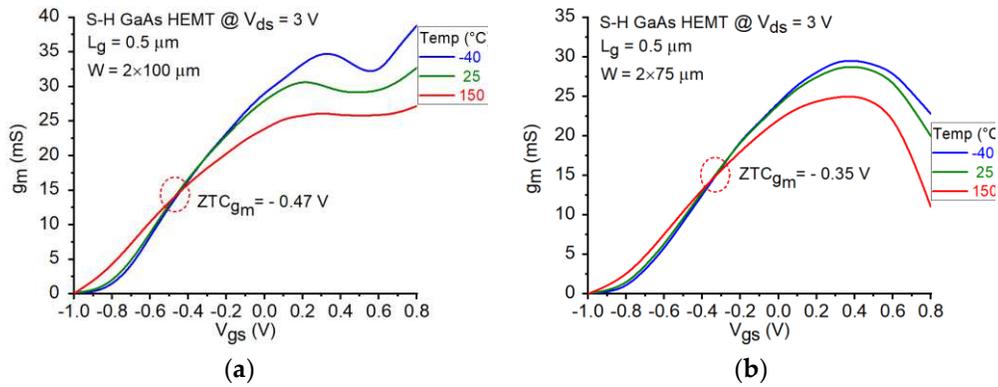


Figure 3. Behavior of the DC transconductance versus V_{gs} for the two studied S-H GaAs HEMTs at $V_{ds} = 3$ V and $T = -40^{\circ}\text{C}$, 25°C , and 150°C : (a) 0.5 $\mu\text{m} \times (2 \times 100)$ μm , (b) 0.5 $\mu\text{m} \times (2 \times 75)$ μm .

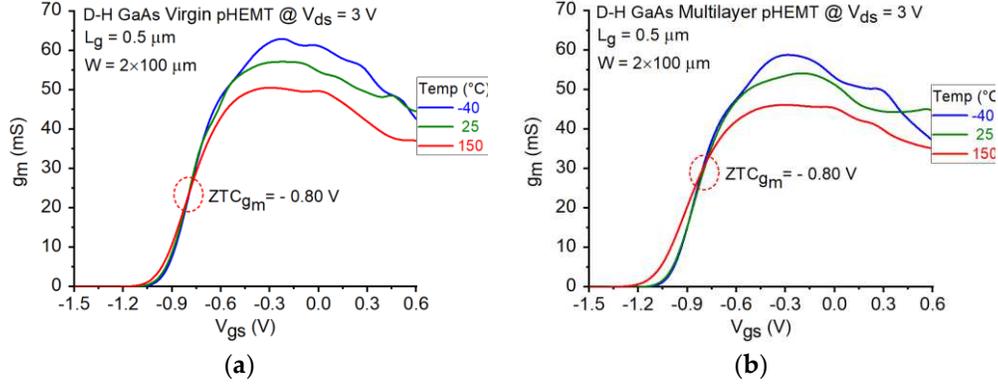


Figure 4. Behavior of the DC transconductance versus V_{gs} for the two studied D-H GaAs pHEMTs at $V_{ds} = 3$ V and $T = -40^\circ\text{C}$, 25°C , and 150°C : (a) virgin: $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$, (b) multi-layer: $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$.

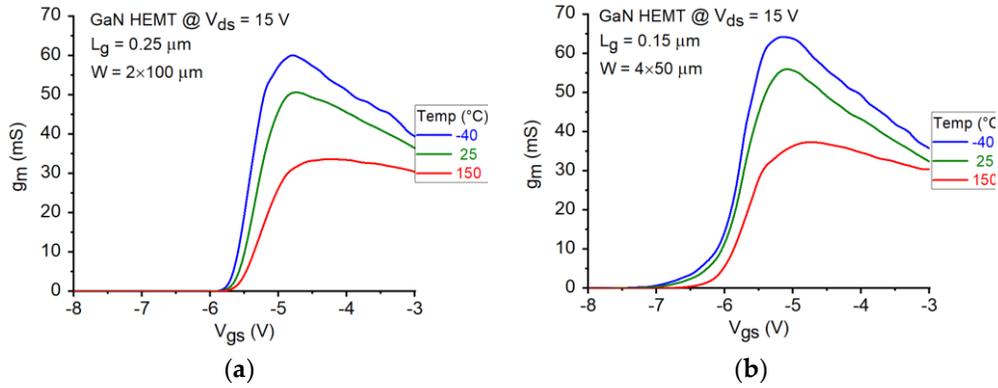


Figure 5. Behavior of the DC transconductance versus V_{gs} for the two studied GaN HEMTs at $V_{ds} = 15$ V and $T = -40^\circ\text{C}$, 25°C , and 150°C : (a) $0.25 \mu\text{m} \times (2 \times 100) \mu\text{m}$, (b) $0.15 \mu\text{m} \times (4 \times 50) \mu\text{m}$.

Similarly to what has been observed for the S-H GaAs HEMTs, the two studied D-H GaAs pHEMTs at $V_{ds} = 3$ V show a GZTC point in the DC transconductance that is achieved at $V_{gs} = -0.8$ V with $V_{ds} = 3$ V (see Figure 4). This result indicates that the GZTC point is the same for virgin and multi-layer devices and is shifted towards more negative values of V_{gs} for the D-H GaAs pHEMTs with respect to those observed for the S-H GaAs HEMTs (see Figures 3 and 4). Likewise to the S-H GaAs HEMTs, both virgin and multi-layer D-H GaAs pHEMTs show a peak in g_m that decreases with increasing temperature. This peak occurs at about $V_{gs} = -0.3$ V. By selecting the bias condition of $V_{ds} = 3$ V and $V_{gs} = -0.3$ V, we obtain the following values of g_m for the two devices at the three different ambient temperatures: 63 mS (-40°C), 57 mS (25°C), and 50 mS (150°C) for the virgin device and 59 mS (-40°C), 54 mS (25°C), and 46 mS (150°C) for the multi-layer device. This denotes that g_m is slightly reduced after using the multilayer 3-D MMIC technology [42].

Figure 5 shows that, in case of the two studied GaN HEMTs, the DC transconductance is significantly degraded with rising temperature, due to the degradation of the carrier transport characteristics that is predominant temperature-dependent effect. The two devices show a peak in g_m that decreases with increasing temperature and occurs at about $V_{gs} = -4.8$ V. By selecting the bias condition $V_{ds} = 15$ V and $V_{gs} = -4.8$ V, we obtain the following values of g_m for the two devices at the three different ambient temperatures: 59 mS (-40°C), 51 mS (25°C), and 33 mS (150°C) for the longer device and 61 mS (-40°C), 53 mS (25°C), and 38 mS (150°C) for the shorter device. As expected, the values of g_m are higher for the device with a shorter gate length.

At frequencies low enough to neglect the reactive components, Y_{21} can be defined in terms of the equivalent-circuit parameters (ECPs) (see Fig. 6) as follows [43]:

$$Y_{21} = \frac{g_{mo}}{1 + g_{mo}R_s + \frac{R_s + R_d}{R_{ds}}} \quad (1)$$

This equation shows that the RF transconductance can be estimated as the low-frequency Y_{21} , which should be purely real and correspond to the DC transconductance when the low-frequency dispersion effects are negligible. To develop the present analysis, we consider only the real part of the measured Y_{21} that is evaluated at 45 MHz, which is the lowest frequency point of our measurements.

Figures 7-9 reports the impact of the temperature on the performance of the six studied devices by focusing on $\text{Re}(Y_{21})$ at 45 MHz. Similarly to what has been observed for the DC transconductance, the low-frequency $\text{Re}(Y_{21})$ also exhibits the GZTC point in case of the GaAs HEMTs and pHEMTs (see Figures 7 and 8), whereas the low-frequency $\text{Re}(Y_{21})$ gets degraded for all V_{gs} values by increasing the temperature in case of the GaN HEMTs (see Figure 9).

The equivalent-circuit model in Figure 6 was used to represent the measured S-parameters of the six studied devices. The ECPs were obtained using the well-known "cold" pinch-off methods, which has been widely and successfully applied to HEMT technology in recent years [44-50]. The intrinsic RF transconductance values are then extracted at the "hot" bias conditions of interest. The achieved values of the intrinsic RF transconductance for the six studied devices are presented in Figures 10-12. Similarly to what has been observed for the DC and RF transconductance (see Figures 3-5 and 7-9), the intrinsic RF transconductance also exhibits the GZTC point in case of the GaAs HEMTs and pHEMTs (see Figures 10 and 11), whereas the intrinsic RF g_m gets degraded for all V_{gs} values by increasing the temperature in case of the GaN HEMTs (see Figure 12). Table 1 shows that, by considering a fixed bias point, the intrinsic RF g_m for the studied devices is found to be greater than the $\text{Re}(Y_{21})$ at 45 MHz and g_{mo} , which is due to the impact of the extrinsic resistances (see equation (1)).

Table II reports the values of V_{gsGZTC} , which is the gate-source voltage at which the transconductance is temperature insensitive, for the four studied S-H GaAs HEMTs and D-H GaAs pHEMTs at $V_{ds} = 3$ V. The achieved values of V_{gsGZTC} are roughly the same by using g_m , $\text{Re}(Y_{21})$ at 45 MHz, and g_{mo} .

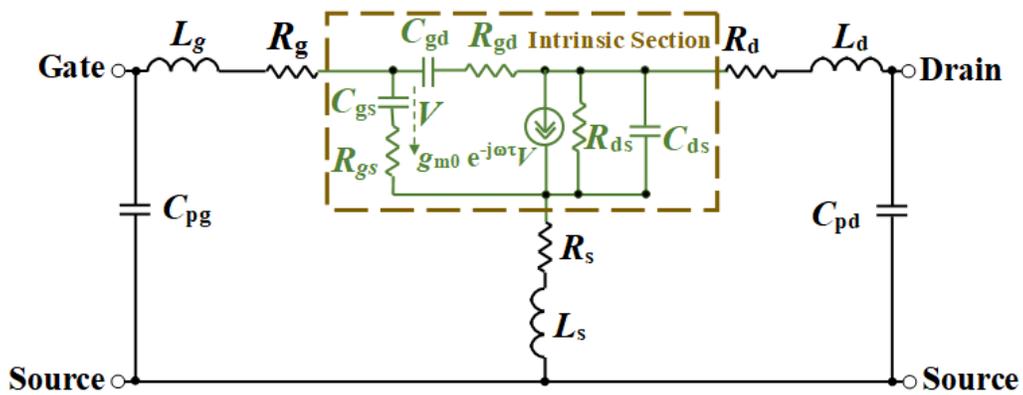


Figure 6. Equivalent-circuit model for the studied HEMTs.

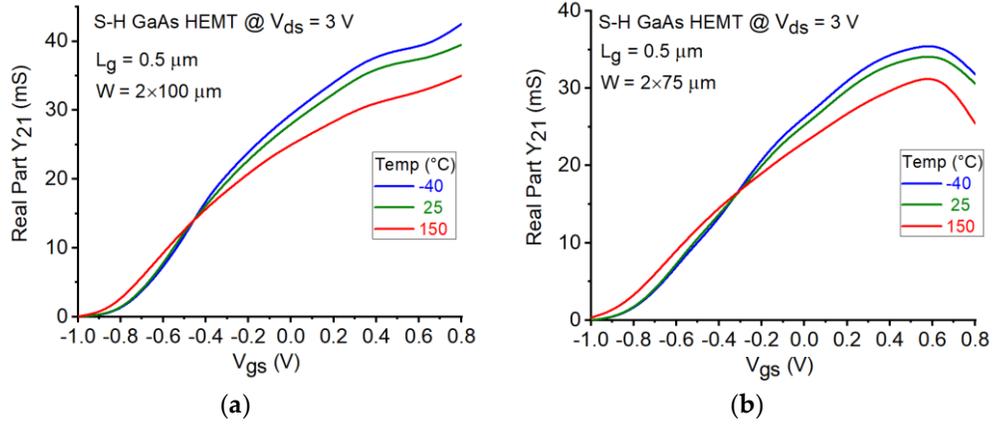


Figure 7. Behavior of the real part of Y_{21} at 45 MHz versus V_{gs} for the two studied S-H GaAs HEMTs at $V_{ds} = 3$ V and $T = -40^{\circ}\text{C}$, 25°C , and 150°C : (a) $0.5\ \mu\text{m} \times (2 \times 100)\ \mu\text{m}$, (b) $0.5\ \mu\text{m} \times (2 \times 75)\ \mu\text{m}$.

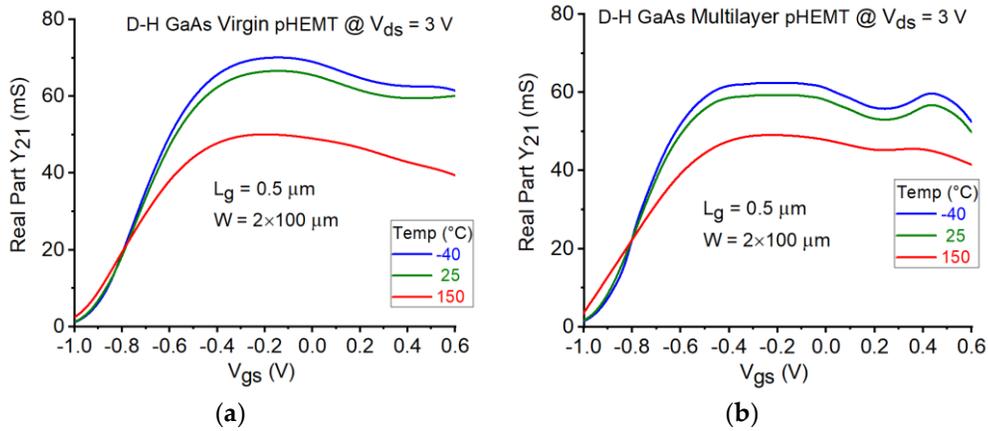


Figure 8. Behavior of the real part of Y_{21} at 45 MHz versus V_{gs} for the two studied D-H GaAs pHEMTs at $V_{ds} = 3$ V and $T = -40^{\circ}\text{C}$, 25°C , and 150°C : (a) Virgin: $0.5\ \mu\text{m} \times (2 \times 100)\ \mu\text{m}$, (b) multi-layer: $0.5\ \mu\text{m} \times (2 \times 100)\ \mu\text{m}$.

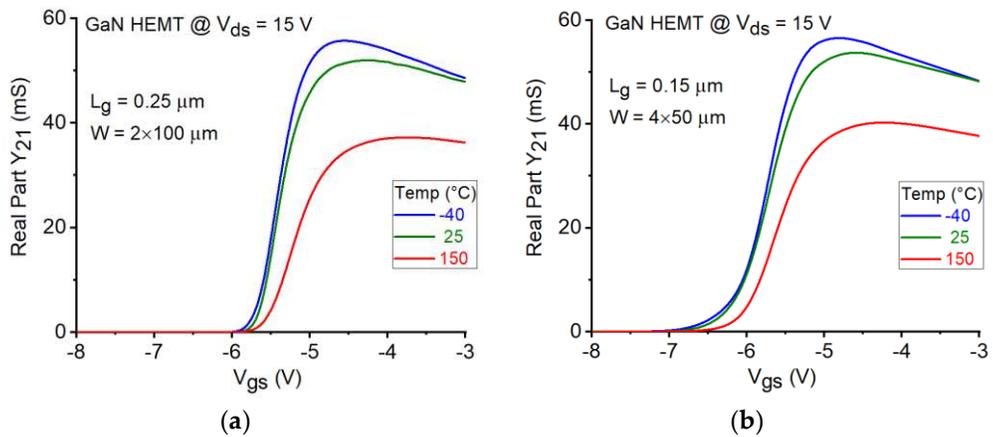


Figure 9. Behavior of the real part of Y_{21} at 45 MHz versus V_{gs} for the two studied GaN HEMTs at $V_{ds} = 15$ V and $T = -40^{\circ}\text{C}$, 25°C , and 150°C : (a) $0.25\ \mu\text{m} \times (2 \times 100)\ \mu\text{m}$, (b) $0.15\ \mu\text{m} \times (4 \times 50)\ \mu\text{m}$.

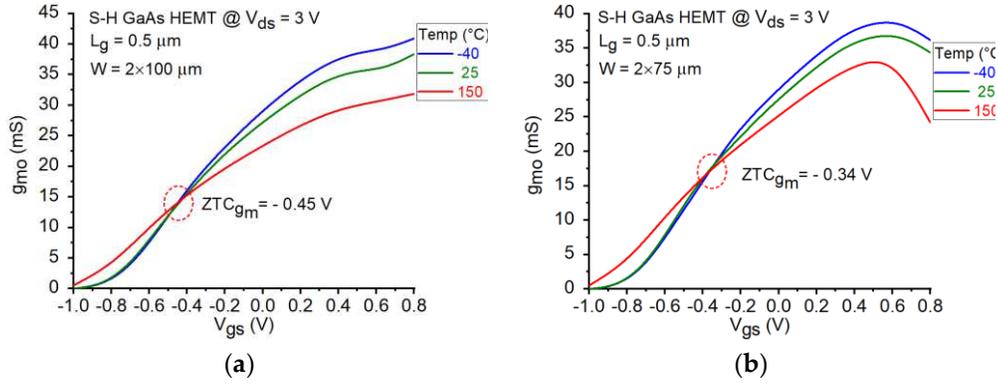


Figure 10. Behavior of the intrinsic RF transconductance versus V_{gs} for the two studied S-H GaAs HEMTs at $V_{ds} = 3$ V and $T = -40^\circ\text{C}$, 25°C , and 150°C : (a) $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$, (b) $0.5 \mu\text{m} \times (2 \times 75) \mu\text{m}$.

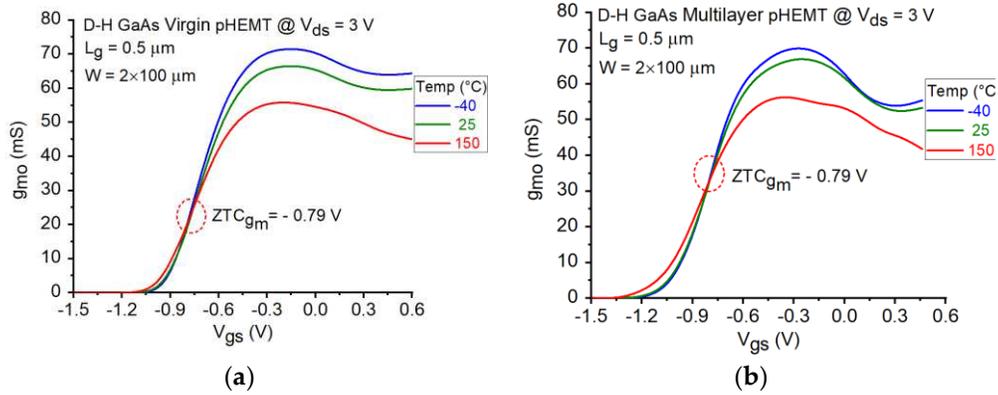


Figure 11. Behavior of the intrinsic RF transconductance versus V_{gs} for the two studied D-H GaAs pHEMTs at $V_{ds} = 3$ V versus V_{gs} under different temperature conditions: (a) Virgin: $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$, (b) multi-layer: $0.5 \mu\text{m} \times (2 \times 100) \mu\text{m}$.

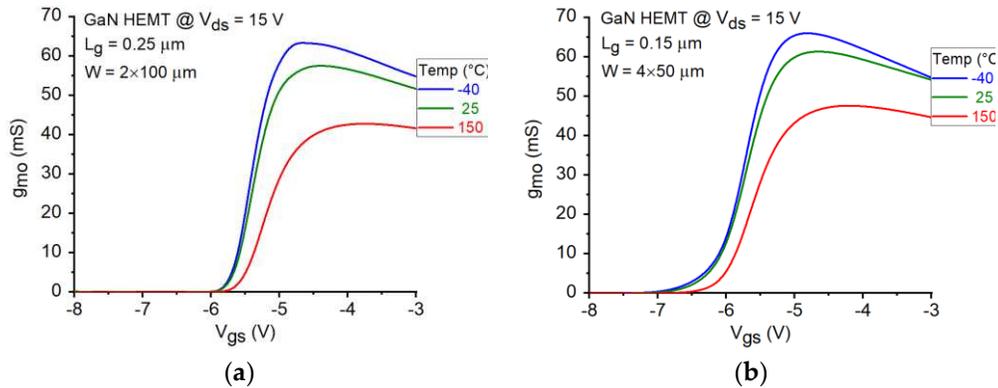


Figure 12. Behavior of the intrinsic RF transconductance versus V_{gs} for the two studied GaN HEMTs at $V_{ds} = 15$ V and $T = -40^\circ\text{C}$, 25°C , and 150°C : (a) $0.25 \mu\text{m} \times (2 \times 100) \mu\text{m}$, (b) $0.15 \mu\text{m} \times (4 \times 50) \mu\text{m}$.

Table 1. DC and RF transconductance for the six studied HEMTs at a selected bias condition.

HEMTs	T _a (°C)	g _m (mS)	Re(Y ₂₁) (mS) @ 45 MHz	g _{mo} (mS)
S-H GaAs HEMT	-40	35	36	38
0.5× 200 μm ²	25	32	34	35
@ V _{ds} = 3 V and V _{gs} = 0.3 V	-150	26	29	30
S-H GaAs HEMT	-40	30	32	34
0.5× 150 μm ²	25	28.6	30	32
@ V _{ds} = 3 V and V _{gs} = 0.3 V	-150	24	26	29
Virgin D-H GaAs pHEMT	-40	63	68	70
0.5× 200 μm ²	25	57	61	63
@ V _{ds} = 3 V and V _{gs} = -0.3 V	-150	50	51	53
Multi-layer D-H GaAs pHEMT	-40	59	62	65
0.5× 200 μm ²	25	54	59	61
@ V _{ds} = 3 V and V _{gs} = -0.3 V	-150	46	49	51
GaN HEMT	-40	59	55	64
0.25× 200 μm ²	25	51	50	56
@ V _{ds} = 15 V and V _{gs} = -4.8 V	-150	33	31	37
GaN HEMT	-40	61	57	68
0.15× 200 μm ²	25	53	54	61
@ V _{ds} = 15 V and V _{gs} = -4.8 V	-150	38	39	44

Table 2. Values of the gate-source voltage at which the transconductance is temperature insensitive for the four studied S-H GaAs HEMTs and D-H GaAs pHEMTs at a drain-source voltage of 3 V.

HEMTs	V _{gsGZTC} (V)	V _{gsGZTC} (V)	V _{gsGZTC} (V)
	based on g _m	based on Re(Y ₂₁) @ 45 MHz	based on g _{mo}
S-H GaAs HEMT	-0.47	-0.45	-0.45
0.5× 200 μm ²			
S-H GaAs HEMT	-0.35	-0.34	-0.34
0.5× 150 μm ²			
Virgin D-H GaAs pHEMT	-0.80	-0.79	-0.79
0.5× 200 μm ²			
Multi-layer D-H GaAs pHEMT	-0.80	0.79	0.79
0.5× 200 μm ²			

4. Conclusion

To gain a comprehensive overview of the temperature effects on the HEMT performance, an experimental study was developed focusing on the behavior of both DC and RF transconductance for various HEMT devices in high- and low-temperature conditions. It was shown that the temperature effects can strongly depend on the chosen device technology and selected bias condition. However, in GaAs-based devices, an operating bias condition at which the DC and RF transconductance are temperature insensitive can be defined, as a result of two-opposite temperature-dependent effects

counteracting with each other: the degradation of the electron transport properties and the shift of the threshold voltage towards more negative values. On the other hand, the GaN-based devices show a significant reduction of both DC and RF transconductance at higher temperatures for all studied values of the gate-source voltage, as a result of the degradation of the electron transport properties that is the predominant temperature-dependent effect.

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