The Role of Dual-Stacked Oxide Semiconductor in High Performance Thin Film Transistors

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Abstract

Oxide thin film transistors (TFTs) have attracted much attention because they can be applied to flexible and large-scaled switching devices. Especially, Oxide semiconductors (OSs) have been developed as active layers of TFTs and, among them, Indium-Gallium-Zinc-Oxide (IGZO) is actively used in the OLED display field. However, IGZO TFTs are limited by low field-effect mobility, which critically affects display resolution and power consumption, despite superior off-state properties. Herein, we prevailed new working mechanisms in dual-stacked OS and, based on this, developed dual-stacked OS-based TFT with high field-effect mobility ($\sim 80 \text{ cm}^2/\text{V}\cdot\text{s}$), ideal threshold voltage near 0 V, high on-off current ratio ($>10^9$), and good stability at bias stress. In dual-stacked OS, induced areas are formed at interface by band-offset: band-offset-induced area (BOIA) and BOIA-induced area (BIA). They connect gate-bias-induced area (GBIA) and electrode-bias-induced area (EBIA), resulting in high current flow. Such mechanism will provide new design rules for high performance OS-based TFTs.

Introduction

With the recent emphasis on the importance of the fourth industrial revolution, new material technologies are emerging to commercialize and apply for various electronic components such as next-generation displays, memory, energy storage devices, and power generators, which go beyond the limits of Si-based materials, especially 'Oxide electronics' based on oxide semiconductor (OS) materials^{1,2}. Based on these points, the potential for an application consisting of OSs is significant in the future. An OS has an energy band gap of approximately less than 3 eV and the voltage injection that can have energy above the energy band gap is essential to move electrons, resulting in electrical current flow³. Therefore, the OSs are widely used as switching devices as the current can be controlled by voltage regulation. OS-based thin film transistors (TFTs) are transparent and can be fabricated at low temperature, so it is possible to process on transparent and flexible substrates such as plastic and polyimide⁴⁻⁸. This is suitable for display devices that are changing transparently and flexibly. Because OSs are low cost and transparent, they are in spotlight as an active layer of TFTs, and the researches are ongoing^{1,9}. In addition, OS-based TFTs, which use OS as an active layer, are suitable for applications such as virtual reality (VR) and augmented reality (AR)^{10,11}. And with these transparent property and low cost as well as high electrical performances, OS-based TFTs will be widely applied to many wearable devices¹².

Indium-gallium-zinc-oxide (IGZO) is widely used as an active layer of TFTs because of low leakage current in the off state, and an ideal threshold voltage formed near 0 V^{1,2,13}. However, due to low field-effect mobility ($\sim 10 \text{ cm}^2/\text{V}\cdot\text{s}$), which causes excessive power consumption and limits high resolution display, it is difficult to apply to next-generation displays, so more improvements are needed. Although there have been many studies such as various types of doping¹⁴⁻¹⁷, material changes¹⁸⁻²⁵, and OS films reinforcement²⁶⁻²⁹, there have been limitation to a single OS-based TFT due to low field-effect mobility. To address this issue, dual-stacked OS-based TFTs have been recently considered potential candidates to improve field-effect mobility, and researches showing a relatively high field-effect mobility (30~50

$\text{cm}^2/\text{V}\cdot\text{s}$) have been reported³⁰⁻³⁵. However, they still have a considerably low on-off current ratio ($<10^6$), an undesirable threshold voltage far from 0 V, or an unstable reliability caused by bias stress. When the threshold voltage is formed far from 0 V and on-off ratio is low, power consumption occurs even at off state, which can cause reliability problems such as degradation of the display devices. It is very challenging to improve these things while maintaining high field-effect mobility. Above all, the main bottleneck for applying OS-based dual-stacked TFTs to actual applications is the lack of a comprehensive understanding of the conduction mechanism, which hinders the actual application in display industry.

Here, we prevailed newly the exact role of dual-stacked OSs, consisting of the channel layer at the bottom and the buffer layer at the top in TFTs, and demonstrated the high performance dual-stacked OS-based TFTs with very high field-effect mobility, ideal threshold voltage near 0 V, high on-off current ratio, and stable reliability at bias stress. InO_x with high field-effect mobility was used as a channel layer, and IGZO with excellent off-state properties was used as a buffer layer. In more detail, InO_x stacked on top of the gate insulator, serves to supply the accumulated electrons to the source-drain electrodes in on-state when gate bias is applied, and IGZO stacked under source-drain electrodes serves to reduce leakage current in off-state and cause the threshold voltage to be formed near 0 V. The key point in this mechanism is 'induced area'. Because of the connection between such induced areas, the electrical performances were significantly improved for very high field-effect-mobility ($\sim 80 \text{ cm}^2/\text{V}\cdot\text{s}$), ideal threshold voltage near 0 V, low subthreshold swing (SS) value ($<0.5 \text{ V}\cdot\text{dec}^{-1}$), and very high current on-off ratio ($>10^9$). In addition, the stabilities of the dual-stacked OS-based TFTs were maintained under positive bias stress (PBS) and negative bias stress (NBS). As a result, the dual-stacked OS-based TFTs had little threshold voltage shift of 2.62 V and 1.72 V respectively on PBS and NBS, similar to the results in a single IGZO TFTs.

Above all, we proposed the novel working conduction mechanism and the exact role of the dual-stacked OSs in TFTs with the concept of induced area. When bias is applied or OSs are connected, an induced area is always formed, which can explain the conduction mechanism through the connection between these induced areas. Based on interactions between these induced areas, the conduction mechanism of dual-stacked OS-based TFTs has been newly developed. As the process of the current conduction can be understood in detail through this mechanism, dual-stacked OS-based TFTs with remarkably improved properties can be implemented, and furthermore, they show great potential for the next-generation display industry.

Results

Fig. 1a shows the schematic of dual-stacked OS-based TFT consisting of a channel layer at the bottom and a buffer layer at the top. InO_x was used as the channel layer to enhance the field-effect mobility and IGZO was used as the buffer layer to ensure ideal threshold voltage near to 0 V, high on-off ratio, low off current level, and stability at bias stress. It is essential to design the optimal configuration,

which took the advantage of both InO_x and IGZO, based on understanding the exact mechanism. These OSs were deposited at room temperature by radiofrequency (RF) sputter. Subsequently, rapid thermal annealing (RTA) was carried out immediately after deposition of OSs. This RTA method is the most effective compared to other annealing methods such as annealing in tube furnace and annealing in glove box, and detailed results are shown in Supplementary Fig. 1 and Supplementary Table 1.

The TEM image of the TFT device with dual-stacked OS is shown in Fig. 1b. In this image, it shows that InO_x has a thickness of 9.86 nm and IGZO has a thickness of 30.24 nm, showing that it is similar to the optimal setting thickness of 10 nm and 30 nm, respectively. Also, atomic components were extracted using high-resolution transmission electron microscopy (HR-TEM) to ensure that each layer was properly formed (Fig. 1c). As expected, through the distribution of each atomic component, such as In, Ga, Zn and O, it confirms that InO_x and IGZO were well formed.

Electrical Characteristics of TFTs

Fig. 2a shows the transfer curves of three kinds of OS-based TFTs. The red one and the blue one are single OS-based TFTs consisting of InO_x and IGZO, respectively. The thickness of InO_x and IGZO are 10 nm and 30 nm, respectively. And the pink one is dual-stacked OS-based TFT consisting of InO_x and IGZO. The thickness of InO_x and IGZO in dual-stacked OS is 10 nm and 30 nm, respectively, the same thickness as in a single InO_x TFT and IGZO TFT. Their optimized thicknesses were determined based on the performance according to the thickness of a single InO_x layer and a single IGZO layer, respectively. More details can be identified in Supplementary Fig. 2, Supplementary Table 2, and Supplementary Table 3.

For a single InO_x TFT, relatively high on-state current level can provide excellent field-effect mobility^{31,36,37}. However, the off-state current level is also high, which can cause excessive power consumption and degradation of switching signals in circuits. In addition, a single InO_x TFT represents a negatively shift turn-on voltage far from 0 V, causing additional power consumption. Given all of this, it is difficult to utilize the single InO_x TFTs in display industries that need accurate switching system. For a single IGZO TFT, it shows low off-state current level of 1 pA (10^{-12} A) and turn-on voltage near 0 V. They play a major role in preventing leakage current^{1,4,7,8}. However, it is difficult to apply the single IGZO TFTs to displays that require high resolution due to their limited field-effect mobility to $\sim 10 \text{ cm}^2/\text{V}\cdot\text{s}$. In these critical reasons, OS-based TFTs with both the advantages of InO_x and IGZO are required, and can be realized through the dual-stacked OS-based TFT that uses InO_x and IGZO as the channel layer at the bottom and buffer layer at the top, respectively. For the dual-stacked TFT, it represents low off-state current level and ideal turn-on voltage near 0 V similar to a single IGZO TFT. It also represents high on-state current level above 10 mA (10^{-2} A) at gate bias of 70 V, similar to a single InO_x TFT. It is more clearly shown in the inset of Fig. 2a.

Important electrical parameters representing the performance of the TFTs, such as field-effect mobility, threshold voltage, SS value, and current on-off ration, can be extracted from the transfer curve shown in Fig. 2a^{1,4}. In case of field-effect mobility, as shown on the left y-axis in Fig. 2b, it was calculated using the following equation:

$$I_{DS} = \mu C_i \frac{W}{L} \left((V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right), \quad (1)$$

where μ is the field-effect mobility, C_i is the capacitance of the gate insulator, W is the channel width, and L is the channel length. A single InO_x TFT and dual-stacked TFT represented very high field-effect mobility of $77.01 \text{ cm}^2/\text{V}\cdot\text{s}$ and $77.48 \text{ cm}^2/\text{V}\cdot\text{s}$, respectively. On the other hand, a single IGZO TFT showed relatively low field-effect mobility of $19.62 \text{ cm}^2/\text{V}\cdot\text{s}$. In the case of threshold voltage, as shown on the right y-axis in Fig. 2b, it was calculated by fitting a straight line to the plot of the square root of I_{DS} versus V_{GS} , shown in eq. 1. A single IGZO TFT and dual-stacked OS-based TFT represented threshold voltage of 1.12 V and 4.36 V , respectively. InO_x TFT, on the other hand, showed a threshold voltage of -21.81 V , which was negatively shifted far from 0 V . In the case of SS, as shown on the left y-axis of Fig. 2c, it was calculated by the inverse of the maximum slope of the transfer characteristic:

$$SS = \left(\frac{d \log(I_{DS})}{dV_{GS}} \Big|_{\max} \right)^{-1}. \quad (2)$$

A single IGZO TFT and dual-stacked OS-based TFT showed very low SS value of $0.28 \text{ V}\cdot\text{dec}^{-1}$ and $0.47 \text{ V}\cdot\text{dec}^{-1}$, respectively. On the other hand, a single InO_x TFT showed a rather high SS value of $2.42 \text{ V}\cdot\text{dec}^{-1}$, resulting in a tilted shape of the transfer curve near turn-on voltage. In the case of current on-off ratio, as shown on the right y-axis of Fig. 2c, both a single IGZO TFT and dual-stacked OS-based TFT showed very high current on-off ratio over 10^9 . On the other hand, a single InO_x TFT showed a low current on-off ratio about 10^5 .

All things considered, the dual-stacked OS-based TFTs showed the most outstanding characteristics. It is noteworthy that the field-effect mobility and off-state characteristics (threshold voltage and current on-off ratio), which have been considered trade-offs, have improved at the same time^{38,39}. This is due to the induced area formed at the interface of OSs, resulting from electron confinement by band-offset, which is a key point of the working mechanism in our newly proposed dual-stacked OS-based TFTs.

Analysis on Oxygen Vacancy and Energy Bandgap of OSs

XPS measurements were conducted to verify the oxygen vacancy in InO_x and IGZO, respectively, which constitute the dual-stacked OS-based TFTs. Fig. 3 shows the chemical changes in the O 1s spectrum of three kinds of TFTs measured using X-ray photoelectron spectroscopy (XPS). For further analysis, the O 1s spectrum was fitted by the Gaussian-Lorentzian function. For a single InO_x TFT shown in Fig. 3a, the O 1s spectrum could be divided into the three peaks centered at 532.2, 531.1, and 529.8 eV, corresponding to the oxygen bond of the hydroxide (O-H bond), the oxygen vacancy (O_{vac}), and metal-oxide bond without oxygen vacancy (M-O bond), respectively^{28,40}. And for a single IGZO TFT and dual-stacked OS-based TFT shown in Fig. 3b and Fig. 3c respectively, the O 1s spectrum could be divided into the three peaks centered at 532.2, 531.1, and 530 eV. The $\text{O}_{\text{vac}} / (\text{O}_{\text{vac}} + \text{M-O bond})$ area ratios calculation method used to verify the effect of oxygen vacancy are 0.40 (a single InO_x TFT), 0.15 (a single IGZO TFT), and 0.18 (dual-stacked OS-based TFT).²⁶ A single InO_x TFT and dual-stacked OS-based TFT represent very low area ratios, which are expected to have affected the improved off-state properties such as threshold voltage, SS value, and current on-off ratio except field-effect mobility. This is consistent with the tendency of the data shown in Fig. 2.

It is widely known that the reduction in oxygen vacancy reduces the carrier density, resulting in less electron mobility⁴¹. However, dual-stacked TFT showed high field-effect mobility similar to a single InO_x TFT, although oxygen vacancy was low. This means that there are charge carriers that can be involved in current conduction except for oxygen vacancy. These charge carriers exist at the interface of OSs in TFTs, which is due to the electrons confined by band-offset.

In order to clearly confirm the presence of confined electrons at the interface of OSs and to understand the mechanism of current conduction, it is important to know the energy band structure diagram of the OSs in TFTs. To that end, ultraviolet-visible spectroscopy (UV-vis) and ultraviolet photoelectron spectroscopy (UPS) measurement were conducted. First of all, the optical band gap energy of InO_x and IGZO film was calculated based on UV-vis measurement data, respectively, as shown in Fig. 4a⁴². Then, the energy gap from valence band maximum (VBM) to Fermi energy level and work function were extracted from UPS measurement data, as shown in Fig. 4b. Based on these data, the energy band gap structure of dual-stack OS consisting of InO_x and IGZO was drawn, as shown in Fig. 4c⁴³. The electrons are confined in an induced area bent by a band-offset, and they play a very important role in the current conduction as the charge carriers in dual-stacked OS-based TFTs.

Conduction Mechanism in a Single OS-based TFTs

Theoretical studies on the conduction mechanisms in the single OS-based TFTs have been studied a lot so far, and specific theories, such as the accumulation or depletion of electrons at the boundary between semiconductor and gate insulator, have been established accordingly.^{1,3,12} However, the exact conduction mechanisms in the dual-stacked OS-based TFTs have not been reported so far. In this study,

we prevail the new types of conduction mechanisms that can be applied to both single OS-based TFTs and dual-stacked OS-based TFTs. A key point is the overlap between induced areas, which is due to the electrons confined by band-offset.

Fig. 5 shows the conduction mechanisms of accumulation mode and depletion mode, respectively, in a single OS-based TFT. First of all, an area induced by the gate bias is formed at the bottom of OS layer adjacent to the gate insulator, which is named as a gate-bias-induced area (GBIA). And another area induced by the source-drain bias is formed at the top of OS layer adjacent to the source-drain electrodes, which is named as an electrode-bias-induced area (EBIA). Based on these, Fig. 5a shows GBIA and EBIA in accumulation mode of a single OS-based TFT. When positive gate bias is applied, electrons accumulate at GBIA (red area) of OS layer, as shown in the top image of Fig. 5a. As gate bias increases, GBIA widens, resulting in more accumulated electrons. EBIA (green area) also widens as source bias increases, meaning that the deeper area is affected by source-drain bias.

GBIA and EBIA are always formed together and can be divided into three cases depending on the thickness of OS layer. First, as shown in Fig. 5b, it is the case that OS layer is included in GBIA. As these two areas are connected, electrons accumulated in GBIA can be used in current flow from source to drain in EBIA. At this time, as the thickness of OS layer increases in the range of GBIA, the field-effect mobility increases proportionally because of OS layer having more overlap with GBIA where the electrons are accumulated. Second, as shown in Fig. 5c, it is the case that OS layer is included in the combined area of EBIA and GBIA. Even in this case, since GBIA and EBIA are connected, the electrons accumulated in GBIA can be used in current flow from source to drain in EBIA. Since GBIA is already included within OS layer, all electrons accumulated in GBIA can always be used even if the thickness of OS layer increases. Thus, it represents maximum field-effect mobility, which also remains unchanged. Third, as shown in Fig. 5d, it is the case that OS layer is not included in the combined area of EBIA and GBIA. In this case, the electrons accumulated in GBIA cannot be used in current flow because GBIA and EBIA are not connected, so the dual-stacked OS-based TFTs represent the bulk characteristics of EBIA where current flows directly.

The tendency in the depletion mode is similar as in the accumulation mode. When applying gate and source-drain bias in TFT, it is the same as in accumulation mode that two areas of GBIA and EBIA are formed, respectively, as shown in Fig. 5e. However, there is a difference that electrons are depleted in GBIA, unlike accumulated electrons in accumulation mode. GBIA and EBIA are always formed together and can be divided into three cases depending on the thickness of OS layer, as in the above mentioned accumulation mode. First, as shown in Fig. 5f, it is the case that the OS layer is included in the GBIA. In this case, there is little current flow from source to drain regardless of the thickness of OS layer because electrons are depleted in GBIA. Second, as shown in Fig. 5g, it is the case that the OS is included in the combined area of EBIA and GBIA. Even in this case, there is little current flow from source to drain due to the effects of the depleted electrons in GBIA connected to EBIA. Even if the thickness of OS layer thickens, there is still little current flow as long as EBIA is connected to GBIA with depleted electrons. Third, as shown in Fig. 5h, it is the case that the OS is not included in the combined area of EBIA and GBIA. In this case, since GBIA and EBIA are not connected, the current flow is not affected by the depleted electrons in

GBIA, but only by the characteristics of the bulk area in EBIA. This tendency is similar as in accumulation mode shown in Fig. 5d.

Conduction Mechanism in the Dual-Stacked OS-based TFTs

Fig. 6 shows the conduction mechanism in the dual-stacked OS layers in the accumulation mode of TFT, based on the conduction mechanism in a single OS layer of TFT mentioned above. Because GBIA is formed at the bottom of the OS layer adjacent to the gate insulator, it affects the lower OS layer in the dual-stacked OS. Since EBIA is formed at the top of the OS layer adjacent to the source-drain electrodes, it affects the upper OS layer in the dual-stacked OS. In this study, because it has high carrier concentration, resulting in high field-effect mobility, InO_x was used as a lower OS layer affected by GBIA. Then, IGZO was used as an upper OS layer affected by EBIA because it has a low SS value and good off-state performance such as threshold voltage and current on-off ratio.

As shown in Fig. 4c above, in the dual-stacked structure, the electrons are confined by band-offset at the boundary between connected OSs, an effect that cannot be seen in a single OS structure. As a result, as shown in Fig. 6b, an area induced by confined electrons is formed at the top of InO_x and named as a band-offset-induced area (BOIA). As shown in Fig. 6c, another area is induced at the bottom of IGZO in contact with InO_x , by BOIA, and named as BOIA-induced area (BIA). In summary, BOIA and BIA are formed at each boundary of the connected semiconductors when two OSs come into contact. At this time, when gate bias and source-drain bias are applied, GBIA and EBIA are formed, respectively, and connected to BOIA and BIA as shown in Fig. 6d. After all, GBIA with accumulated electrons is connected sequentially to EBIA, which can lead to high current flow. However, if the thickness of IGZO, upper layer in dual-stacked OS, becomes thicker, EBIA and BIA is not connected. It means that the accumulated electrons in GBIA cannot be used in current flow from source to drain, resulting in the bulk characteristics of EBIA.

Meanwhile, in the case of depletion mode of dual-stacked OS-based TFT, the depleted electrons in GBIA can be considered as a key factor instead of the accumulated electrons. GBIA and EBIA formed by gate bias and source-drain bias, respectively, are connected to BOIA and BIA as in the accumulation mode. Then, there is little current flow from source to drain by the influence of depleted electrons in GBIA. In addition, if the thickness of IGZO becomes thicker, it represents the characteristics of the bulk area of EBIA as in the accumulation mode.

It is important to design the optimal thickness of OSs due to the characteristics of the dual-stacked structure. Especially, in the case of IGZO used as the buffer layer at the top in the dual-stacked OS-based TFTs, the field-effect mobility has a maximum convergence value as the thickness of IGZO increases within the overlapping range of EBIA and BIA, as shown in Supplementary Fig. 3 and Supplementary Table 4. On the other hand, in the case of InO_x used as the channel layer at the bottom, the minimum optimized thickness should be maintained to reduce leakage current. Therefore, only the thickness of

IGZO were adjusted to verify the conduction mechanism. This precise design of the thickness of OS layers will provide the realistic design rules for actual applications in the display industry.

Stabilities of OS-based TFTs in PBS and NBS

Another important criterion for evaluating the performance of OS-based TFTs is stability, which should be considered important as a switching device in the display. To evaluate the stability of dual-stacked OS-based TFTs, positive bias stress (PBS) measurements were carried out compared to a single IGZO TFT over 3600 s, at a gate voltage (V_{GS}) of 20 V, a drain voltage (V_{DS}) of 10 V, as shown in Fig 7a. And the threshold voltage shifts, the results of PBS measurements, were listed in Table 1. The dual-stacked OS-based TFT represents a small shift of 2.62 V after 3600 s, similar to a single IGZO TFT representing 2.65 V. Subsequently, negative bias stress (NBS) measurements were carried out over 3600 s, at V_{GS} of -20 V, V_{DS} of 10 V as shown in Fig. 7b. The threshold voltage shifts and the results of NBS measurements were listed in Table 2. The dual-stacked OS-based TFT also represents a small shift of 1.72 V after 3600 s, similar to a single IGZO TFT representing 1.67 V. As a result, it was confirmed that the dual-stacked OS-based TFT represented good stability similar to a single IGZO TFT in both PBS and NBS. This can be attributed to the influence of IGZO layer, which are used as top layer in dual-stacked OS of TFT structure. As expected, the results of PBS and NBS measurements of a single InO_x TFT are not good, as shown in Supplementary Fig. 4 and Supplementary Table 5.

Discussion

In summary, we have prevailed the working mechanism and the role of dual-stacked OSs with the concept of induced area, consisting of the channel layer at the bottom and the buffer layer at the top, resulting in high electrical performance TFTs. In the case of lower OS layer in the dual-stacked OS, InO_x was deposited on SiO_2 , acting as gate insulator, to improve the field-effect mobility. In the case of upper layer in the dual-stacked OS, IGZO was subsequently deposited to reduce the leakage current. As a result, electrical performances of dual-stacked OS-based TFTs were remarkably improved for very high field-effect mobility of $\sim 80 \text{ cm}^2/\text{V}\cdot\text{s}$, ideal threshold voltage near 0 V, and very high on-off current ratio of $>10^9$, which could not be realized by a single OS-based TFT alone. Field-effect mobility and threshold voltage, which have been considered trade-off so far, have been improved at the same time, resulting from the investigation of the role of dual-stacked OS in TFTs. And these dual-stacked OS-based TFTs represent little threshold voltage shifts of 2.62 V and 1.72 V at PBS and NBS, respectively. Meanwhile, accumulated or depleted electrons in gate-bias-induced area (GBIA) are a key factors in conduction mechanism of dual-stacked OS-based TFTs. GBIA is connected to electrode-bias-induced area (EBIA) by band-offset-induced area (BOIA) and BOIA-induced area (BIA) induced by the band-offset, resulting in contribution of current conduction. Based on the comprehensive understanding of the role of dual-stacked OSs in TFTs, we developed new design rules for the high performance OS-based TFTs. Such proposed design rules are

expected to be widely implemented for applications that require fast response, ultra-high resolution, and low power consumption.

Methods

Fabrication of the TFTs. To fabricate the single OS-based and dual-stacked OS-based TFTs, the heavily B-doped p-type Si wafers (P^{++} -Si) with thermally grown 200 nm SiO_2 layer was used as a role of the gate electrode and the gate insulator, respectively. These wafers were subsequently cleaned by detergent for 15 min, de-ionized (DI) water rinsing for 20 min, acetone for 15 min, and isopropyl alcohol (IPA) for 15 min. All cleanings except DI water rinsing were conducted in ultrasonic bath. InO_x or IGZO layer was deposited on a SiO_2 / Si substrate by using RF sputter (DAEKI HI-TECH co., Ltd, Co-Sputtering System) with a planer round target consisting of InO_x or IGZO ($In:Ga:Zn:O = 1:1:1:4$ at%) under 10^{-4} mTorr at room temperature. The RF sputtering power for InO_x or IGZO layer was fixed at 40 W in mixed Ar / O_2 (50 sccm / 5 sccm) gases and at 90 W in Ar (25 sccm) gas, respectively. Then, sputtered InO_x or IGZO layers were annealed in the air at 250 °C for 90 s by RTA method. As the electrodes of source and drain, Al was deposited on InO_x or IGZO layer by thermal evaporation with a thickness of 100 nm, a channel width of 1000 , and a channel length of 50 through shadow masks. And all TFTs were patterned using photolithography and wet etching process to prevent leakage current.

Measurement and Analysis. The current-voltage characteristics for all TFTs were measured using an Agilent 4155B semiconductor parameter analyzer with compliance current of 10^{-2} A at room temperature in the dark conditions. The absorption and bandgap of a single OS layer were measured from 300 to 800 nm by UV-vis (Lambda 35, PerkinElmer). And work function and energy gap from VBM to Fermi energy were measured by UPS (AXIS SUPRA, Kratos). XPS (AXIS SUPRA, Kratos) equipped with a monochromic Al αK X-ray source was used to analyze the chemical properties of OS layers. The samples for HR-TEM observation were prepared by ion-beam processing techniques through Quanta 3D FEG. A platinum-plated layer with a thickness of 15 nm was deposited via sputter before TEM sample preparation to make its surface more conductive. The HR-TEM images were all obtained by a JEM-2100F field emission electron microscope from JEOL Ltd.

Declarations

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Author contributions

C.I., N.-K.C., J.P., S.-E.L. and Y.S.K. designed the experiments and studied in-depth about the dual-stacked OS-based TFTs. C.I., E.G.L. and H.-J.N. performed the experiments for electrical properties of the devices. C.I. and Y.S.K. discussed the theoretical developments and working mechanism and carried out specification on the role of the dual-stacked OS in TFTs. C.I. and Y.S.K. wrote the manuscript based on discussion with all authors. Y.S.K. supervised the project direction including experimental and theoretical investigations for the dual-stacked OS-based TFTs.

Additional information

Supplementary information is available in the online version of the paper. Reprints and permissions information is available online at www.nature.com/reprints. Correspondence and requests for materials should be addressed to Y.S.K.

Competing financial interests

The authors declare no competing financial interests.

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Tables

Table 1. Threshold voltage shifts in a single IGZO TFT and dual-stacked OS-based TFT after PBS test

V _{TH} (V)	0 sec	1 sec	10 sec	100 sec	1000 sec	3600 sec
IGZO	-	0.01	0.03	2.14	2.58	2.65
InO _x + IGZO	-	0.02	0.03	2.22	2.59	2.62

Table 2. Threshold voltage shifts in a single IGZO TFT and dual-stacked OS-based TFT after NBS test

V_{TH} (V)	0 sec	1 sec	10 sec	100 sec	1000 sec	3600 sec
IGZO	-	0.00	0.02	1.21	1.54	1.67
InO_x + IGZO	-	0.00	0.01	1.23	1.61	1.72

Figures

Figure 1

Schematic images of the dual-stacked OS-based TFT and cross sectional images. (a) Dual-stacked OS-based TFT consisting of InO_x as a channel layer and IGZO as a buffer layer. (b) Cross sectional TEM images of dual-stacked OS-based TFT. (c) Mapping images of TEM representing the atomic dispersion.

Figure 2

(a) Transfer curves of a single InOx TFT, a single IGZO TFT, and dual-stacked OS-based TFT ($V_{DS} = 20V$). Inset: Zoom in region of the on-state current. Electrical properties extracted from transfer curves : (b) field-effect mobility (black), threshold voltage (red), (c) subthreshold swing (black), and current on-off ratio (red)

Figure 3

O 1s X-ray photoelectron spectroscopy (XPS) analysis for (a) a single InO_x TFT, (b) a single IGZO TFT, and (c) dual-stacked OS-based TFT

Figure 4

Optical analysis and energy band diagram of dual-stacked OS-based TFT. (a) PL spectra calculated from UV-vis data of InOx and IGZO films. (b) UPS spectra showing cut-off and VBM energy of InOx and IGZO films. (c) Energy band diagram of dual-stacked OS-based TFT drawn on the basis of (a) and (b).

Figure 5

Conduction mechanism in a single OS-based TFT in accumualtion and depletion mode. (a), (e) Two kinds of areas (GBIA and EBIA) induced by gate bias and source-drain bias. Relationship between GBIA and EBIA when (b), (f) only GBIA including OS, (c), (g) GBIA and EBIA including OS, and (d), (h) GBIA and EBIA not including OS.

Figure 6

Conduction mechanism in dual-stacked OS-based TFT. (a) GBIA induced in lower OS layer (InO_x) and EBIA induced in upper OS layer (IGZO). (b) BOIA induced from confined electrons by band-offset. (c) BIA induced by BOIA. (d) Final connection between GBIA, BOIA, BIA, and EBIA.

Figure 7

(a) Positive bias stress (PBS) results for a single IGZO TFT and dual-stacked OS-based TFT at $V_{GS} = 20V$ and $V_{DS} = 10V$, respectively. (b) Negative bias stress (NBS) results for a single InOx TFT and dual-stacked OS-based TFT at $V_{GS} = -20V$ and $V_{DS} = 10V$.

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