Mechanism for reconfigurable logic in disordered dopant networks

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Mechanism for reconfigurable logic in disordered dopant networks

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Abstract

We present an atomic-scale mechanism based on variable-range hopping of interacting charges enabling reconfigurable logic and nonlinear classification tasks in dopant network processing units in silicon. Kinetic Monte Carlo simulations of the hopping process show temperature-dependent current-voltage characteristics, artificial evolution of basic Boolean logic gates, and fitness-dependent gate abundances in striking agreement with experiment. The simulations provide unique insights in the local electrostatic potential and current flow in the dopant network, showing subtle changes induced by control voltages that set the conditions for the logic operation. These insights will be crucial in the systematic further development of this burgeoning technology for unconventional computing. The establishment of the principles underlying the logic functionality of these devices encourages the exploration and utilization of the same principles in other materials and device geometries.

The steeply increasing demand for computational power triggered by the rise of artificial intelligence and machine learning leads to unprecedented hardware demands [1]. At the same time, further miniaturization of state-of-the-art CMOS-based hardware to meet the demand slows down. One of the main problems is that the ongoing miniaturization of CMOS transistors leads to device variability induced by the decreasing number of dopant atoms in the transistor, which is below ten in the nowadays standard 10 nm node CMOS technology [2]. This leads to so-called 'random dopant fluctuations', causing a major problem in nanoscale devices [3]. Novel computing concepts that are insensitive to these fluctuations, or can even profit from them, would be a solution. Also, reconfigurability [4] exploiting intrinsic complexity and nonlinear operation [5–7] would be highly desirable. Recently, we explored a novel computing concept of this kind in dopant network processing units (DNPUs) made by implantation of boron (B) dopant atoms in silicon, with eight electrodes in a circular geometry defining a 300 nm-diameter active region at the Si surface [8]. An individual device can be configured to execute a specific logic or classification task by choosing one electrode as output and the other seven electrodes as inputs or controls. For example, Boolean logic can be realized when voltages corresponding to logic levels '0' and '1' are applied to two input electrodes, giving rise to a low ('0') or high ('1') current at the output electrode. The voltages applied at the remaining five control electrodes are adjusted to

obtain a high fitness of the Boolean gate, warranting a precise realization of the intended logic operation. Using suitable control voltages, an individual device can be configured to match any of the six basic logic gates (AND, OR, NOR, NAND, XOR, XNOR), demonstrating reconfigurability on demand. More complex logic functionality, e.g., using four input and three control electrodes, can also be achieved, which illustrates the potential of this new technology. Regarding energy-efficiency and footprint, the devices can compete with CMOS-based logic, while competitiveness regarding speed seems achievable. The devices operate reliably at liquid-nitrogen temperature (77 K) and even operation at room temperature has been demonstrated using a backgating technique. The devices are stable over periods of months and the logic operation is unchanged upon heating to room temperature and cooling back to 77 K [8]. Efficient neural network-type computing can be achieved by coupling DNPUs in hierarchical structures [9].

The control voltages for realizing a specific logic gate are different for each device and depend on the specific configuration of the dopant atoms in the active area. From the estimated B concentration at the silicon surface of the order of 10^{17} cm^{-3} and the implantation penetration depth of about 20 nm, we estimate that a few hundred dopant atoms are present in the active area. Previously, reconfigurable Boolean logic functionality was realized in disordered networks of Au nanoparticles [10], where conduction takes place by hopping of electrons between about 100-150 nanoparticles in the active area, governed by Coulomb blockade-physics. The limited number of active elements (dopant atoms or nanoparticles) in combination with disorder in their locations results for both systems in a strong device variability. However, in contrast to conventional transistors, this is not an impediment for realizing functionality, but an asset, since it allows designless fabrication without limiting functionality. The main advantages of the DNPUs over the Au nanoparticle devices are the compatibility with silicon technology, the operation at higher temperature (77 K, or even room temperature, vs 0.3 K), and the expanded functionality.

Functionality can be realized in both types of devices by artificial evolution, where the control voltages are treated as 'genes' that evolve by mutation and cross-breeding in an evolutionary process to optimize fitness for the desired functionality [8, 10]. Alternatively, a deep neural network can be trained to accurately emulate the complex multi-dimensional input-output relationship of a device, after which a desired functionality is found by gradient descent, with the difference between the actual and the desired input-output relation

as cost function [11]. Both approaches are physics agnostic, i.e., they do not assume a specific physical mechanism for the device operation. However, in order to understand the operation, and explore and improve the ultimate performance of the devices on rational grounds, it is mandatory to consider the underlying microscopic physical mechanisms. For the Au nanoparticle system a kinetic Monte Carlo (KMC) simulation tool based on Coulomb blockade-governed hopping between adjacent nanoparticles was developed [12]. The tool was applied to small regular networks of nanoparticles, where the evolution of basic Boolean gates with reasonable fitness was demonstrated.

In the present paper we explore the atomic-scale mechanism for the reconfigurable logic operation of DNPUs. The mechanism is based on variable-range hopping (VRH) of charge carriers in between the dopant atoms, which can occur in the neutral or ionized state. All Coulomb interactions between the charges are taken into account. A specialized KMC tool was developed for simulations of the device behaviour. We first show that the simulations reliably describe the measured electrical behaviour of the devices and their reconfigurable Boolean logic. We then use the simulations in an analysis of device operational aspects, providing a profound understanding of the operation mechanism that will be crucial for a systematic further development of DNPU technology. Our work presents a unique study of VRH physics, which has been explored in great depth to describe charge transport in a large variety of bulk disordered materials, to a disordered nanoscale system. Our study focuses specifically on DNPUs, but the methods, results and conclusions have a general applicability to a wide range of disordered nanoscale systems of materials and device geometries for unconventional computing.

RESULTS

Current-voltage characteristics

The inset of Fig. 1a shows the simulated geometry of a representative device, where circular segments are used to model the electrodes. The dots indicate 200 randomly placed B dopant atoms (dopants), a number roughly estimated from experiment [8]. Since in the experiments silicon wafers with an n-type background doping are used, we also randomly place three n-type counterdopants in the active area (red crosses), corresponding to a typ-

ical background doping of 2×10^{15} cm^{-3}. We assume that the counterdopants are ionized and thus positively charged. The ionization energy of a dopant depends on its random distance to the Si surface and possibly other random fluctuations in its environment. We model these fluctuations by a Gaussian energy disorder in the dopant ionization energy with standard deviation σ. For specified voltages applied to the eight electrodes we solve the Laplace equation for the electrostatic potential. We simulate the two-dimensional (2D) VRH of charge carriers in between the dopants and between the dopants and the electrodes, described by the phonon-mediated Miller-Abrahams (MA) hopping rate [13]. We take into account Coulomb interactions between all charges (see Methods).

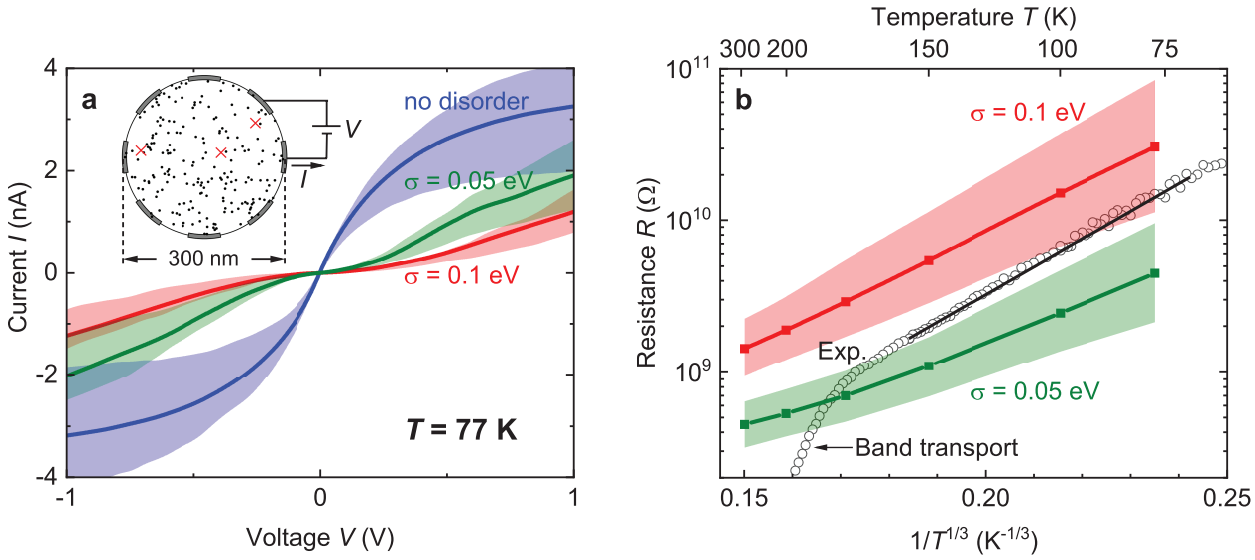


Figure 1. **Current-voltage characteristics.** **a**, Inset: geometry of a representative simulated device with segmented electrodes, and 200 randomly positioned dopants (dots) and 3 counter-dopants (red crosses). Main panel: simulated current I as function of voltage V at temperature $T = 77$ K averaged over 8 adjacent electrode combinations of 30 devices, without energy disorder (blue) and with energy disorder strengths $\sigma = 0.05$ (green) and 0.1 eV (red). Half of the 240 I-V characteristics fall in the shaded regions. **b**, Squares connected by lines: geometrically averaged resistances R for $\sigma = 0.05$ and 0.1 eV as function of $1/T^{1/3}$, obtained from the linear parts of the I-V characteristics in panel a around $V = 0$. Half of the resistances fall in the shaded regions. Circles: measured resistances from Fig. 2 in Ref. [8]. Line: linear fit in the region 70–160 K. Error bars of the simulated and experimental data are negligible on the used scales.

The curves in the main panel of Fig. 1a are the averaged simulated currents I at a temperature $T = 77$ K of the device displayed in the inset and 29 other devices with different positions of the (counter)dopants, when applying a voltage V between two adjacent electrodes. The average includes the eight possible adjacent electrode combinations for each device. The results can be compared to the device characterization measurements in Ref. [8]. For the case without energy disorder (blue curve) the current saturates with growing voltage, leading to sublinear instead of the observed superlinear I-V characteristic, measured for a combination of adjacent electrodes of a device (see Fig. 2 of Ref. [8]). The reason for the saturation is that for energetically downward hops, which dominate the transport at high electric field, the MA rate has no energy dependence. Introducing the energy disorder yields the observed superlinear characteristics on a voltage and current scale comparable to the experiment. We show results for $\sigma = 0.05$ eV (green curve) and 0.1 eV (red curve). For $\sigma = 0.05$ eV, the I-V characteristics become sublinear beyond $|V| \approx 0.5$ V. For $\sigma = 0.1$ eV, the superlinear behaviour is present up to $|V| = 1$ V, like in the experiment. Half of the simulated 240 I-V characteristics fall in the shaded regions in Fig. 1a, which quantifies the device variability. Since different Si wafers may have different background doping concentrations we checked the effect of changing the number of counterdopants. Figure S1 in Supplementary Note 1 compares for $\sigma = 0.1$ eV the average I-V characteristics of Fig. 1a for 3 counterdopants with those for 10, 20, and 50 counterdopants. We find only a modest increase of the current with the number of counterdopants. The reason for this insensitivity is that the number of mobile charges present in the system is mostly determined by injection from the electrodes and not by the number of counterdopants. We thus conclude that variations in the background doping concentration are not critical.

For a further analysis we plot in Fig. 1b for $\sigma = 0.05$ and 0.1 eV the geometric average of the resistances R, extracted from the linear parts of the simulated I-V characteristics around $V = 0$, as a function of $1/T^{1/3}$. The almost straight lines in the semi-logarithmic plots confirm the dependence $R(T) = R_0 \exp\left[(T_0/T)^{1/(1+d)}\right]$ predicted for VRH hopping in $d = 2$ dimensions by Mott [14]. Half of the resistances fall in the shaded regions. The large width of the shaded regions of almost an order of magnitude at low T is the reason why we consider the geometric instead of the ordinary average of the resistances. Also plotted (symbols) is the T-dependent resistance extracted from the measurements in Ref. [8] for an adjacent electrode combination of a device. Above about 160 K, the experimental resistance

starts to deviate from VRH behaviour, which is attributed to the onset of band conduction due to thermal dopant ionization [8]. We note that the KMC simulations do not take into account band conduction. Considering the large variation in R, the simulated results for both disorder strengths are below this temperature in fair agreement with the measurements. It is reassuring that agreement is obtained using a prefactor in the MA hopping rate equal to a typical phonon frequency (10^{12} Hz, see Methods), which sets the absolute current scale. A modest increase of this prefactor by a factor of about 2 would for $\sigma = 0.1$ eV lead to an almost perfect agreement with experiment.

The temperature at which the experimentally observed transition from hopping to band transport occurs yields an estimated effective ionization energy of 130 meV [8], instead of the 45 meV ionization energy of boron in bulk silicon [15, 16]. The difference is attributed to the smaller dielectric screening of the Coulomb interaction at the Si surface. Since the distance of the active B dopants to the Si surface will vary between dopants, so will their ionization energy. Disorder strengths of the order of the difference between the experimentally estimated and bulk ionization energy are therefore expected, which holds for the two considered disorder strengths. Because (1) the value $T_0 = 4.7 \times 10^4$ K for $\sigma = 0.1$ eV (obtained from the slope of the red line in Fig. 1b) agrees better with the experimental value of 7.7×10^4 K than the value $T_0 = 2.7 \times 10^4$ K for $\sigma = 0.05$ eV and (2) the superlinear behaviour is, as in the experiment, present in the whole voltage range, we will from now on consider the case $\sigma = 0.1$ eV as a realistic estimate of the energy disorder strength. The quantification of the influence of energy and positional disorder of the dopants is a first demonstration of how our modelling can be used to extract critical parameters determining the functioning of the DNPUs that are at present impossible to obtain experimentally.

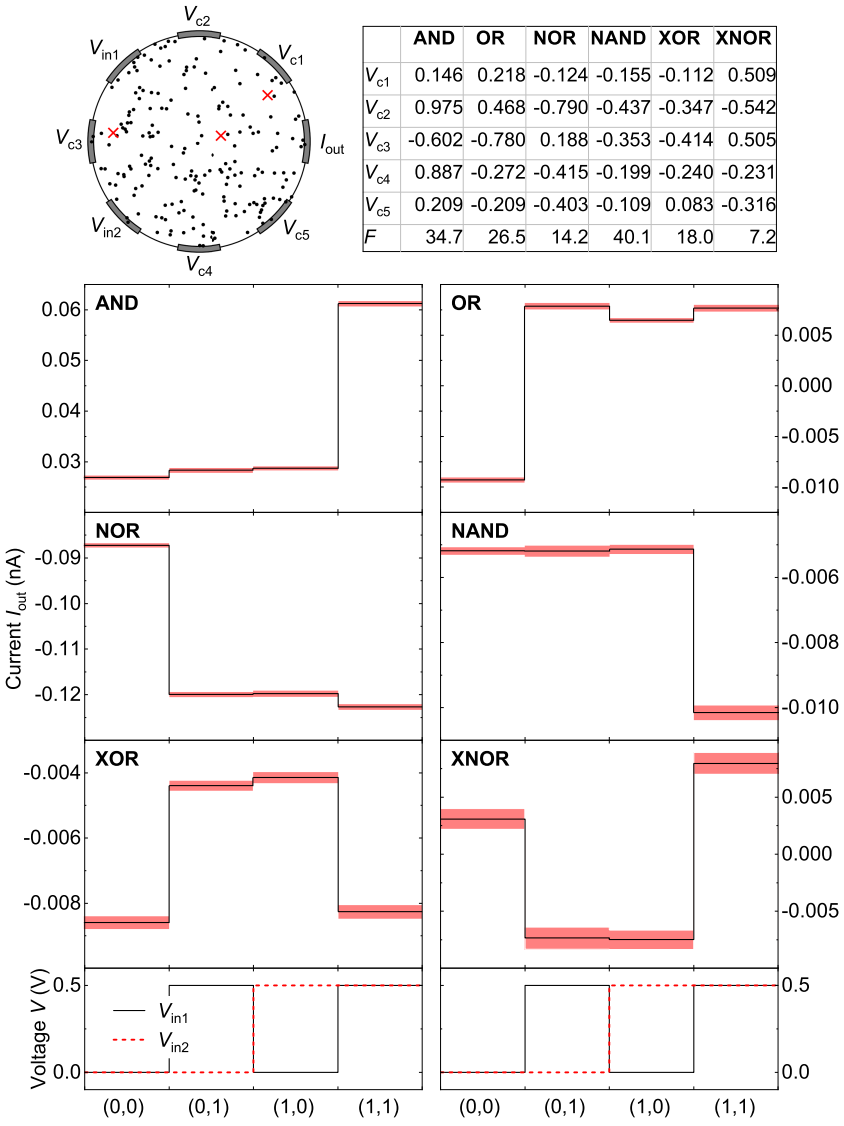
Boolean functionality

As in the experiment, we obtain Boolean functionality at 77 K by optimizing a fitness function for each logic gate, where two voltages V_{in1} and V_{in2} can take on the values 0 V (logic '0') and 0.5 V (logic '1'), and the current I_{out} to ground (0 V) is measured at an output electrode. The optimization takes place by artificial evolution of the control voltages V_{c1}–V_{c5} of the five remaining electrodes using an evolutionary algorithm (see Methods). These are referred to as the 'genes' and are restricted to lie in the interval [−1,1] V. At the top

left of Fig. 2 the model device shown in the inset of Fig. 1a is reproduced, indicating the input, output, and control electrodes. Examples of artificially evolved control voltages for the six basic Boolean logic gates and their gate fitnesses F are given in the table at the top right. The panels below show I_{out} for the different logic input combinations, displayed in the bottom panels. The shaded regions indicates the uncertainty in I_{out} (see Methods for its determination). We find excellent agreement with the gates reported in the experiment [8]. This holds for the quality (fitness) of the gates as well as the magnitude of the currents, which is of the order of 0.01–0.1 nA. Relatively high fitnesses are obtained for the AND, OR, and NAND gate, whereas the NOR, XOR and particularly the XNOR gate show relatively low fitnesses. We note that the AND, OR, NAND, and NOR gates solve linearly separable problems. We will show in the next subsection that typical fitness values for these four gates are very similar. The relatively small fitness value for the NOR gate found in this specific example reflects the challenge of fitness optimization in a complex high-dimensional fitness landscape.

We note that it is to a large extent an arbitrary choice which electrodes are used for input, output, and control. It may be advantageous when the input electrodes are not adjacing the output electrode or each other, because the control voltages can then more effectively influence the output current differences for the different inputs. This is the case for the electrode choices in Fig. 2, but, as shown in experiment [8], two adjacent electrodes can also be chosen as the input electrodes. We also note that there is nothing special or specifically suitable about the device of Fig. 2. Figure S2 in Supplementary Note 2 shows the realization of the six basic logic gates with comparable fitnesses in a device with other random positions of the (counter)dopants. This shows that gates with good fitness can in principle be evolved for any device, as also found experimentally [8].

The 10^7 KMC steps used to obtain the results in Fig. 2 correspond to time intervals in the range $1.5\text{–}3.5 \times 10^{-5}$ s, where the actual value for each case depends on the specific gate and input combination. This is more than four orders of magnitude shorter than the 0.5 s used in the experiment [8]. In the simulations, the uncertainty in the current is the cumulative effect of stochastic hopping events of single charges. During the measurement time of 0.5 s considerable fluctuations in the experimental current are observed, which are much larger than the fluctuations KMC simulations show on this time scale. This demonstrates that in the experiment the noise in the current is not the intrinsic noise due to individual hopping



	AND	OR	NOR	NAND	XOR	XNOR
V_{c1}	0.146	0.218	-0.124	-0.155	-0.112	0.509
V_{c2}	0.975	0.468	-0.790	-0.437	-0.347	-0.542
V_{c3}	-0.602	-0.780	0.188	-0.353	-0.414	0.505
V_{c4}	0.887	-0.272	-0.415	-0.199	-0.240	-0.231
V_{c5}	0.209	-0.209	-0.403	-0.109	0.083	-0.316
F	34.7	26.5	14.2	40.1	18.0	7.2

Figure 2. **Boolean functionality.** Top left: device (same as in inset Fig. 1a) with input voltages V_{in1}, V_{in2}, control voltages V_{c1}–V_{c5}, and output current I_{out}. Middle panels: I_{out} and uncertainties (shaded regions) for the six basic Boolean logic gates found with artificial evolution at 77 K, with V_{in1}, V_{in2} given in the bottom panels and V_{c1}–V_{c5} and fitnesses F in the table at the top right. The currents and their uncertainties were determined from KMC simulations of 10^7 steps.

events but extrinsic noise, probably caused by the measurement equipment. If the noise can be suppressed to the intrinsic noise level, much shorter experimental measurement times should be possible. We verified that the uncertainty in the simulated current scales as $1/\sqrt{N}$

with the number N of KMC steps for time scales exceeding the used equilibration time ($\sim 10^4$ KMC steps, see Methods), which demonstrates that the intrinsic noise is uncorrelated at these time scales. Figure S3 in Supplementary Note 3 gives results equivalent to Fig. 2, but for $N = 10^6$ instead of 10^7 KMC steps, showing an approximately $\sqrt{10}$ larger uncertainty in the current. For even smaller simulation times it will finally become impossible to distinguish between the different logic current levels. This is for the device in Fig. 2 most critical for the realization of the XOR gate, where the logic current levels will become indistinguishable if the uncertainty in the current increases by a factor of about 5. The 25 (5^2) times shorter time scale than that of 1.5–3.5 $\times 10^{-5}$ s in Fig. 2 leads to an estimate from our simulations of about 1 MHz for the maximum DNPU operational frequency where current levels can still be distinguished for all gates.

The KMC simulations offer the unique possibility to obtain microscopic information about the local potential and current flow within the device that is, at least presently, impossible to obtain experimentally. Figure 3 shows, for the same device and Boolean gate realizations in Fig. 2, the time-averaged voltages at the electrodes and at each dopant as well as the currents in between the dopants and between the dopants and the electrodes. The currents flowing into or out of the electrodes are also shown. The first row shows results for the AND gate, as an example of a gate solving a linearly separable problem (the others are OR, NOR, and NAND), and the second row shows results for the XOR gate, as an example of a gate solving a linearly inseparable problem (the other is XNOR) [6, 7, 17]. Results are given for the logic input combinations (0,0), (0,1), (1,0), and (1,1). We observe that the differences in the voltage and current distributions between the four different input combinations are for both gates remarkably small, while the differences in between the AND and XOR gate are comparatively large. The third row shows results for the OR, NOR, NAND, and XNOR gates, in these cases only for the (0,0) input. We verified that also for these gates the differences in the voltage and current distributions between different input combinations are small. The fourth row shows results for four randomly chosen control voltages in the interval $[-1,1]$ V for (0,0) input, while results for 16 other randomly chosen control voltages are given in Fig. S4 of Supplementary Note 4. We observe that, in general, the output currents for the control voltages found for the Boolean gates are smaller than those for random control voltages. Taken together, these observations suggest an explanation – substantiated below – for the realization of Boolean functionality by the evolutionary algorithm that has

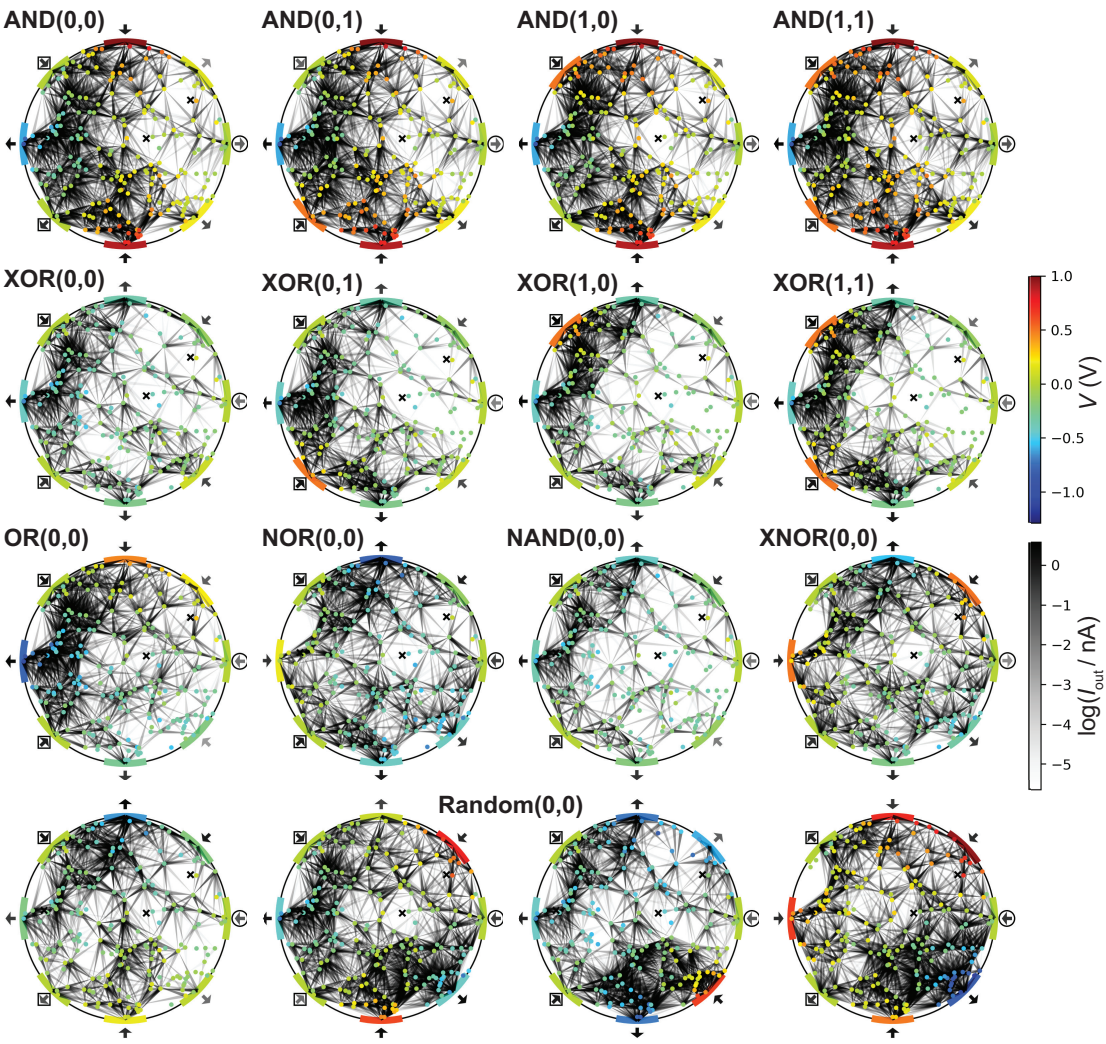


Figure 3. **Voltage and current distributions.** Time-averaged voltages (linear colour scale) and currents (logarithmic grey scale, current direction from wide to narrow) in the device, for the simulations in Fig. 2. Arrows with different grey scale: currents flowing into or out of the electrodes. Squares: input electrodes. Circle: output electrode. First row: AND gate for the four different logic input combinations. Second row: XOR gate. Third row: OR, NOR, NAND, and XNOR gates for logic input (0,0). Fourth row: four random control voltages in the interval [−1,1] V for logic input (0,0).

two ingredients. (1) For all gates, the tuning of the control voltages by the evolutionary algorithm is such that the output current is small for all input combinations. As a result, small changes in the control and input voltages can lead to large relative changes in the

output current, thus creating a high tunability. We note here that the used fitness function is only sensitive to relative current differences and not to the absolute current scale (see Methods). (2) For each specific gate, the high tunability allows relatively facile tuning of the control voltages by the evolutionary algorithm to yield the corresponding logic with high fitness. The non-linearity, complexity, and flexibility of the DNPUs allow a high-fitness realization of all Boolean logic gates in one and the same device. Interestingly, there is no obvious correlation between a particular gate and its voltage and current distribution, as shown by the completely different voltage and current distributions for another device in Fig. S5 of Supplementary Note 5. Also for the hopping dynamics in other disordered systems it has been found that the total current in the non-linear regime does not need to be related to some obvious pattern of the current distribution [18].

This tentative explanation for the realization of Boolean functionality is corroborated by a study of the output currents I_{out} for the four logic input combinations and the resulting gate fitness F when changing a control voltage from the value found by artificial evolution. In Fig. 4 I_{out} is shown for the AND and XOR gate when changing the control voltage V_{c1}. At the values of V_{c1} found by the evolutionary algorithm (vertical dashed lines, values as in Fig. 2) all four output currents are small, as is clear by comparing panels a and b, and panels c and d. As a result, changes in the voltages of the input electrodes can have a large relative influence on the output current, despite the fact that these electrodes are further away from the output electrode than the adjacent electrode to which V_{c1} is applied. The strong correlation in the output currents for the four logic input combinations observed in Figs. 4a and c is a general feature that is confirmed in Fig. S6 in Supplementary Note 6, where this correlation is studied for random control voltage combinations. By comparing the heights as well as the widths of the peaks in Figs. 4b and d we conclude that it is much easier to find a good AND gate than a good XOR gate. This is understandable, because the negative differential resistance (NDR) required for the XOR gate to obtain a decreasing current when switching from the logic input (0,1) or (1,0) to the logic input (1,1) is a subtle feature that is difficult to realize (see next subsection). By contrast, the AND gate does not require NDR. We note that stochastic fluctuations in the current lead to fluctuations in the fitness values, which are most clearly visible around the peak in Fig. 4b. Figure S7 in Supplementary Note 7 shows results equivalent to Fig. 4 for the output currents for the four logic input combinations and the resulting AND and XOR gate fitnesses when changing V_{c2}

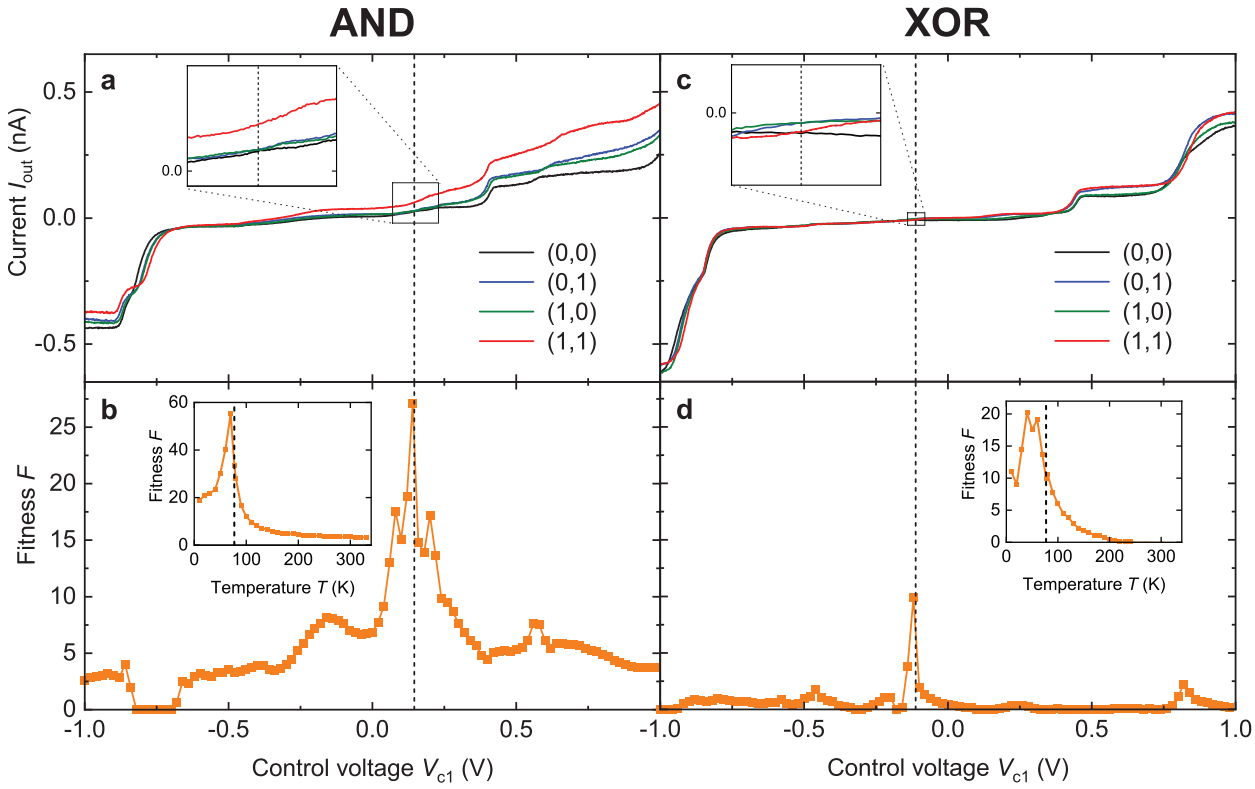


Figure 4. **Control voltage and temperature sensitivity of AND and XOR gates. a**, Output currents I_{out} for the four logic input combinations and **b**, fitness F of the AND gate of Fig. 2 as a function of the control voltage V_{c1}. Vertical dashed lines in a and b: value of V_{c1} found by artificial evolution. Inset in a: magnification of indicated area. Inset in b: temperature dependence of F for the control voltages found by artificial evolution at 77 K (vertical dashed line). **c** and **d**, Same as a and b, but for the XOR gate.

and V_{c3}. Because the corresponding electrodes are further away from the output electrode than the electrode of V_{c1}, the output currents are in that case less influenced by the control voltage than in Fig. 4. Results for changing V_{c4} (V_{c5}) are qualitatively similar to those for changing V_{c2} (V_{c1}) because of symmetry (see the electrode labeling of the device at the top left in Fig. 2).

The insets in Figs. 4b and d show the temperature dependence of the fitness of the AND and XOR gate, respectively, when the control voltages V_{c1}–V_{c5} are fixed to their values found by artificial evolution at 77 K. The results are qualitatively similar to those presented in Extended Data Fig. 3b of Ref. [8] (in that case for a NAND gate). Like in the experiment,

we find that F first slightly increases with decreasing temperature and then decreases, while with increasing temperature F decreases monotonically.

Boolean gate abundances

In order to quantify the ease or difficulty of finding a Boolean gate with a certain fitness we plot in Fig. 5 for random combinations of the control voltages V_{c1}–V_{c5} in the interval $[-1,1]$ V the abundance p of combinations that give rise to a gate realization with a minimal fitness F_{min}. Panel a shows results for the simulated device of Fig. 2 at 77 K and panel b shows equivalent results for an experimental device (same data as underlying Extended Data Fig. 3b of Ref. [8], for consistency analysed in exactly the same way as the simulated data). We find a very good global agreement between simulation and experiment, showing that in both cases the abundance of realizations of the XNOR and XOR gates for a certain minimal fitness is considerably less (by an order of magnitude or more) than that of the AND, OR, NAND, and NOR gates. The decay in abundance with increasing F_{min} can both in the simulations and experiment be empirically approximated by a power law, indicated by the dashed line. We also observe some differences between the simulations and experiment. For example, the abundance of XOR and XNOR realizations is in experiment larger than in the simulations. Also, in experiment the AND, OR, and NOR gates have comparable abundances, which are larger than the abundance of the NAND gate, while in the simulations the NAND and NOR gate have comparable abundances. These differences appear to be systematic, because they also occur for another simulated device; see Fig. S8 in Supplementary Note 8. They can possibly be attributed to the different choice of the input and control electrodes. In the experimental realization the input electrodes are adjacent [8], while in the simulations they are separated by a control electrode.

The inset in Fig. 5a shows similar simulated results as in the main panel, but at room temperature (293 K). XNOR and XOR gates with reasonable fitness are now quite rare, which we attribute to the difficulty of realizing NDR at a higher temperature. NDR is presumably based on blocking mechanisms in the current by an increase of V_{in1} or V_{in2}, where, for example, a charge is moved to a position where it blocks the current. Blocking mechanisms are expected to be more effective at low than at high temperature, where thermal activation is more likely to lift a blocking configuration of charges. The decrease

in gate abundances with increasing $F_{\min}$ is at room temperature also much steeper than at 77 K, which is clear from the much more negative power-law exponent of -7 of the dashed line that now roughly describes the decrease. We conclude that the realization of Boolean logic with the present devices is at room temperature more challenging than at 77 K. In experiment, room-temperature Boolean functionality could be obtained by applying a high voltage (12 V) on a backgate, although with lower gate fitnesses than at 77 K [8] due to an increased signal-to-noise ratio. The room-temperature functionality was explained in Ref. [8] by a suppression of band conduction by the electric field induced by the backgate voltage. Our simulations offer the possibility to investigate the precise conditions required for reliable room-temperature functionality.

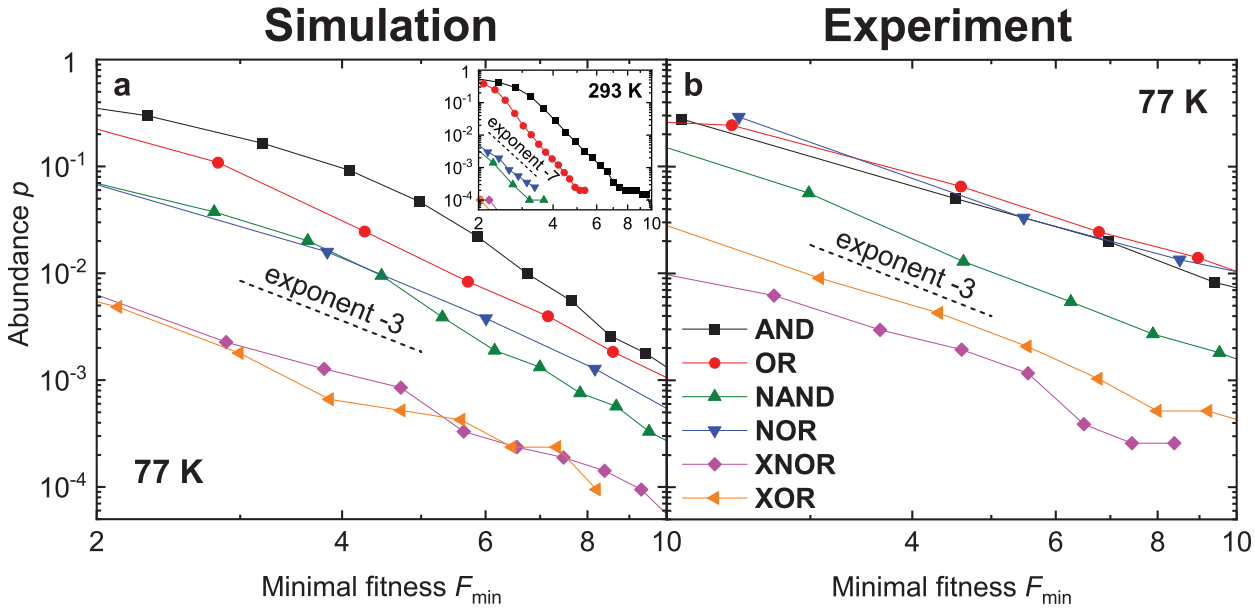


Figure 5. **Boolean gate abundances.** **a**, Main panel: abundance p at 77 K of the six basic Boolean gates with fitness larger than $F_{\min}$ among about 20,000 random combinations of the control voltages V_{c1}–V_{c5} of the simulated device in Fig. 2. Fitnesses were obtained from simulations of 10^7 KMC steps for each control voltage combination. Dashed line: power law with exponent -3. Inset: same as main panel, but at 293 K (room temperature). Dashed line: power law with exponent -7. **b**, Same as main panel in a but for the experimental device in Ref. [8], with results from about 10,000 random control voltage combinations.

To further investigate the differences in abundance and character between the AND and XOR gates – as representatives of gates solving a linearly separable and inseparable problem,

respectively – we introduce the volume V_0 of a gate realization in the five-dimensional (5D) hypercubic phase space of all possible control voltages V_{c1}–V_{c5} in the interval [−1,1] V. This phase space has a total volume $V_{tot} = 2^5$ V^5. We again choose random control voltages, but now restricted to a local hypercube $[V_{c1}^{min}, V_{c1}^{max}] \times \cdots \times [V_{c5}^{min}, V_{c5}^{max}]$, with volume ΔV, centered around the set of control voltages found by artificial evolution of the gate realizations in Fig. 2. We calculate the local probability p_0 that a combination of control voltages leads to a minimal gate fitness F_{min} from 10^4 random combinations chosen in this local hypercube. We then define $V_0 \equiv p_0 \Delta V$ as the local volume in phase space of this particular gate realization. From the gate abundance (global probability) p in Fig. 5a we obtain an estimate of the global volume V of all gate realizations with minimal fitness F_{min} as $V = pV_{tot}$. An estimate of the number of distinct gate realizations with minimal fitness F_{min} in phase space is then found as the ratio between the global volume of all gate realizations and the local volume of a particular gate realization: $N_{gates} = V/V_0$. The local hypercube should be chosen (1) large enough to contain all control voltage combinations leading to a minimal fitness close to the combinations found by artificial evolution, but at the same time (2) small enough to avoid overlap with other distinct gate realizations. Condition (1) is fulfilled by making sure that at the edges of the local hypercube the gate fitness has decreased well below the chosen F_{min}, implying $p_0 \ll 1$. Condition (2) is fulfilled by making sure that $V_{tot}/\Delta V \gg N_{gates}$. We find that with relative local hypercube volumes $\Delta V/V_{tot} = 5.6 \times 10^{-3}$ and 3.6×10^{-3} both conditions are fulfilled for the AND gate the XOR gate, respectively, for the considered values of F_{min}.

Table I gives the quantities discussed in the previous paragraph for the device of Fig. 2 for realizations of the AND and XOR gate at 77 K. For the AND gate we have chosen $F_{min} = 10$ as a criterion for a sufficiently 'good' gate (as a reference, the fitness of the AND gate of Fig. 2 is $F = 34.7$). We find that for the present device an estimated number of 7 distinct AND gate realizations are present for this value of F_{min}. We saw in the previous subsection that for the XOR gate it is more difficult to obtain high fitness realizations and therefore we considered, next to $F_{min} = 10$ (the fitness of the XOR gate of Fig. 2 is $F = 18.0$), also $F_{min} = 5$, which is a still practically acceptable fitness value. The table shows that for $F_{min} = 10$ the volume V_0 of a XOR gate realization is about two orders of magnitude lower than that of an AND gate realization, which shows that for the XOR gate more subtle tuning of the control voltages is required than for the AND gate. This is in

Table I. Estimated local probability p_0, relative local volume $V_0/V_{\rm tot}$, relative global volume $p = V/V_{\rm tot}$, and number of distinct realizations $N_{\rm gates}$ of AND and XOR gates with a minimal fitness $F_{\rm min}$ in the phase space of control voltages $V_{\rm c1}$–$V_{\rm c5}$ in the interval [−1,1] V, for the device of Fig. 2 at 77 K. The gate abundance (global probability) p is estimated from Fig. 5a, using the empirical power law for an extrapolation to $F_{\rm min} = 10$ in case of the XOR gate. The chosen relative local volume $\Delta V/V_{\rm tot}$ and its inverse are indicated. The results are obtained from 10^7 KMC steps for each combination of control voltages.

Gate	$\Delta V/V_{\rm tot}$	$V_{\rm tot}/\Delta V$	$F_{\rm min}$	$p_0 = V_0/\Delta V$	$V_0/V_{\rm tot}$	$p = V/V_{\rm tot}$	$N_{\rm gates} = V/V_0$
AND	5.6×10^{-3}	179	10	4.8×10^{-2}	2.7×10^{-4}	2×10^{-3}	7
XOR	3.6×10^{-3}	278	5	8.5×10^{-3}	3.1×10^{-5}	4×10^{-4}	13
			10	1.2×10^{-3}	4.3×10^{-6}	7×10^{-5}	16

accordance with the narrower peak in the main panel of Fig. 4d as compared to Fig. 4b. By contrast, the estimated number of distinct realizations $N_{\rm gates}$ of the XOR gate is of comparable magnitude, namely about 16 for $F_{\rm min} = 10$ as compared to about 7 for the AND gate. The smaller abundance of the XOR gate as compared to the AND gate is thus not due to a smaller number of distinct gate realizations in phase space but due to a much smaller phase space volume of a distinct realization. Remarkably, the number $N_{\rm gates}$ of distinct XOR gate realizations is not very different for $F_{\rm min} = 5$ and 10 (13 and 16, respectively), showing that the strong decrease of the abundance p with fitness in Fig. 5 is not due to a decrease of distinct XOR gate realizations but due to a strong decrease in the phase space volume of a distinct realization. These observations are crucial for the further development of DNPU technology.

DISCUSSION

We have presented an atomic-scale mechanism for reconfigurable logic in dopant network processing units (DNPUs) in silicon that is based on variable-range hopping (VRH) of interacting charge carriers. Kinetic Monte Carlo (KMC) simulations of the hopping process demonstrate the flexibility, complexity, and non-linearity of the devices necessary for their

reconfigurability and ability to solve linearly separable as well as inseparable problems. We demonstrated artificial evolution of the six basic logic Boolean gates at 77 K, where control voltages serve as genes and the current at an output electrode changes with the voltages applied to two input electrodes according to the specific Boolean logic. The simulated gates show a striking agreement with experiment. The simulations provide a unique visualization of the voltage and current distributions in the devices, revealing an intricate operation mechanism. The simulated abundances of gates of a certain minimal fitness also agree well with experiment, with much higher abundances of the AND, OR, NOR, and NAND gates, solving linearly separable problems, than the XOR and XNOR gates, solving linearly inseparable problems. The smaller abundance of the XOR gate as compared to the AND gate was shown not to be due to a smaller number of distinct gate realizations but due to a smaller volume of a distinct realization in the 5D phase space of control voltages.

The first goal of this work was to underpin the experimental observations on the DNPUs and unravel the mechanism behind their reconfigurable logic. After having achieved this goal, we can now use the gained insights into this mechanism in the development of a mature DNPU technology. We have found, for example, that the output currents of the Boolean gates are relatively small, which makes signal propagation in networks of coupled DNPUs challenging. The simulations pioneered in this work can help to develop strategies to avoid signal propagation losses, e.g., by increasing input impedances to reduce ohmic losses. Furthermore, the conditions necessary for reliable room-temperature operation can now be systematically studied. The simulations also allow studying the effects of different dopant concentrations, mixing of dopants with very different ionization energies to stimulate the occurrence of negative differential resistance (NDR, required for solving linearly inseparable problems), and further miniaturization of DNPUs.

We finally stress the fundamental aspects of our work. VRH is a widely studied charge transport mechanism occurring in a very broad range of, inorganic and organic, disordered material systems. Existing studies have so far almost exclusively focused on bulk systems. Our study has focused on VRH at the nanoscale, where it leads to, in this context, unexplored phenomena, like NDR (see the XOR and XNOR gates in Fig. 2) and percolation effects at the nanoscale (see the current patterns in Fig. 3). Moreover, we have demonstrated the exploitation of the resulting physical behaviour for computing. To our knowledge, this is the first time that VRH modelling has focused on this regime. Our modelling has illustrated

the possibility to realize unconventional computing based on VRH in a network of dopants in silicon, but it should be applicable to many other materials and device geometries. For example, VRH has been shown to be the charge transport mechanism in the disordered conducting polymer mixture poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) [19]. Using drops of PEDOT:PSS instead of dopant networks in silicon could lead to more easily manufacturable nanoscale devices for reconfigurable logic with possibly superior properties.

METHODS

Device simulations

We solve the two-dimensional (2D) Laplace equation for the electrostatic potential on a dense triangular mesh in the device plane, using a finite element method adapted from the MFEM library [20]. This defines the static external potential in which the charge hopping takes place. Electrons hop from an ionized B atom i to a neutral B atom j, separated by a distance r_{ij}, by phonon-mediated VRH, with a Miller-Abrahams (MA) rate $\Gamma_{ij} = \nu_0 \exp\left(-2r_{ij}/a - \Delta E_{ij}/k_\mathrm{B}T\right)$ if $\Delta E_{ij} > 0$ and $\Gamma_{ij} = \nu_0 \exp\left(-2r_{ij}/a\right)$ otherwise [13]. Here, ΔE_{ij} is the energy change when the electron hops and $k_\mathrm{B}T$ is the thermal energy. The energy consists of the electrostatic energy of the electrons in the external potential created by the electrodes (see above) and the ionized counterdopants, the mutual Coulomb energy of the electrons, and a random contribution to the dopant ionization energy drawn from a Gaussian distribution with standard deviation σ. The MA rate has been derived for electron hopping between dopants in semiconductors and should thus be applicable to our system. For simplicity, we also take the MA rate to describe electron hopping between the electrodes and the B dopants. For r_{ij} we then take the distance between the dopant and the center of the electrode, representing the electrode tip in the actual experiment [8]. The electrodes are treated as infinite reservoirs of electrons. We use an effective relative dielectric constant $\epsilon_\mathrm{r} = 6$ in the Coulomb interaction between the charges, which is in between the value of 11.7 for bulk silicon and the vacuum value of 1, reflecting the decreased dielectric screening at the Si surface. We take the typical value $a = 10$ nm for the wave function decay length. We verified that other reasonable values for ϵ_r and a lead to very comparable results. For the

hopping prefactor we take a typical phonon frequency of $\nu_0 = 10^{12}$ s^{-1}, which determines the absolute current scale.

We use a standard, in-house developed rejection-free KMC algorithm that considers at each step all possible electron hops in the system. Voltages are applied to seven electrodes and the current is determined at a chosen grounded output electrode by counting the net number of electron hops to or from that electrode in a certain time interval. Starting with as many electrons in the system as counterdopants (neutral system), 10^4 KMC equilibration steps are sufficient to reach a steady state current for all considered voltage combinations. Unless stated otherwise, we determine the current in a time interval corresponding to 10^7 KMC steps and estimate the statistical uncertainty in the current from the current fluctuations in 100 equally long subintervals.

Artificial evolution of Boolean gates

The six basic Boolean gates in Fig. 2 are found by artificial evolution, where the control voltages $V_{\rm c1}$–$V_{\rm c5}$ are the 'genes' that are evolved to optimize a fitness $\widetilde{F} = F_0 - 2u_F$, where

$$F_0 = 1 - \frac{1}{4}\sum_{V_{\rm in1},V_{\rm in2}} \left| G(V_{\rm in1},V_{\rm in2}) - \frac{I_{\rm out}(V_{\rm in1},V_{\rm in2}) - I_{\rm out}^{\rm min}}{I_{\rm out}^{\rm max} - I_{\rm out}^{\rm min}} \right| + 0.05\frac{I_{\rm out}^{\rm max} - I_{\rm out}^{\rm min}}{\max(|I_{\rm out}^{\rm max}|,|I_{\rm out}^{\rm min}|)}, \quad (1)$$

with

$$\begin{aligned} I_{\rm out}^{\rm max} &\equiv \max_{V_{\rm in1},V_{\rm in2}} I_{\rm out}(V_{\rm in1},V_{\rm in2}), \\ I_{\rm out}^{\rm min} &\equiv \min_{V_{\rm in1},V_{\rm in2}} I_{\rm out}(V_{\rm in1},V_{\rm in2}). \end{aligned} \quad (2)$$

Here, $G(V_{\rm in1},V_{\rm in2}) \in \{0,1\}$ is the output of the logic gate searched for and u_F is the statistical uncertainty in F_0, which follows from the individual statistical uncertainties in the four currents $I_{\rm out}(V_{\rm in1},V_{\rm in2})$, where $V_{\rm in1}$ and $V_{\rm in1}$ can be either 0 or 0.5 V. By subtracting $2u_F$ from F_0 we avoid spurious high fitnesses occurring as a result of statistical fluctuations in the current. The following genetic algorithm is used in the artificial evolution of each gate:

1. **Initial generation**

   The initial generation of 'genomes' consists of 25 control voltage combinations $V_{\rm c1}$–$V_{\rm c5}$, randomly generated from a uniform distribution on the interval [−1,1] V.

2. **Evaluate fitness**

   For each genome and each input voltage combination, the four currents and their

uncertainties are obtained from KMC simulations with a variable number of steps (see below), after an equilibration of 10^4 KMC steps. The fitness $\widetilde{F} = F_0 - 2u_F$ is evaluated for each genome. The genomes G_k^l ($k = 1, \ldots 25$) of a generation l are ordered according to decreasing fitness.

3. **Next generation**

   A new generation of 25 genomes G_k^{l+1} is generated in the following way:

   - **Genome 1-5:** The five fittest genomes of the previous generation: $G_1^{l+1} = G_1^l, \ldots, G_5^{l+1} = G_5^l$.
   - **Genome 6-10:** The five fittest genomes of the previous generation, with slightly adjusted control voltages (genes), randomly chosen from the interval $[V_{ci}(G_k^l) - 0.05V, V_{ci}(G_k^l) + 0.05V]$, where $V_{ci}(G_k^l)$ is the previous control voltage (gene). This allows random exploration in the vicinity of the current elite genomes.
   - **Genome 11-15:** The next five genomes are generated by performing crossover between the fittest and next fittest genome with a 50% chance. If the control voltages of G_1^l are $V_{c1}(G_1^l), \ldots, V_{c5}(G_1^l)$ then $V_{ci}(G_{11}^{l+1})$ is either $V_{ci}(G_1^l)$ or $V_{ci}(G_2^l)$, both with 50% probability. Similarly, $V_{ci}(G_{12}^{l+1})$ is either $V_{ci}(G_2^l)$ or $V_{ci}(G_3^l)$, both with 50% probability, etc.
   - **Genome 16-20:** The next five genomes are generated by performing crossover between the five fittest five genomes and five random genomes. So, G_{16}^{l+1}, for instance, is a crossover between G_1^l and a random genome.
   - **Genome 21-25:** The last five genomes are completely randomly generated.

   Additionally, each gene (control voltage) has a 10% chance of mutating. If a gene mutates, its new value is drawn from a triangular distribution between -1 and 1 V around its old value.

4. **Iterate until convergence**

   Repeat step 2 and 3 until a sufficiently high fitness value is obtained.

For a randomly chosen initial generation and for a given gate the genetic algorithm was run for a fixed CPU time (of the order of one week on 8 threads). Initially, the current was determined from 10^5 KMC steps. To reduce the statistical uncertainty in the current, the

number of KMC steps was doubled as soon as $F_0 + u_F > 1$ for the best gate during the artificial evolution. This doubling was applied for a maximum of ten times. Each run was repeated 20 times with different initial conditions. Finally, based on these runs for each gate the realization of control voltages, yielding a particular high fitness value, was selected for Fig. 2. To obtain the actually shown currents and uncertainties in Fig. 2 for these control voltages, an additional KMC simulation with 10^7 steps was performed after an equilibration of 10^4 steps. Figure 2 shows the currents for the best gates found after the 20 runs of the genetic algorithm. The shown currents and their error bars were obtained for each gate by a final KMC simulation with 10^7 KMC steps using the found optimal control voltages, after 10^4 equilibration steps.

The fitness function F used in the final analysis of the results is similar to that of Refs. [8] and [10], and is defined as

$$F = \frac{m}{\sqrt{r_{ss}} + k|C|}, \tag{3}$$

where m and C are fit parameters of a linear fit $I_{\text{out}}(V_{\text{in1}}, V_{\text{in2}}) = mG(V_{\text{in1}}, V_{\text{in2}}) + C$. Here, r_{ss} is the mean squared error of the linear regression. The constant k is set to 0.01, as in the experiments [8, 10]. A finite value of k awards a large relative separation of the high and the low current levels, which is relevant for the experimental separation of these levels. This is achieved when the ratio of m and $|C|$ is large.

DATA AVAILABILITY

Data supporting this publication are available from the corresponding authors upon reasonable request.

CODE AVAILABILITY

The kinetic Monte Carlo code used in this work is available at https://github.com/MUTUEL.

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AUTHOR CONTRIBUTIONS

The project was conceived and planned by P.A.B., A.H., B.J.G. and W.G.v.d.W. The used KMC code was developed by B.d.W., M.B. and I.K. The final calculations with this code that are the basis of the paper were performed by H.T. and J.B. The writing of this paper

was coordinated by P.A.B. All authors contributed to the results of this work and the final version of the paper.

COMPETING INTERESTS

The authors declare no competing interest.

ADDITIONAL INFORMATION

Supplementary information. The online version contains supplementary material available at xxx.

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