Reliability and Power Analysis of FinFET Based SRAM

Alluri Navaneetha (✉ neethaalluri@gmail.com)

Mahatma Gandhi Institute of Technology

K. Bikshalu

Kakatiya University

Research Article

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Abstract

Demand for accommodating more and new functionalities within a single chip such as SOC needs a novel devices and architecture such as FinFET device instead of MOSFET. FinFET is emerged as non-planar, multigate device to overcome short channel effects such as subthreshold swing deterioration, drain induced barrier lowering, threshold voltage roll off which degrade circuit performance. As the need of device technology is mounting in electronic gadgets the important parameters are taken into consideration such as low leakage, high reliability, low power dissipation, and high operating speed. Reliability is one of key considerations in converting a proof of concept into reality. In this work Reliability of FinFET device is studied experimentally according to ITRS (international technology roadmap for semiconductor) roadmap using several standard test protocols such as multiple current stressing, harsher environment conditions, and effect of electromigration. Furthermore, power analysis of FinFET based SRAM is done by using 7nm bsimcmg PTM files in mentor graphics tool. The FinFET based SRAM shown low leakage, power dissipation, delay compared to existing conventional MOSFET based SRAM.

1. Introduction

Electronic devices are in high demand in the electronics sector and are utilized in a variety of applications including automobiles, computing, communications, entertainment, artificial intelligence, neural networks, computer vision, big data, and many others [1], in which advanced nanodevice FinFET is used as a transistor instead of MOSFET to achieve high performance, low power dissipation, low area at reduced technology. Channel electrostatics is controlled by single gate MOSFET whereas control of channel in 3 directions to reduce short channel effects is achieved by 3 gate FinFET [2, 3] For digital circuit, Mixed signal circuit, Analog/RF circuit, FinFET is emerged as superior device to get low power dissipation, high speed, low area at deep submicron range. FinFET can be fabricated in 2 ways one is SOI (silicon on insulator) and alternatively as BULK. Due to the presence of an insulating layer beneath oxide, SOI FinFETs with lower parasitic capacitance increases switching speed and reduces power consumption [4]. RF characteristics, Linearity, is achieved by spacer dielectric optimization.

For nanoscale applications reduction of leakage is required which in turn reduces and improves system performance [4]. FinFET has well established structure and fabrication due to this TSMC and Intel manufacturing Industries made used from 2011 to till date at sub 22nm technology nodes [5]. SOI FinFET shows reduced device cross talk, lower junction leakage, fully dielectric isolation, lower junction leakage, reduced capacitance, nearly ideal subthreshold slope [6–8]. FinFET reduces short channel effects by wrapping gate over channel from four sides. Due to continuous scaling FinFET faces several challenges in terms of cost effective, patterning, layout, device performance [9–12]. Due to several advantages FinFET can be used in variety of application such as terrestrial systems, infrared detectors, space, satellite communication, nuclear reactor, military [12–13].

2. Reliability Study Of Finfet

One of the most important factors to consider when turning a proof of concept into reality is reliability. It is critical to investigate the dependability of these surface passivation methods in more depth. The specific contact resistance is the most important factor in determining reliability. Under any adversity, the resistance values should not change dramatically. The ITRS (International Technology Roadmap for Semiconductors) developed a number of typical test techniques to ensure reliability. Multiple current stressing is a test that involves repeatedly passing a variable current of quite high amplitude through a test structure. There will be no major performance decrease in a trustworthy framework. Temperature cycling is another more rigorous reliability test that is performed on a regular basis. Repeating the numerous current stressing measurements at different temperatures is part of the experiment. -55°C to $+125^{\circ}\text{C}$ is the standard temperature range. In order to ensure reliability, the test structure should be able to withstand these circumstances without degrading. Last but not least, the test structure should be exposed to a harsher environment to account for variability caused by differing storage circumstances. Over a lengthy period of time, the test structure is normally maintained in a high relative humidity environment (usually $\text{RH} > 60\%$) and at a high temperature ($> 100^{\circ}\text{C}$) (typically a week or more). To ensure trustworthiness, the repeat measurements should resemble those of the original measurements.

Preparation of the substrate, Fin etch, oxide deposition, planarization, recess etch, gate oxide deposition, and ultimately gate deposition was used in the fabrication of the FinFET device. Figure 1 shows the TEM cross section of the fabricated FinFET device at 22nm CMOS technology node, whereas Fig. 2 shows the corresponding 3D FinFET device structure in Sentaurus Tcad simulation domain.

Prior to go for reliability studies, fabricated FinFET device bonded with feeder lines (M1, M2) at low temperature (160°C) and low pressure (2.5 mbar) for Kelvin structure design [18], process flow is explained below. Figure 3 shows the cross-sectional TEM of bonded region of the feeder lines. Figure 4 shows the complete experimental process flow of reliability study of FinFET device.

2.1. Reliability assessment of the Fabricated FinFET using Multiple Current Stressing test

For applications such as high-speed super-fast multi-core processor design, the electrical performance of the FinFET device is critical, especially when numerous operations are performed. As a result, the constructed Kelvin structure along with FinFET device (with M1,M2 feeders) was treated to 1000 cycles of current stress with magnitudes ranging from -0.1 A to $+0.1\text{ A}$. At room temperature, all measurements were made with a Keithley source measuring unit. Each 100 cycles, the specific resistance was measured.

2.2. Reliability assessment of the fabricated FinFET device using Temperature Cycling Test

The thermal stability test, as per the JESD22-A104B standard, involves subjecting the FinFET device through feeder to 1000 cycles of current sweeping from -0.1 A to $+0.1\text{ A}$ at various temperatures ranging from -55°C to $+125^{\circ}\text{C}$. The resistance behavior of a FinFET device specimen pre and post temperature

cycles is shown in Fig. 6. It can be inferred from the figure that even at very high and very low temperature the fabricated FinFET device is reliable and there is no deprivation of the specific resistance. As a result, FinFET devices may be viable and efficient at both high and low temperatures.

2.3. Reliability assessment of the Fabricated FinFET structure under harsher environment conditions

The specimens were maintained under harsher environment circumstances for 96 hours, with a high relative humidity (RH) of 65 percent and a high temperature of 130°C, in order to investigate the effect of tougher environmental condition on the produced FinFET. The data taken after this storage correlate extremely well to the ones taken before this retention, as shown in Fig. 7. After such a lengthy period of exposure to harsher environmental results, it is clear that the unique resistance of both CMOS technology situations has not degraded. This shows that FinFET devices produced utilizing both CMOS and CMOS technology is more resistant to dampness and high temperatures.

2.4. Electromigration Assessment of the FinFET device post bonding

During an EM test, four-point sensing is used to evaluate electrical resistance. As shown in Fig. 8, resistance measurements taken during EM testing demonstrate a latency period during which the resistance remains unchanged, followed by a gradual and then rapid increase.

3. Static Random Access Memory (Sram)

Cache memory which is made of SRAM cell [9-11] occupies 50% of area in processor the leakage power due to cache memory in processor is the major source of power dissipation [12]. Now a days SRAM is operating in nanometer range in electronic gadgets so, the power dissipation in SRAM should be as low as possible in which leakage currents has to be less and speed should be more. Low power dissipation and more speed in SRAM is obtained by using advanced devices such as FinFET instead of MOSFET. To meet technology scaling new structure challenges have been proposed such as FinFET and Nanowire [13]. FinFET device attracted many SRAM designer's as FinFET has superior short channel effects, reduced dopant fluctuations, independent gating, better subthreshold slope [13,14]. From device level to architecture level many FinFET based SRAM cells have been proposed [15-17]. The trend of SRAM along with CMOS technology scaling in different processors and SOC products has fuelled the need of innovation in the area of SRAM design. Simulation results are carried out for 7nm FinFET based SRAM to analyze the parameters for leakage power, delay and power dissipation which is compared with existing MOSFET device. 7nm FinFET based SRAM shown less leakage, low power, high speed compared to the existing MOSFET based SRAM device as shown in comparison table (Table-1). Schematic diagram of simulated FinFET based SRAM and simulation result shown in Fig. 9 and Fig. 10 respectively.

Table 1. Comparison of parameters of 7nm FinFET based SRAM along with conventional MOSFET based SRAM.

Parameter	MOSFET		FinFET	
Mode	Write	Read	Write	Read
Technology	180nm	180nm	7nm	7nm
Delay	143ps	974ps	96ps	603ps
Leakage power	286nW	793nW	1.6nW	1.98nW
Power Dissipation	1.50nW	618pW	787pW	397pW

Conclusion

Reliability assessment of the experimental FinFET device under 7nm and 22nm is demonstrated under various tests such as temperature cycling test, harsher environment condition, multiple current stress, the results shown that the device structure above to withstand under any circumstances without degrading to ensure reliability. The most important component to decrease or increase performance of system is SRAM memory which is used as cache memory in multiprocessor chip, requires low power dissipation, low leakages, high speed for the future IOT devices which connects nearly \$50 billion devices in future. Analysis of leakage and power of SRAM is done using 7nm bsimcmg FinFET file in Mentor Graphic tool which show low power dissipation and high speed compared to the existing MOSFET at high technology node.

Declarations

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Figures

Figure 1

Cross-sectional TEM image of fabricated FinFET at 22nm CMOS technology node.

Figure 2

3D structure of simulated FinFET Device.

Figure 3

Bonded feeder lines for voltage and current feeding.

Figure 4

Process Flow of reliability analysis of fabricated FinFET device.

Figure 5

Electrical performance assessment using multiple current stress. Even after 1000 cycles of current straining, no decrease of contact resistance was found as shown in Fig. 5, indicating that the constructed FinFET device is trustworthy.

Figure 6

Electrical performance of Fabricated FinFET structure under temperature cycling test.

Figure 7

Electrical performance evaluation of the fabricated FinFET device at harsher environment condition.

Figure 8

Relative degradation plot of FinFET device under EM test.

Figure 9

Schematic of FinFET based SRAM

Figure 10

Simulation results of FinFET based SRAM