Leakage Mitigation in NW FET using Negative Schottky Junction Drain and its Process Variation Analysis

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Abstract—In this work, a Schottky junction on the drain side employing low workfunction (WF) metal is proposed as a method to suppress the OFF-state leakage in nanowire (NW) field-effect transistor (FET). Instead of a highly n+ doped drain, low WF metal with negative electron Schottky-barrier height (SBH) as a drain minimizes the lateral band-to-band tunneling (L-BTBT) considerably. L-BTBT is the movement of carriers (holes) from the drain conduction band (CB) into the channel valence band (VB) during the OFF-state. Impact of varying WF at channel-drain junction on the device characteristics is studied. It is observed that $SBH \leq 0$ eV is required to mitigate L-BTBT compared to the conventionally-doped and junctionless (JL) NW counterpart. Furthermore, unlike L-BTBT, leakage in NW Schottky-drain (SD) comprises of holes tunneling through the SB from the metal drain into the channel and termed as the lateral SB tunneling (L-SBT). In contrast to JL NW FET, the process variation immunity (varying channel doping, N_{Ch} and NW diameter, d_{NW}) and the ON-state current of the proposed device is not compromised at the expense of lower OFF-state L-SBT. Instead, the device is less susceptible to process variations and retains the ON-state performance of the NW MOSFET. For a $\pm 20\%$ change in N_{Ch} , $\Delta I_{OFF}/I_{OFF}$ of 7% compared to 97% in NW JL FET is observed.

Index Terms—Junctionless (JL), Nanowire (NW), Schottky-barrier height (SBH)

I. INTRODUCTION

Until now, low drive current due to band-to-band (BTBT) tunneling mechanism in Tunnel FET has hampered the replacement of MOSFETs in low power circuits [1]–[3]. Additionally, traps induced non-idealities at source/channel interface and gate/oxide interface further exacerbates the TFET performance [4]–[6]. Even though multiple TFET architectures in the form of lateral and vertical tunneling device exists, none of them have been promising enough to facilitate future MOSFET replacement [7]–[14].

In contrast, nanowire (NW) configurations in MOSFET research space are emerging out to be a possible candidate

for scaling in the sub-10-nm regime [15]–[17]. Gate-all-around (GAA) configuration is shown to have a better electrostatic integrity with suppressed short-channel effects (SCEs) in comparison to the planar and FinFET architecture [18]–[20]. GAA architecture, however, has its own disadvantage of considerable band overlap between the channel valence band (VB) and the drain conduction band (CB) due to the tight gate control. This occurs due to higher electric field at the channel-drain junction in the OFF-state, which in turn, facilitates the lateral band-to-band tunneling (L-BTBT) of electrons from the channel VB to the drain CB in case of n-channel NW MOSFETs [15]–[17].

In addition, at ultra-short gate lengths, recently, it is also observed that the realization of junctions with high doping gradient is a challenging task in NW MOSFETs. Thus, to overcome this junction constraint problem, junctionless (JL) FET with uniform device layer doping is proposed and fabricated [21]. Typically, to have an efficient gate control facilitating OFF-state volume depletion, source/channel/drain doping in n-NW JL FETs is of around $\sim 1 \times 10^{19} \text{cm}^{-3}$. Unlike NW MOSFET, the absence of a sharp channel-drain junction in NW JL FET results in lower L-BTBT; however, at the expense of smaller ON-current [15], [16]. Low drive current due to the increased device layer resistance originates from the controlled device layer doping in JL structure. Hence, it is inferred that NW JL FET cannot simultaneously, retain the advantage of suppressed L-BTBT in addition to drive current capacity of NW MOSFET [21]–[24].

Another major problem with the JL architecture is the increased threshold (V_{th}) variability due to the high channel doping. A lot of fabricated and simulated results have validated this effect which needs immediate rectification [25]–[28]. To resolve the aforementioned issues, NW JL accumulation mode FET (NW JAM FET) is also proposed, wherein, source/drain (S/D) are additionally ion-implanted while channel doping is more controlled compared to the JL architecture [15], [16]. This allows for higher channel mobility with reduced S/D resistance. However, the advantage is not without a trade off. It is observed that L-BTBT is more in NW JAM FET compared to the JL counterpart. Another reason to control L-BTBT at the channel-drain junction is the formation of bipolar junction transistor (BJT), in the OFF-state, as explained in detail in [15], [16], [24]. The holes are accumulated in the channel region due to L-BTBT which makes the channel p-type. Following this, source, channel, drain regions start to

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TABLE I
DEVICE SIMULATION PARAMETERS AND THEIR VALUES

Parameters	NW MOSFET	NW JL FET	NW SD FET
Gate length (L_g)	20 nm	20 nm	20 nm
EOT	1 nm	1 nm	1 nm
NW diameter (d_{NW})	5-10 nm	5-10 nm	5-10 nm
N_{Sext} doping (N_D), cm^{-3}	1×10^{20}	1.5×10^{19}	1×10^{20}
N_{Dext} doping (N_D), cm^{-3}	1×10^{20}	1.5×10^{19}	-
N_{Ch} doping (N_A), cm^{-3}	1×10^{17}	-	1×10^{17}
N_{Ch} doping (N_D), cm^{-3}	-	1.5×10^{19}	-
Gate workfunction	4.5 eV	4.73 eV	4.5 eV
Channel-drain SBH	-	-	0-0.6 eV
S/D extension, (L_{ext})	50 nm	50 nm	50 nm
Supply voltage (V_{DD})	1V	1V	1V

Fig. 2. Calibration of model parameters from transfer characteristic of [22]. Additionally, non-local tunneling parameters ($m_e = 0.4m_0$, $m_h = 0.65m_0$) along with the density of states ($g_c = 2.1$, $g_v = 0.66$) parameters are taken from [15], [16] to correctly account for the lateral tunneling in all three devices.

act as emitter, base, and collector of a virtual BJT. This, in turn, significantly increases the OFF-state leakage in NW MOSFETs.

To overcome the L-BTBT problem and simultaneously retains the advantage of higher ON-state current of NW MOSFET with better process variation immunity, the present work proposes a NW FET architecture employing a low workfunction metal drain. It is observed that the possibility of tuning Schottky-barrier height (SBH) at the channel-drain junction facilitates the suppression of L-BTBT. Furthermore, unlike NW JL FET, ON-state current is not compromised for $SBH \leq 0$ eV and is at par with the NW MOSFET.

Section II presents the 3D device schematic, cross-sectional view of the various NW configurations, alongside the device parameters and simulation approach to capture the L-BTBT. Section III discusses the proposed device process immunity pertaining to d_{NW} scaling and N_{Ch} doping and spacer permittivity variation. Impact of the variation in drain WF is also analyzed. Finally, the paper is concluded in Section IV.

II. DEVICE STRUCTURE AND SIMULATION APPROACH

Fig. 1(a)-(c) shows a 3D view alongside cross-sectional schematic of the NW MOSFET, NW JL FET and the proposed NW SD FET. Also, 2D cross-sectional view represents the doping used in the thin Si NW for various devices. Except for the NW JL FET, the other two structures have an abrupt S/D junction, considered for the worst case scenario of L-BTBT. This is confirmed with the lesser L-BTBT in JL architecture wherein it is observed that the absence of sharp doping gradient at channel-drain junction increases the tunnel barrier width. No gate-drain overlap/underlap and air ($\kappa = 1$) as the default spacer is assumed for all three NW configurations. A suitable gate workfunction of 4.5 eV is used for both the NW MOSFET and the NW SD FET, since they fall into the category of inversion-mode (IM) devices. However, for NW JL FET, higher gate workfunction of 4.73 eV is chosen to deplete the channel in the OFF-state. This facilitates proper transistor action keeping the gate overdrive fairly same in all three devices. All other relevant parameters are shown in the table I.

All 3-D simulations were run on the Synopsys Sentaurus simulation tool release J-2014.09 [29]. Philips and Lombardi model to consider doping, concentration and field dependent mobility degradation is activated. Alongside band gap narrowing model for high source/drain doping is also invoked. Shockley-Read-Hall and Auger recombination model in conjunction with drift diffusion physics are also accounted for. To account for the L-BTBT current in NW MOSFET and NW JL FET, calibrated parameters from [22] is activated, as shown in the 2. The calibrated tunneling masses of non local tunneling model provided in [15], [16] are obtained via reproducing the results fabricated in [17], to minimize the discrepancy between the simulated and the experimental results. Furthermore, unlike L-BTBT, leakage in NW SD FET comprises of holes tunneling through the SB from the metal drain into the channel and termed as the lateral SB tunneling (L-SBT). The OFF-state L-SBT tunneling in NW SD FET is taken into account via the same non local tunneling model. In addition, the calibrated tunneling masses (m_e and m_h) are kept the same to model the leakage current fairly in all three devices. High- κ /metal gate stack is assumed and thus the direct gate tunneling leakage is not considered. Furthermore, quantum induced bandgap widening for $d_{NW} \leq 7$ nm is significant and is taken into consideration. For $d_{NW} = 5, 7$ nm, increase in effective bandgap is accounted for by changing the default E_g of the material [15], [16]. Although the tunneling masses are expected to increase at smaller d_{NW} , the incompatible numerical solvers limits the possibility to implement in commercial simulators. And thus, the calibrated tunneling mass is used in all the simulations.

Furthermore, to have a fair comparison between the I_D - V_G characteristics in all three devices, same gate workfunction is chosen for both the IM devices, i.e., NW MOSFET and NW SD FET. However, NW JL FET, not being the inversion mode (IM) device, OFF-state current (at $V_{GS} = 0$ V) and subthreshold slope (SS) for greater part of the curve are

Fig. 1. 3D view and cross-sectional schematic of (a) NW MOSFET, (b) NW JL FET, and (c) NW SD FET. $L_g = 20\text{nm}$. $EOT = 1\text{nm}$.

matched to the NW SD FET by tuning the gate workfunction. The change in OFF-state and ambipolar characteristics for the same gate overdrive can then be appreciated for all three devices. It is noteworthy to mention that for the same gate overdrive, the degradation in the ON-state current is a trade off for the suppressed OFF-state leakage in NW JL FET.

III. RESULTS AND DISCUSSION

Fig. 3(a) compares the I_D - V_G characteristics of the three NW configuration. For the same $d_{NW} = 5\text{ nm}$ and $V_{GS} \leq 0\text{V}$, it can be observed that the NW MOSFET and NW SD FET have higher rate of change of L-BTBT with negative gate bias compared to the JL device, owing to sharp channel-drain junction. However, NW SD FET suppresses the lateral tunneling considerably for drain workfunction of 4.0 eV. More than a order of magnitude reduction in the L-BTBT leakage is observed for the NW SD FET compared to the other two devices at $V_{GS} = -0.2\text{V}$. As can be observed, I_D - V_G variation in NW JL FET is less susceptible to negative gate bias. This is largely due to the absence of sharp metallurgical junction which results in larger tunnel barrier width and thus, minimizes the L-BTBT leakage in NW JL FET, previously reported in [15], [16]. However, the ON-state current ($I_{DS}@ V_{GS} = 1\text{V}$) in such scenario is significantly compromised compared to NW MOSFET, which is not the case with the NW SD FET. Fig 3(b) shows the band diagram of the NW SD FET for negative gate bias of -0.2V . The zoomed-in portion illustrates the presence of negative Schottky barrier height (SBH) at the channel-drain junction for the drain WF of 4.0eV.

The corresponding hole tunneling rate in all three device structures at $V_{DS}=1\text{V}$ and $V_{GS}=-0.2\text{V}$ is shown in the Fig. 3(c). The higher tunneling rate in case of the NW MOSFET and NW JL FET is clearly evident, which further results in the increased leakage compared to the NW SD FET. Fig 4 further compares the drain current values in all three NWs for fixed $V_{DS}=1\text{V}$ and different V_{GS} of 1V, -0.2V and -1V .

TABLE II
 I_{ON}/I_{OFF} RATIO AS A FUNCTION OF NW DIAMETER, d_{NW}

Parameter evaluated	d_{NW} (nm)	NW MOSFET	NW JL FET	NW SD FET
I_{ON}/I_{OFF}	5	3.9×10^5	7.9×10^5	9.6×10^6
	7	5.2×10^4	5.8×10^2	9.2×10^5
	10	1.7×10^3	6.6	1.3×10^4
$\frac{I_{ON}/I_{OFF} _{d_{NW}=5\text{nm}}}{I_{ON}/I_{OFF} _{d_{NW}=10\text{nm}}}$	-	2.2×10^2	1.1×10^5	7.3×10^2

A. Impact of d_{NW} Scaling

Fig.5(a)-(c) compares the I_D - V_G characteristics of three NW configuration as a function of NW diameter, d_{NW} . As shown, more than ~ 3 orders of magnitude change in the I_D - V_G characteristics for negative gate bias is observed for $d_{NW} = 5\text{nm}$ and 7nm (difference shown via the shaded red portion) in case of NW JL FET. For NW MOSFET and NW SD FET, the variation in I_D - V_G characteristics for negative gate bias is less compared to the NW JL FET. Table II compares the corresponding ON-OFF ratio between the three structures for $d_{NW} = 5, 7, 10\text{nm}$. Two observations can be made from the above results. One is the improved current ratio as the d_{NW} is scaled and the other is the better process variation immunity to d_{NW} in NW SD FET. For $d_{NW} = 5\text{nm}$, a $2.5\times$ and $1.2\times$ improved ON-OFF ratio is observed in NW SD FET compared to the NW MOSFET and NW JL FET device, respectively. I_{ON}/I_{OFF} sensitivity is evaluated by defining the parameter $\Delta(I_{ON}/I_{OFF})$ defined as:

$$\Delta(I_{ON}/I_{OFF}) = \frac{I_{ON}/I_{OFF}|_{d_{NW}=5\text{nm}}}{I_{ON}/I_{OFF}|_{d_{NW}=10\text{nm}}} \quad (1)$$

We observe from the table II that it is maximum for the JL device in comparison to the other two, also illustrated by the red shaded area in Fig.5. The observation made here is synonymous with the results demonstrated in [25]–[27], both experimentally and via simulations. It is thus inferred that the

Fig. 3. (a) I_D - V_G characteristics comparison of the NW MOSFET, NW JL FET and NW SD FET for $L_g = 20\text{nm}$ and $d_{NW} = 5\text{nm}$, (b) corresponding band diagrams at $V_{DS} = 1\text{V}$ and $V_{GS} = -0.2\text{V}$ that illustrates the negative SBH at the channel-drain interface Hole tunneling rate in the NW for the same bias in all three devices, showing suppressed leakage in NW SD FET. Drain WF for NW SD FET is 4.0 eV.

process variation immunity is less for the JL device. However, the SD structure shows better immunity to d_{NW} variation similar to that of the NW MOSFET and simultaneously, provides drain WF engineering as a method to lower the L-BTBT.

B. Impact of Channel Doping

Fig 6(a)-(c) compares the I_D - V_G characteristics of three NW configurations for a $\pm 20\%$ change in the channel doping from the standard value, listed in the table I. The curves (red

Fig. 4. Comparison of drain current evaluated in NW MOSFET, NW JL FET and NW SD FET at different V_{GS} of 1V, -0.2V and 1V. $V_{DS} = 1\text{V}$.

Fig. 5. I_D - V_G characteristics of NW MOSFET, NW JL FET, and NW SD FET for NW diameter, d_{NW} values of 5 and 7 nm.

TABLE III
SENSITIVITY TO PROCESS VARIATION IN DIFFERENT NW CONFIGURATIONS

Parameters changed	Parameters evaluated	NW MOSFET	NW JL FET	NW SD FET
N_{Ch} ($\pm 20\%$)	$\Delta I_{ON}/I_{ON}$	0%	8.4%	0%
	$\Delta I_{OFF}/I_{OFF}$	5%	97%	7%
d_{NW} ($+0.5\times$) ($-0.3\times$)	$\Delta I_{ON}/I_{ON}$	$0.95\times$	$1.63\times$	$1.06\times$
	$\Delta I_{OFF}/I_{OFF}$	$4\times$	$117\times$	$12.4\times$
Spacer: $\kappa = 1$ $\downarrow$ $\kappa = 3.9$	$\Delta I_{ON}/I_{ON}$	1.2%	1.6%	0%
	$\Delta I_{OFF}/I_{OFF}$	49%	78%	6.5%

and green) indicate that there is not much variation in NW MOSFET and NW SD FET characteristics unlike NW JL FET, represented by the blue curve. Two parameters defined to measure the impact of change in N_{Ch} are $\Delta I_{OFF}/I_{OFF}$ and

Fig. 6. I_D - V_G characteristics of NW MOSFET, NW JL FET, and NW SD FET for a $\pm 20\%$ change in the channel doping, N_{Ch} . JL device is highly impacted unlike the other two.

Fig. 7. (a) Shows the cross-sectional schematic of the NW SD FET with two different spacers, i.e., air ($\kappa=1$) and SiO_2 ($\kappa=3.9$). (b) Corresponding I_D - V_G characteristics of NW MOSFET, NW JL FET, and NW SD FET structure. NW MOSFET and NW JL FET are more susceptible to spacer permittivity represented by the shaded area (grey and red).

$\Delta I_{ON}/I_{ON}$. Here, ΔI_{ON} (ΔI_{OFF}) is the difference between the I_{ON} (I_{OFF}) observed at $+20\%$ and -20% change from the standard value. For the case of NW MOSFET and NW SD FET, change in I_{ON} is negligible whereas a slight deviation of 5% and 7.8%, respectively, is seen for the I_{OFF} current. However, for NW JL FET, a whopping deviation of 97% is observed in I_{OFF} , whereas the change in I_{ON} is around 8.4%. This simply highlights the disadvantage of JL architecture when it comes to process immunity [25]–[27] during OFF-state performance. Furthermore, in addition to N_{Ch} , we also

tabulated the sensitivity to d_{NW} variation in all three devices, as shown in the table III. For the case of d_{NW} , ΔI_{ON} and ΔI_{OFF} is calculated as the difference in I_{ON} and I_{OFF} values for a change in $+0.5 \times (d_{NW} = 10\text{nm})$ and $-0.3 \times (d_{NW} = 5\text{nm})$ from $d_{NW} = 7\text{nm}$. From the results here, we infer that the NW SD FET is not as susceptible as NW JL FET to process variation and is on par with the NW MOSFET architecture.

C. Impact of Air and SiO_2 Spacers

Fig 7(a) shows schematically the cross-sectional view of NW SD FET with two different spacers, i.e., air ($\kappa=1$) and SiO_2 ($\kappa=3.9$) simulated in this section. The corresponding transfer characteristics for all three NWs with two different spacers is shown in the Fig 7(b)–(d). Two observations can be made here. First, the use of high- κ effectively increases the channel length by depleting the channel of carriers through the fringing gate field. This is observed more in NW JL FET in comparison to the NW MOSFET and NW SD FET, more of which is explained in detail in [23]. Second, the effective increase in the channel length minimizes the leakage and thus for SiO_2 spacer, the leakage for negative gate bias is less both in the NW JL FET and NW MOSFET. However, NW JL FET is more susceptible to spacer variation, as depicted by the shaded curve green area and also reported in the table III by the change in $\Delta I_{OFF}/I_{OFF}$ and $\Delta I_{ON}/I_{ON}$ from reference air spacer to modified SiO_2 spacer. So, we deduce that NW SD FET has better immunity to spacer variation in comparison to another two NWs.

D. Impact of Drain WF Variation

Fig. 8(a) shows the I_D - V_G characteristics of the NW SD FET for different values of drain metal WF. Starting with 3.8eV, WF is varied up to 4.3eV. We observe that as we move towards the lower WF, the SBH at the channel–drain junction becomes negative and suppresses the lateral tunneling of holes from the drain metal into the channel region, as shown by the band diagrams in the Fig. 8(b). For higher WF above 4.0eV, channel–drain SBH becomes positive and relatively large OFF-state leakage is observed. In all cases, the ON-state characteristics is minimally impacted. The advantage of the NW SD FET is that we can tune in the drain metal WF (or SBH) to obtain the desired ON-OFF ratio.

IV. CONCLUSION

In this work, a drain-engineered NW FET with low work-function drain metal is proposed and compared with the existing NW MOSFET and NW JL FET structure for better leakage suppression. The proposed device has Schottky junction at channel-drain interface unlike the chemically doped junction in NW MOSFET and no-junction in NW JL FET. NW SD FET demands negative Schottky barrier height (SBH) at channel-drain junction for effective suppression of lateral holes tunneling from the drain into the channel region during OFF-state. NW SD FET offers better leakage suppression without compromising the ON-state performance as in the case of NW

Fig. 8. I_D - V_G characteristics of NW SD FET (a) for different drain metal workfunction (WF), (b) corresponding band diagrams close to channel–drain interface in the OFF-state.

JL FET. Additionally, the detailed process variation analysis pertaining to parameters, NW diameter d_{NW} , channel doping N_{Ch} and spacer have shown better robustness and immunity in NW SD FET unlike the other two NW configurations.

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