

Junctionless FETs On Silicon-On-Insulator With Buried Metal Fin For Multi Threshold Operation

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Abstract

In this paper, an n-channel junctionless FET (JLFET) based on SOI with a buried metal fin (BMF) is presented. We show that the BMF of suitable workfunction of the proposed device BMF-SOI-JLFET can control the channel electrostatic field by employing Schottky junction effectively. The enhanced association of potential between BMF and the channel combined with gate electric field makes it worthy for multi-threshold and dynamic threshold (DT) operation. Additionally, the biasing of BMF projects the broad range of threshold voltage (V_{TH}) regulation with a high value of body factor (γ). The proposed device demonstrates γ enhancement compared to fin body (FB)-JLFET and conventional SOI-JL FET under identical conditions due to constant potential coupling. The DT mode of operation shows a 73% improvement in ON-state current in addition to reduced subthreshold swing contrast to BMF-SOI-JLFET without DT. This paper imparts a viable option for low power applications with multi-threshold operation and high switching speed applications with DT operation.

Introduction

In recent years, the need for devices having increased switching speed and improved device density leads the device scaling to nanometer regime. But, the aggressively scaled devices are more prone to short channel effects (SCEs) –the critical challenges in nanometer-scaled devices. By employing fully depleted silicon-on-insulator (SOI), multigate architectures such as FinFETs with enhanced electrostatic controlling of gate and different conduction mechanism mainly band-to-band-tunnelling (BTBT), we can alleviate the SCEs substantially [1]–[5]. Recently, a junctionless transistor (JLT), which has the same type of dopant impurity in channel and drain/source regions, has been proposed as an apt alternative for nanometer-scaled devices. The JLTs present simpler fabrication process, reduced SCEs compared to conventional MOSFETs and lower thermal budget [6]–[8].

The JLTs based on SOI has degraded subthreshold behavior and device performance towards SCEs compared to JLTs built on bulk substrate, as their device performances have been compared in [9], [10]. Moreover, to turn off the SOI JLT devices properly and to have reduced leakage current, either a narrow channel width or high gate workfunction required and it is restricted by the process complexity. Additionally, bulk FinFETs offer greater flexibility by specified device parameter for enhanced subthreshold characteristics. In these JLTs, controlling of subthreshold leakage in Si device layer is done by either p-n junction depletion in vertical direction as in BPJLT [9] or by employing a high- κ BOX dielectric integrated with highly doped (p+) substrate [11]. A vertical non-uniform doping profile (Gaussian) has been used for achieving the same as reported by Mondal *et. al.* [12]–[14]. Recently, a buried-metal-SOI-lateral JLT (BM-SOI-LJLT) has been demonstrated in which buried metal induces bottom depletion by employing Schottky junction, with enhanced ON-to-OFF current ratio [15].

The multigate structures with back-gate/substrate biasing has been reported in various literature [16]–[20], and these devices are operated for multi- V_{TH} with legitimate γ by employing substrate/back-gate bias. This back-gate/substrate biasing offers a way to achieve high performance in ON-state (active

mode) and low power in OFF-state (standby mode), it also provides greater flexibility in circuit design [21]. Additionally, DT mode of operation has been demonstrated besides of multi threshold operation to enhance the ON-current without expense of OFF state current [22]. In DT mode of operation, varying voltage of electrically connected gate and body terminals changes the body potential dynamically. It has been illustrated that device having high value of γ decreases threshold voltage and subthreshold swing (S.S) drastically which results in rapid increase of ON-state current [23].

The controlling of V_{TH} in FinFET is still aided by substrate bias, however, the enhanced gate controllability in multigate structure negates the channel to substrate coupling which results in smaller γ and it further reduces notably with increase in fin height. Recently, Kumar *et.al* [24] demonstrated that JLFET with fin body (FB-JLFET) can attain a large γ owing to stronger coupling between channel and fin body (p-n junction coupling). In this work, we propose a SOI-JLFET with a buried metal fin underneath the active layer (BMF-SOI-JLFET). Here, we use the buried metal layer concept in FinFET structures instead of planar SOI-JLFET for multi-threshold and dynamic threshold operation. BMF-SOI-JLFET utilizes Schottky junction at bottom interface of channel to obtain a large body factor and, to enhance the electrical performance of it by implementing workfunction variation of BMF, biasing of BMF and DT operation.

The paper is organized in subsequent section. Section II outline the structural detail, conceptual process flow and simulation setup. In Section III, the effect of BMF workfunction and biasing of BMF are analyzed in continuation with DT operation. Lastly conclusions are made in Section IV on the basis of results.

Device Structure And Simulation Setup

The 3-D view of proposed BMF-SOI-JLFET is depicted in Fig. 1, having a thin active layer doped by n-type impurity with channel thickness T_{CH} wrapped on a buried metal fin. A stack of gate dielectric with equivalent oxide thickness (EOT) = 1 nm has been used, also gate metal with workfunction 5 eV is employed. Here, BMF-SOI-JLFET utilizes a buried metal (with workfunction $\varphi_{BM} > \varphi_{Si}$) fin of width (W_{MF}) and height (H_{MF}), which is sandwiched between active n + layer and buried oxide (BOX) of thickness $T_{BOX} = 20$ nm. It is worth to mention that electrostatic influence of BMF-SOI-JLFET channel is controlled by top contacts of multigate with added coupling at bottoms of channel by Schottky junction (between active layer and buried metal fin).

Figure 2 shows the proposed process flow of BMF-SOI-JLFET. Figure 2(a) depicts the initial handle wafer and subsequently oxide is deposited in Fig. 2 (b). After that metal (Co, $\varphi_{BM} = 5.0$ eV [25]) can be sputtered using ion-beam sputtering on the patterned seed wafer [26]. (d) The plasma-assisted bonding method is used to bond seed wafer and handle wafer and in subsequent annealing[27], [28]. Fin is patterned after splitting the wafer. In Fig. 2(e), gate oxidation, gate metal deposition and patterning are carried out, after that nitride spacer and contacts are developed in Fig. 2(f)

The numerical simulations are carried out using Sentaurus TCAD simulator [29] in a 3-D work-framework. Simulator solves the Poisson and carrier continuity equations in self-consistent manner to estimate the

electrical characteristics of devices. We have employed Drift-diffusion carrier transport model in general. Fermi statistics model is applied for highly doped Si channel $\geq 10^{19}$, as the density of state of the conduction band may be lesser than doping levels. Bandgap Narrowing (doping dependent) model is used for highly doped Si channel. Shockley–Read–Hall (SRH) generation and recombination model, and robust Nonlocal BTBT model based on Wentzel-Kramers-Brillouin (WKB) tunneling probability have been included to evaluate subthreshold characteristics. The mobility model- Lombardi model for interface degradation, doping dependent, velocity saturation, are included in our simulation for reliable ON-state current. The calibration of simulation models was accomplished by replicating BM-SOI-LJLT with the same set of device parameters, as shown in Fig. 3(d).

Table 1 Simulation parameters

Parameters	Values
Gate Oxide Thickness (SiO_2)	1 nm
Doping Concentration (N_D)	$1 \times 10^{19} - 2 \times 10^{19} \text{ cm}^{-3}$
Gate length (L_G)	20 nm
Buried Metal Workfunction (ϕ_{BM})	4.8–5.1 eV
Buried Oxide Thickness (T_{BOX})	20 nm
Channel Thickness (T_{CH})	8–12 nm
Buried metal fin width (W_{BM})/height (H_{BM})	10 nm
Gate workfunction	5 eV
Supply Voltage	1 V
Tunneling mass	$m_e=0.4m_0, m_h=0.4m_0$
Here m_e and m_h are effective tunneling masses of electrons and holes.	

Result And Discussion

In this section, the characteristics of buried metal fin-body and its effect on device performance have been discussed, as the workfunction dependent Schottky-induced depletion of channel significantly affects the device working. Additionally, the impact of biasing of BMF has been explored for multi-threshold and dynamic threshold operation.

A. Impact of Buried Metal Body

Figure 3(a) shows the transfer characteristics of BMF-SOI-JLFET for different buried metal layers' workfunction. It shows the impact of BMF body workfunction on device performance for $T_{CH} = 10$ nm and gate length $L_G = 20$ nm. At zero gate bias, the channel layer of BMF-SOI-JLFET initially depleted both from bottom and top of the channel surfaces due to the workfunction induced Schottky depletion and work function difference of gate metal-channel, respectively. As, the effective channel appears thinner than the physical one due to the Schottky induced depletion at the bottom, which would add to gate electrostatic control.

It is noticed that reduced off-state current, lower subthreshold slop [see in Fig. 3(b)], and enhanced ON to OFF current ratio can be achieved by increasing the buried metal fins workfunction. This is because increased depletion in bottom owing to Schottky-induced junction results in a thinner effective channel and enhanced gate electrostatic control. It is also observed that with increasing WF of BMF, leakage current through it also reduces. The reduced OFF state current with increasing workfunction of buried metal can be explained by band diagram and carrier distributions at $V_{GS} = 0$ V and $V_{DS} = 1$ V. Figure 4(a) and 4(c) show OFF state band diagram and electron density distribution along the vertical cut of plane B-B' for different workfunction. From figures it is evident that with increasing WF (Φ_{BM}) the gap between the conduction band and Fermi level widens, hence barrier height increases. In the OFF state, with increasing BM WF the depletion layer extended deep into the channel, and the maximum carrier concentration lies around the center of the channel, it can be interpreted by Fig. 4(c) in which the maximum concentration for 4.8 eV is around 10^{12} while for 5.1 eV it reduces to around 10^9 . The ON-current show slight departure against workfunction variation of buried metal as seen in Fig. 3(a) and can be recognized from Fig. 4(b) and 4(d) and it is noticed that the conduction band of the channel near gate oxide interface almost coincide for all WFs of buried metal results in matching carrier density.

As carrier concentration in the channel of JLTs steer the current conduction, the behavior of device (bulk conduction and depletion) can be interpreted by electron density in different dimensions (channel thickness) of proposed device for OFF-state and ON-state, as shown in Fig. 5. With increasing channel thickness, the depletion of channel in OFF-state reduces and this lead to increased subthreshold current as well as ON-current. The transfer characteristics of BMF-SOI-JLFET for different channel thickness T_{CH} plotted in Fig. 6(a) suggest the same.

Moreover, the threshold voltage in JL transistors significantly affected by variations in channel dimension and doping [30], [31], the evaluation of V_{th} variability against T_{CH} for different doping concentration is depicted in Fig 7(b). For fixed BM workfunction (5.1 eV), V_{TH} is slightly more sensitive with increased channel doping as observed by Fig 7(b). Furthermore, for fixed channel doping, sensitivity of V_{TH} could be enhanced by increased workfunction of buried metal.

B. Impact of Buried Metal Bias V_{BM}

In addition, to explore the impact of buried metal bias on the electrical performance of the proposed BMF-SOI-JLFET the I_D - V_G characteristics have been plotted for a different V_{BM} as depicted in Fig. 7. On

applying of negative voltage on the BM body with specified gate voltage, the channel depletes additionally from bottom of the channel interface by elevating energy bands as depicted in Fig 8(a). It could be substantiated by the observing the Figs. 5 and 6, even as, a slight shift of conduction band at junction interface results in change of carrier concentration as well as subthreshold current at given gate voltage. So, V_{TH} is affected by change in V_{BM} as can be observed from Fig. 7.

The standard technique to study the impact of body bias on the I_D - V_G -characteristics is body factor (γ) parameter. γ is determined by proportion of change in V_{TH} against change in V_{BM} , i.e., $\gamma = \Delta V_{TH} / \Delta V_{BM}$ [21] and we extracted V_{TH} by constant current method at 10^{-7} A. The demand of high ON-current in active mode of operation and low OFF-current in standby mode for multiple V_{TH} application is achieved by a high valued body factor (γ) transistor. It is noticed that from Fig. 8(a), the gap between conduction band and fermi level is affected by V_{BM} at given gate voltage and hence deviation in V_{TH} . From Fig. 8(b), which shows the estimated γ for $T_{CH} = 8, 10$ and 12 nm, it has been observed that γ is the smallest for $T_{CH} = 8$ nm which means that the electrostatic control on channel will be dominated by top gate. So, it can be stated that for a broad range of threshold regulation thicker channel is recommended. But, it has increased OFF-state current, so the tradeoff is inevitable. Also, Fig. 8(b) shows γ correlation of proposed device with FB-JLFET for different channel thickness T_{CH} , for fair comparison between these devices we adjusted linear threshold voltage approximately 385 mV by altering the gate metal workfunction to 4.75 eV of BMF-SOI-JLFET. The proposed device presents an appreciable γ values (> 2 times) due to constant potential at three BM-junctions of BMF-SOI-JLFET rather than distributed potential in FB-JLFET.

Fig. 9(a) depicts the dependency of γ on workfunction of BM for different channel thickness, it has been demonstrated that with increasing workfunction of BM γ decreases due to reduced coupling in substantially depleted channel. Fig. 9 (b) shows the γ comparison of BMF-SOI-JLFET with conventional tri-gate SOI-JLFET, and proposed device exhibits very large value of γ in contrast to SOI-JLFET thanks to the excellent coupling between BM and channel in BMF-SOI-JLFET.

C. Dynamic Threshold in BMF-SOI-JLFETs

To attain better S.S and enhanced ON-current without any added circuitry in MOSFETs, DT method has been developed. The electrical terminal of gate is tied to the body contact in the DT mode to change the V_{TH} dynamically when the device becomes active (turned ON). The tied body works as secondary gate, i.e., pseudo-multigate [23], as it improves the controlling of gate electrostatic of device. In our proposed device, the gate is electrically tied to the buried metal.

Table 2
 I_{ON}/I_{OFF} under DT mode and Fixed Bias mode

Channel Thickness (T_{CH})	I_{ON}/I_{OFF} (ON to OFF Current Ratio)		
	$V_{BS} = -0.4$ V	$V_{BS} = 0$ V	DT
8 nm	6.11E + 09	3.16E + 08	1.23E + 09
10 nm	1.38E + 08	4.33E + 06	1.05E + 07
12 nm	8.28E + 05	2.01E + 04	3.81E + 04

Here, BMF as secondary gate in this mode of operation will control the depletion of channel at bottom interface and during ON-state, device achieve flatband condition fully as there is any depletion. But, in the OFF-state condition, BMF-SOI and gate contact are at same zero potential and therefore, current remains equal to OFF-state current in the mode when electrical contacts of gate and BM are untied. In ON-state, the barrier at BM-channel interface lowered significantly in DT compared to fixed bias mode $V_{BM}=0$ V as per Fig. 10(a) of the energy band diagram which results in enhanced carriers in channel as shown in Fig. 10(b). In contrast to the fixed bias mode $V_{BM}=0$ V, ON-current has been improved by 73% and Subthreshold Swing improved from 89.94 to 71.19 mV/dec in this mode. It is worth to mentioned that the improved performance in terms of ON-current and SS is achieved without scarifying OFF-state current.

Figure 11 (a) and (b) depicts the I_D-V_G -characteristics of BMF-SOI-JLFET and SOI-JLFET respectively, in fixed bias mode $V_{BM} = 0$ V and DT mode for different channel thickness. Considering similar electrostatic control in both the devices, the influence of DT mode is more noticeable in BMF-SOI-JLFET compared to SOI-JLFET. However, the notable change in ON-current in both the devices are observed without the expense of OFF-current. As in OFF state condition, the gate voltage and buried metal biasing voltage remain same in both operations (for DT mode $V_G = V_{BM} = 0$ and, for fixed bias condition $V_G = 0$ and $V_{BM} = 0$ V).

Table 3
 Comparison of BMF-SOI JLFET and SOI-JLFET

Channel Thickness (T_{CH})	γ , Body factor (Multi- V_{TH} operation)		% I_{ON} improvement (DT mode)	
	BMF-SOI-JLFET	SOI-JLFET	BMF-SOI-JLFET	SOI-JLFET
8 nm	0.1875	0.0325	87.01353	30.09277
10 nm	0.225	0.0375	73.45551	26.21916
12 nm	0.3175	0.0475	60.19778	22.85276

In the previous section, we have seen variation in γ with T_{CH} as large value of γ attributed to current gain. ON-to-OFF current ratio decreases with increase in channel thickness T_{CH} due to poor electrostatic control in thicker channel as observed in Table 2 and Fig. 12(a). High I_{ON}/I_{OFF} is attained in DT mode and fixed biased mode $V_{BM} = -0.4$ V compared to low current ratio in fixed bias mode $V_{BM} = 0$ V. The high value of

I_{ON}/I_{OFF} in DT mode is attributed to the increased ON-current as large no of carriers lie in the channel, while in fixed biased mode $V_{BM} = -0.4$ V, it is because of the reduced OFF-state current by virtue of largely depleted channel. ON-current improvement for different channel thickness T_{CH} for DT operation is compared between proposed device and SOI-JLFET [see Fig. 12(b)] and, BMF-SOI-JLFET experiences larger I_{ON} improvement than SOI-JLFET owing to larger γ . In general, BMF-SOI-JLFET exhibits larger γ and reduced I_{OFF} in fixed bias mode and high ON-current in DT mode contrast to SOI-JLFET. The comparison of multi- V_{TH} and DT mode operation of BMF-SOI-JLFET and conventional SOI-JLFET are tabled in Table 3.

Conclusion

In this work, the numerical simulation of proposed BMF-SOI-JLFET is performed. The novel structure utilizes Schottky junction induced depletion which add-in greater gate controlling with adjusting parameters such as BMF bias and BM workfunction to improve its performance. We have analyzed its operation in multi threshold and DT modes by administering bias scheme on BMF. The BMF-SOI-JLFET exhibits a high γ value owing to robust integration of electrostatics uniformly between channel and BMF. Additionally, DT mode of operation offers a high and low V_{TH} to achieve low leakage and high speed performance by virtue of improved I_{ON} and S.S.

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Figures

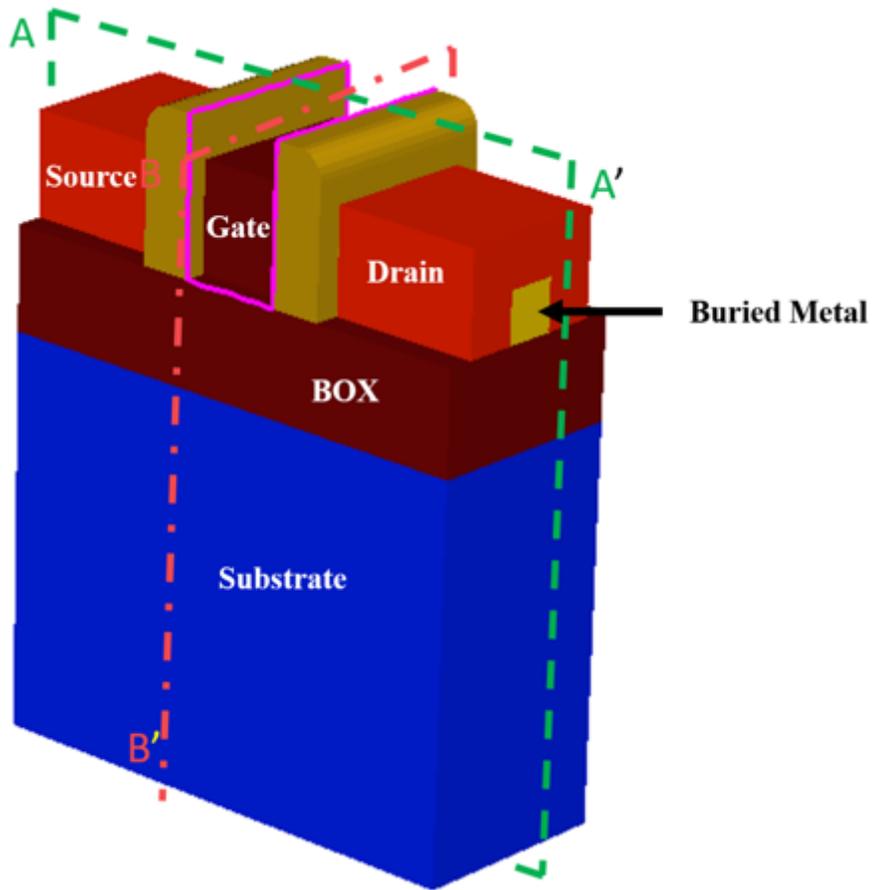


Figure 1

Schematic of tri-gate JL FinFET with a metal Fin and n⁺-active layer (n-typed doped channel)

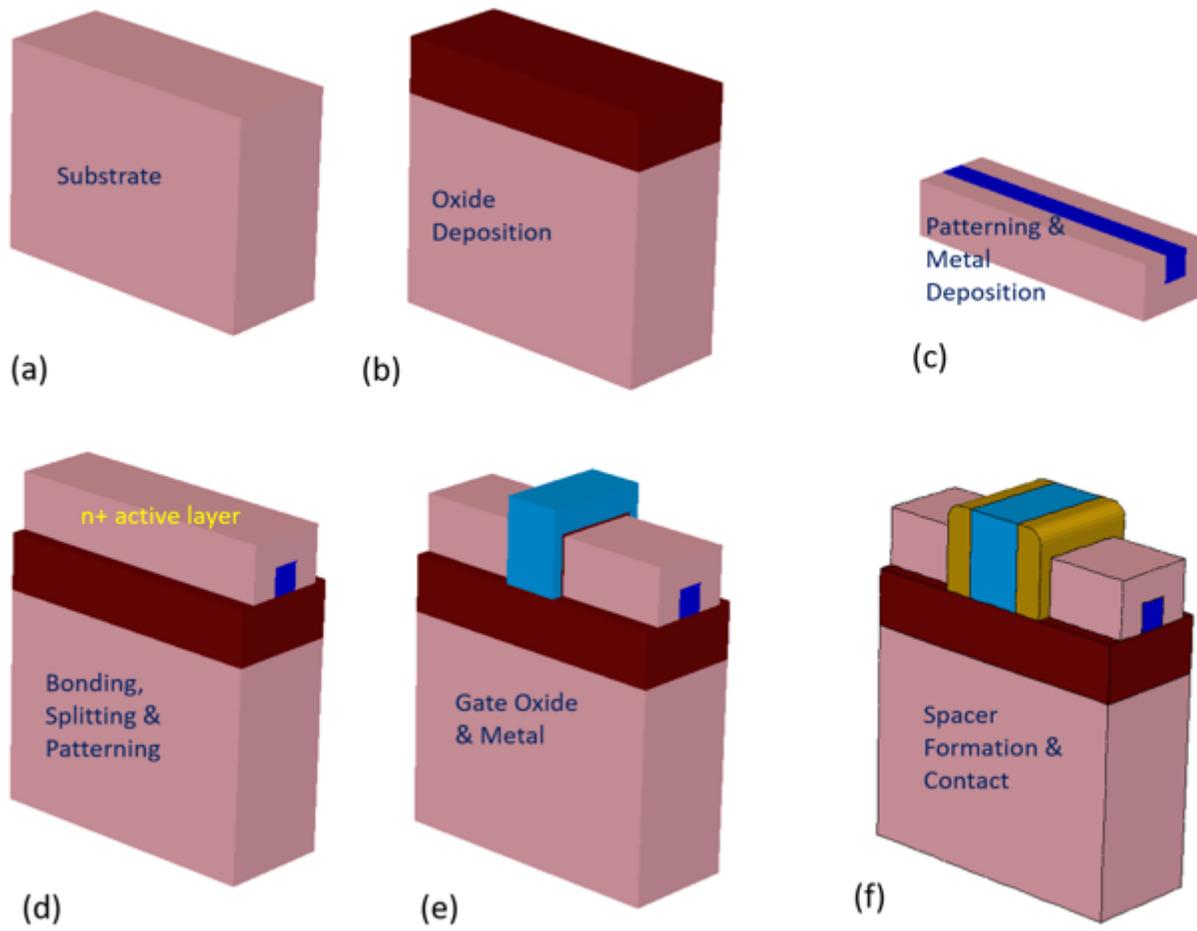


Figure 2

Conceptual process flow of proposed BMF-SOI-JLFET

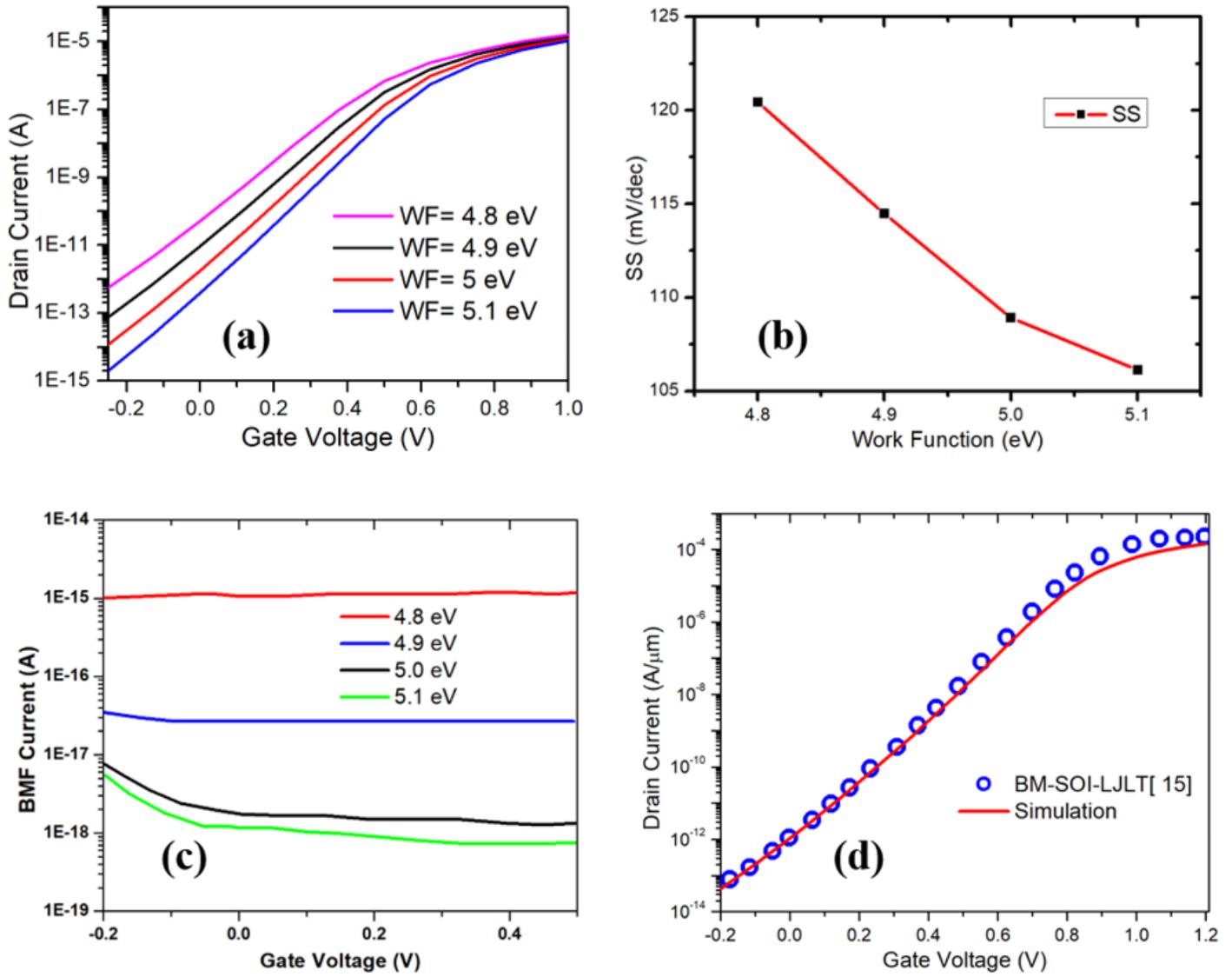


Figure 3

(a) Transfer characteristics BMF-SOI-JLFET for different material workfunction of buried metal and (b) SS correlation of BMF-SOI-JLFET for different WF (c) BMF leakage current vs Gate voltage for different WF of BMF (d) ID-VG of Calibration of BM-SOI-LJLT (Calibration parameters, LG= 20 nm, WF of BM= 5.1 eV, Gate workfunction = 5.1 eV, TCH = 10 nm)

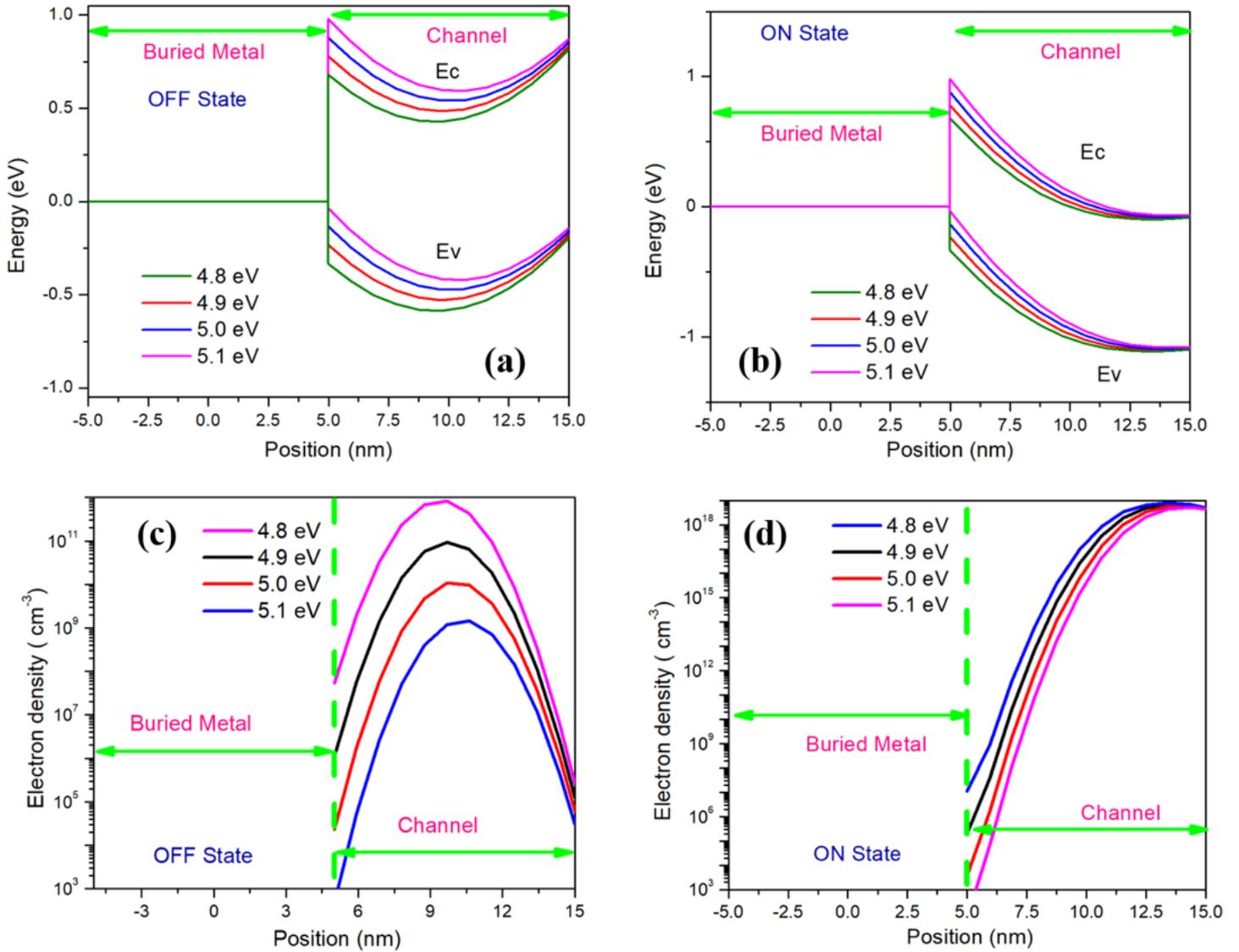


Figure 4

Distribution of Energy Band diagram (a) and (b) and Electron density profile (c) and (d) across vertical cut in cut plane B-B' of BMF-SOI-JLFET for different material workfunction of buried metal. Simulation setup: LG= 20 nm, TCH = 10 nm, ND = $1.5 \times 10^{19} \text{ cm}^{-3}$, WMF = 10 nm, and HMF = 10 nm. ON State (VGS = 1 V and VDS = 1 V) and OFF State (VGS = 0 V and VDS = 1 V)

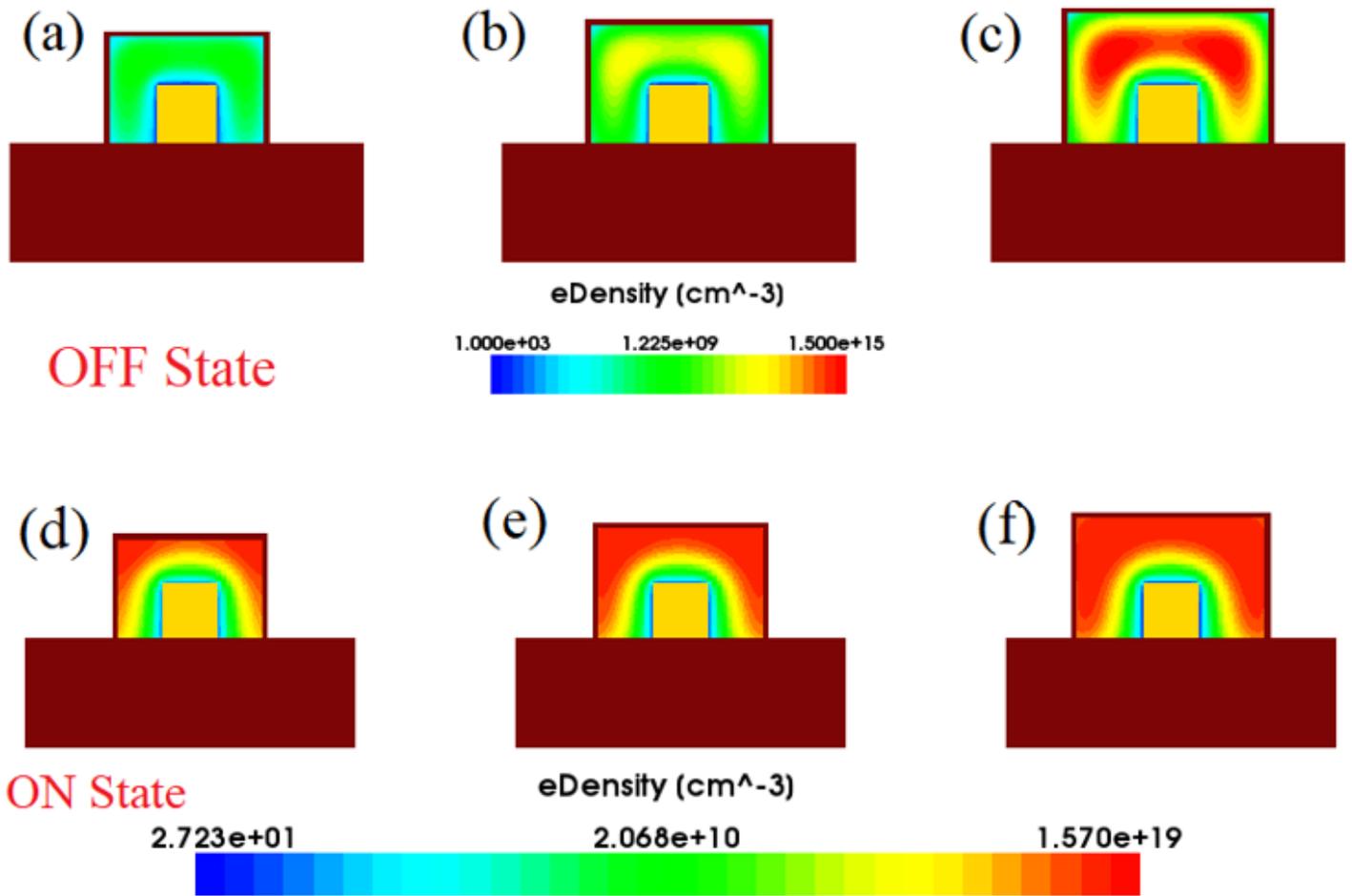


Figure 5

OFF State and ON State Electron density profile across vertical cut plane B-B' of BMF-SOI-JLFET for channel thickness (a, d) 8 nm, (b, e) 10 nm and (e, f) 12 nm

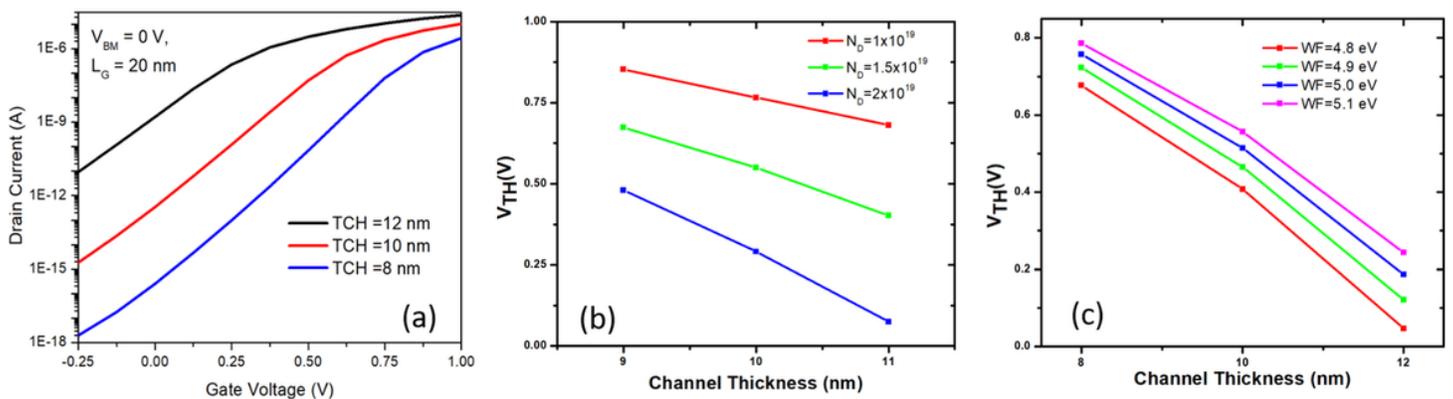


Figure 6

(a) Transfer Characteristics of BMF-SOI-JLFET for channel thickness 8 nm, 10 nm and 12 nm and Threshold voltage variation for different TCH for parameters (b) Channel doping and (c) workfunction of BM Simulation setup: LG= 20 nm, WMF = 10 nm, and HMF = 10 nm. OT = 1 nm

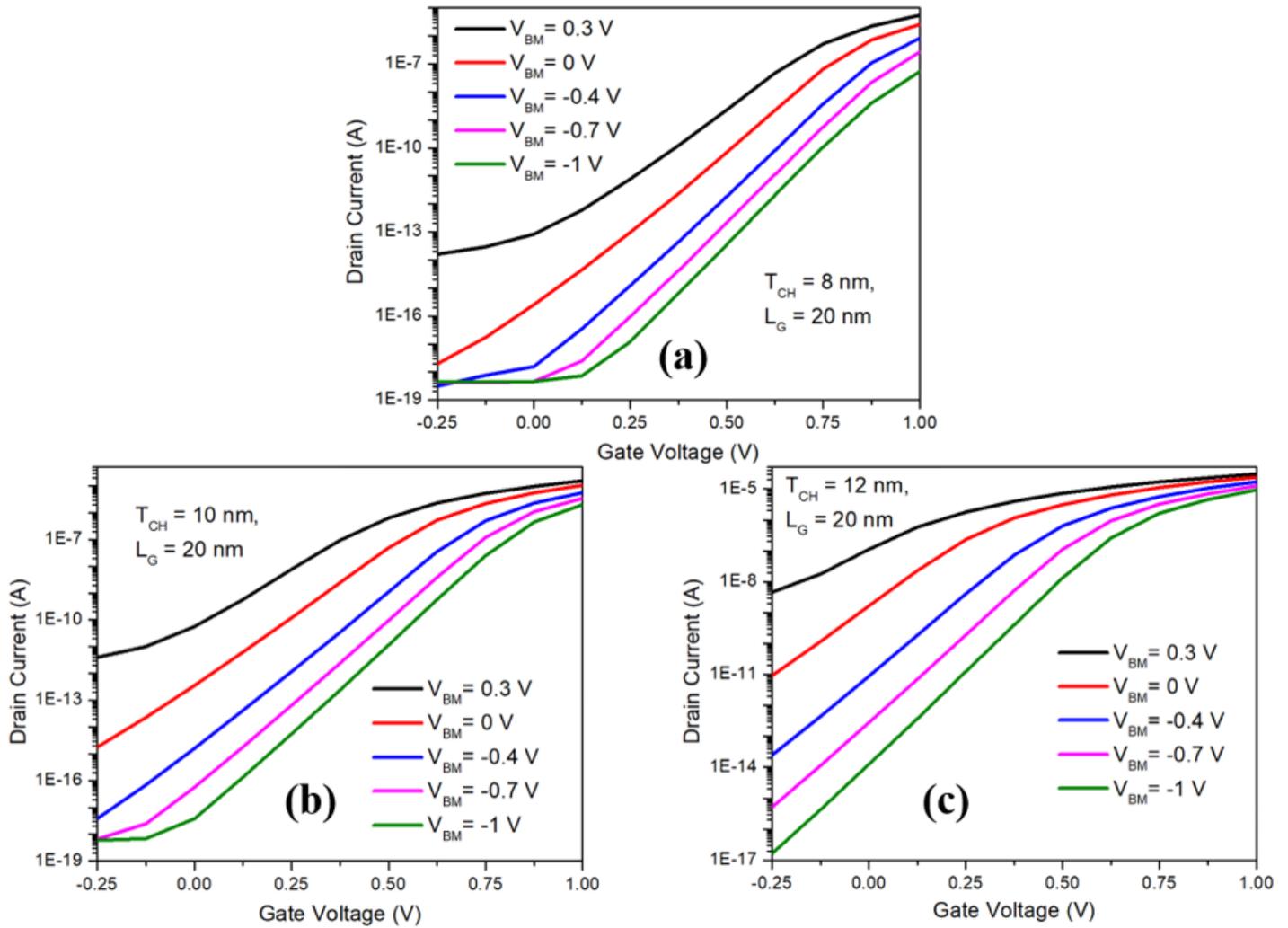


Figure 7

Transfer characteristics BMF-SOI-JLFET for (a) $T_{CH} = 8$ nm, (b) $T_{CH} = 10$ nm and (c) $T_{CH} = 12$ nm against different buried metal biasing (V_{BM}). Simulation setup: $L_G = 20$ nm, $N_D = 1.5 \times 10^{19}$ cm $^{-3}$, $W_{MF} = 10$ nm, and $H_{MF} = 10$ nm. $O_T = 1$ nm

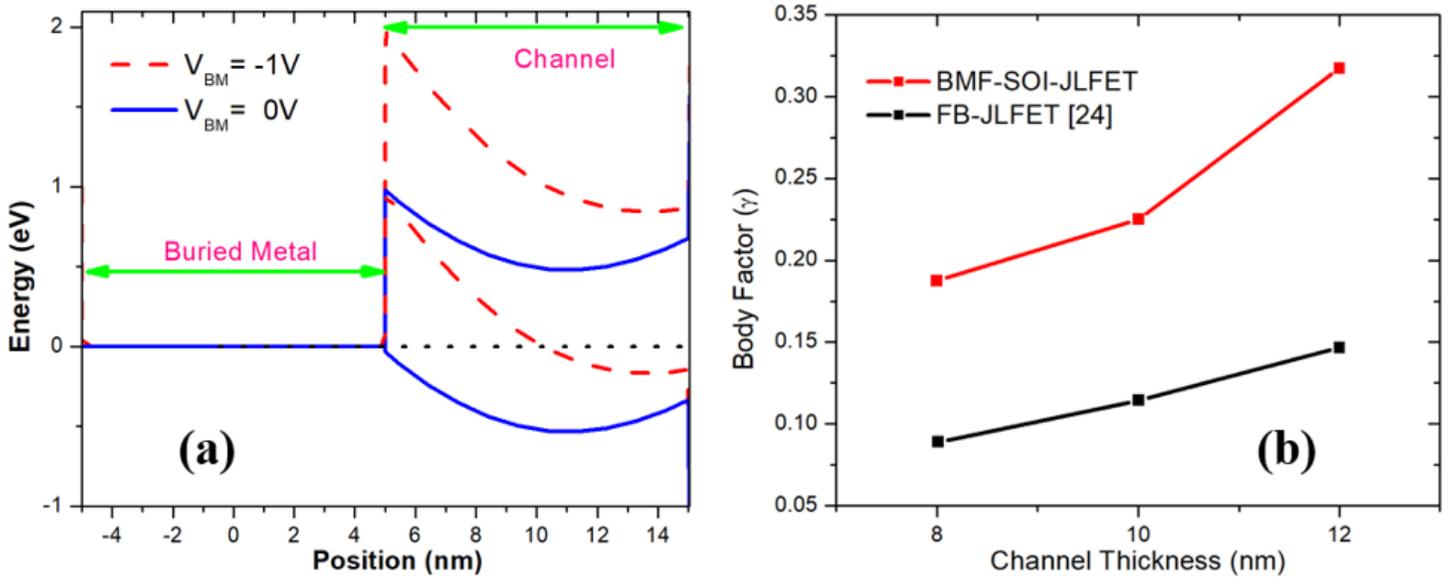


Figure 8

(a) Energy Band diagram across vertical cut in cut plane B-B' of BMF-SOI-JLFET as shown in Fig 1 for $V_{BM} = 0\text{ V}$ and $V_{BM} = -1\text{ V}$ in OFF-state ($V_{GS} = 0\text{ V}$ and $V_{DS} = 1\text{ V}$). (b) Body factor γ comparison of BMF-SOI-JLFET and FB-JLFET for various channel thickness TCH. Simulation setup: $LG = 20\text{ nm}$, $ND = 1 \times 10^{19}\text{ cm}^{-3}$, $TCH = 10\text{ nm}$, $WMF = 10\text{ nm}$, and $HMF = 10$

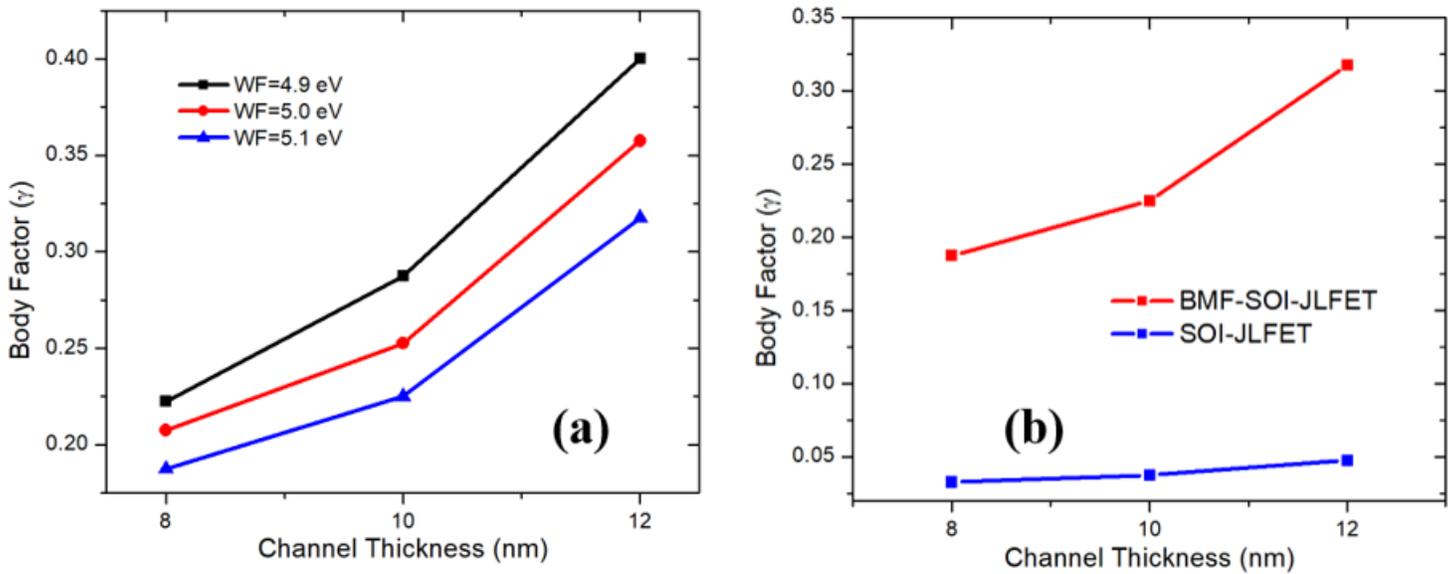


Figure 9

(a) Body factor γ versus channel thickness TCH for different workfunction (b) Body factor γ comparison between BMF-SOI-JLFET and conventional SOI-JLFET for various channel thickness TCH. Simulation setup: $LG = 20\text{ nm}$, $ND = 1.5 \times 10^{19}\text{ cm}^{-3}$, $WMF = 10\text{ nm}$, and $HMF = 10\text{ nm}$. $OT = 1\text{ nm}$

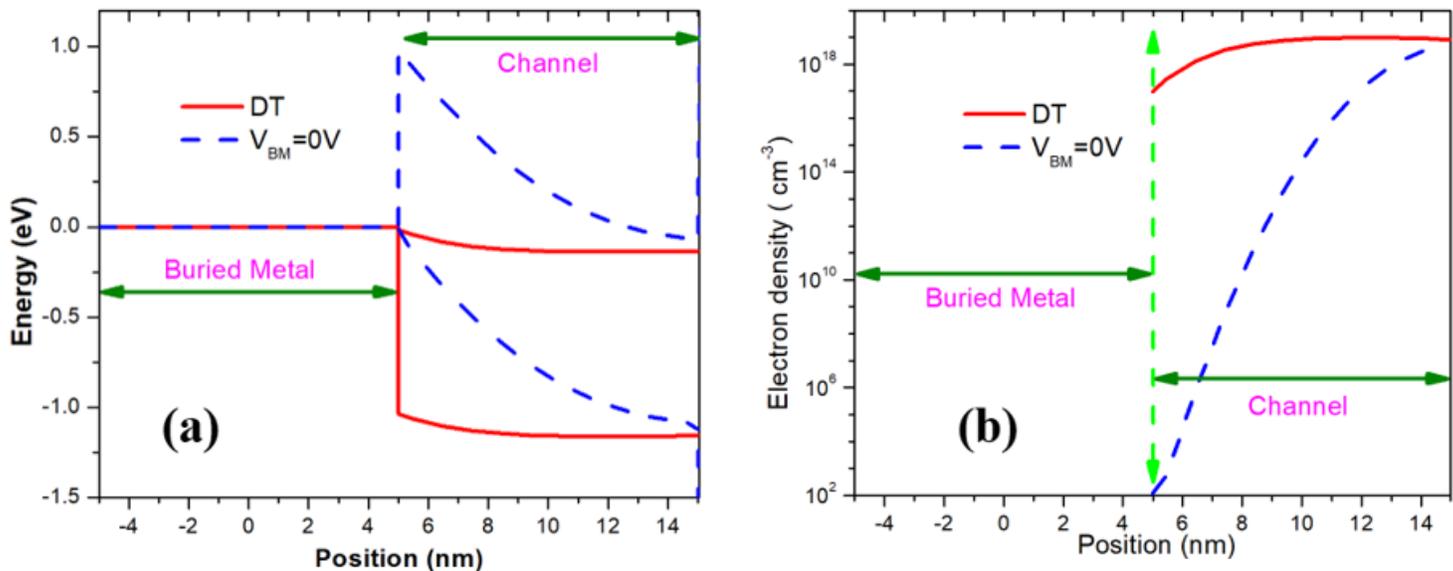


Figure 10

(a) Energy Band diagram across vertical cut in cut plane B-B' of BMF-SOI-JLFET as shown in Fig 1 for $V_{BM} = 0$ V and DT mode in On-state ($V_{GS} = 1$ V and $V_{DS} = 1$ V). (b) On-state ($V_{GS} = 1$ V and $V_{DS} = 1$ V) electron density across channel in DT mode and $V_{BM} = 0$ V

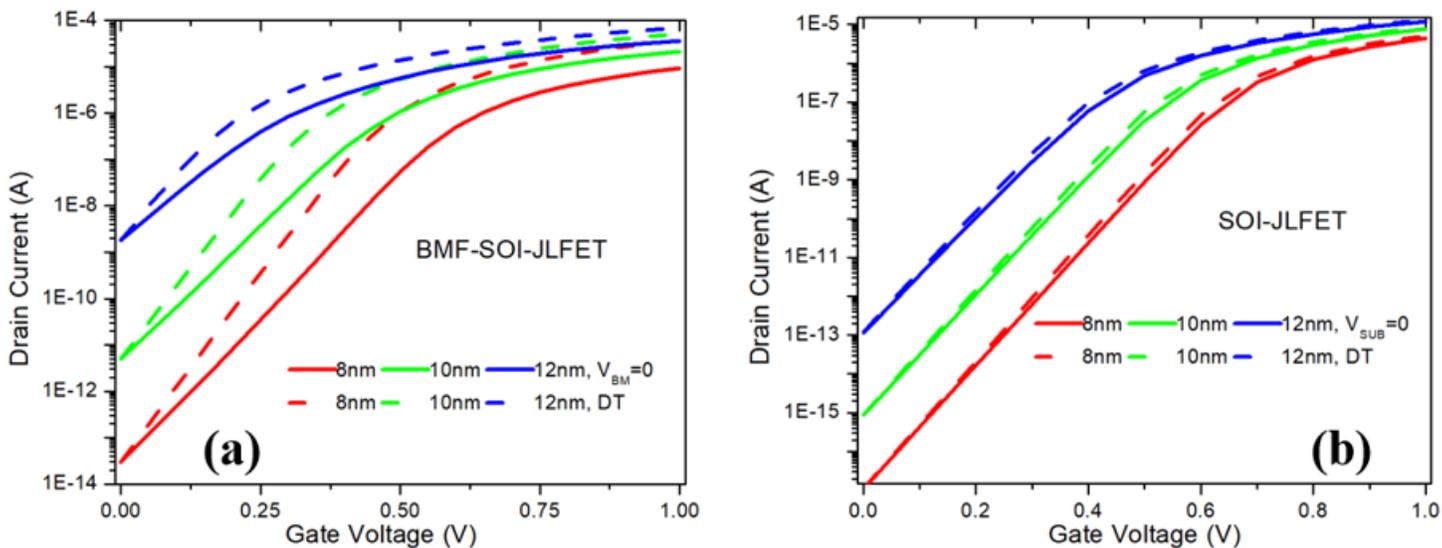


Figure 11

Transfer characteristics of (a) BMF-SOI-JLFET (b) SOI-JLFET for different channel thickness under DT mode and $V_{BM} / V_{SUB} = 0$ V bias. Simulation setup: $L_G = 20$ nm, $N_D = 1 \times 10^{19}$ cm⁻³, $W_{MF} = 10$ nm, and $H_{MF} = 10$ nm. $O_T = 1$ nm

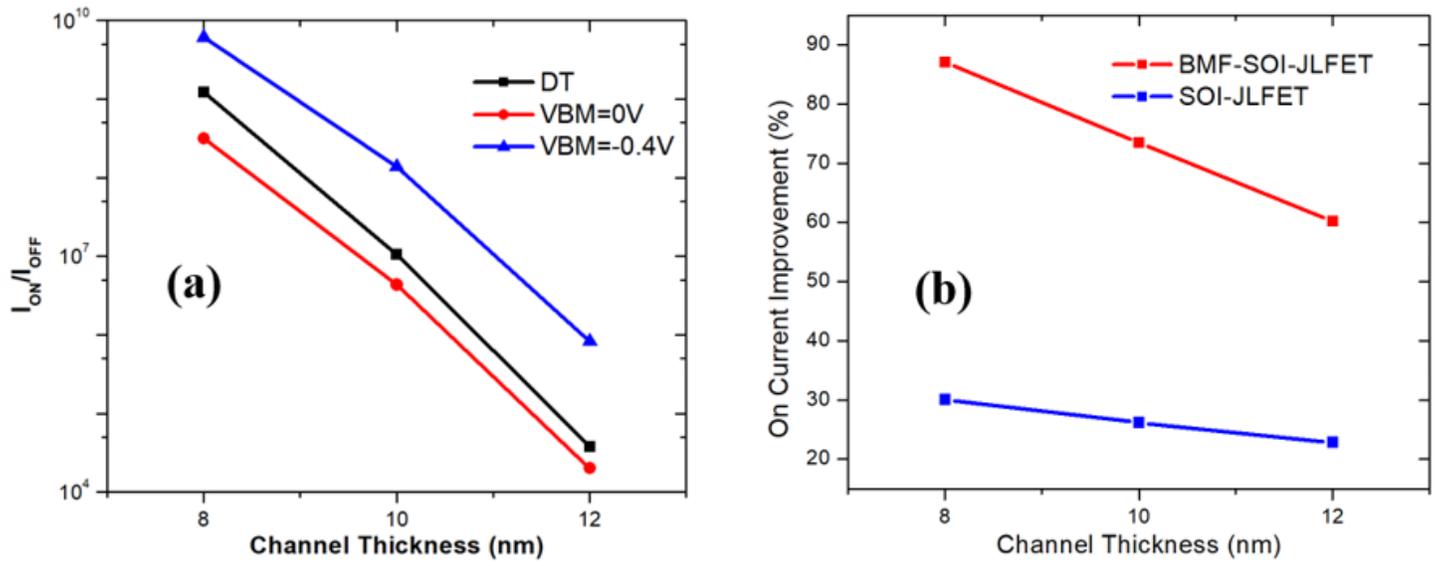


Figure 12

(a) ON-to-OFF current ratio of BMF-SOI-JLFET various channel thickness TCH for DT mode and fixed bias mode with bias voltage $V_{BM} = 0$ V and $V_{BM} = -0.4$ V, (b) % ON-current improvement for different channel thickness of proposed BMF-SOI-JLFET and SOI-JLFET. Simulation setup: $L_G = 20$ nm, $N_D = 1 \times 10^{19}$ cm⁻³, $W_{MF} = 10$ nm, and $H_{MF} = 10$ nm. $O_T = 1$ nm