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Simulation of Ultra-Thin Si-Channel Nanowire FET

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Abstract: Since at the regime of nanometer, the quantum confinement effects are observed and the wave nature of electrons is more dominant. Therefore, the classical approach of current formulation in mesoelectronics and nanoelectronics results in inaccuracy as it does not consider the quantum effect, which is only applicable for the bulk electronic device. For accurate modeling and simulation of nanoelectronics, device atomic-level quantum mechanical models are required. In this work, an ultra-thin (3 nm diameter) Silicon- channel Cylindrical Nanowire FET (CNWFET) is designed and simulated by invoking non-equilibrium green function (NEGF) formalism and self-consistent Schrodinger-Poisson's equation model. Then impact variation of temperature, oxide thickness, and metal work function variation in the proposed NWFET is investigated to analyze the distinct performance parameters of the device e.g. threshold voltage (V_{th}) drain induced barrier lowering (DIBL), sub-threshold swing (SS), and I_{ON}/I_{OFF} ratio. The designed device exhibits reliable results and shows a SS of 57.8 mV/decade and I_{ON} to I_{OFF} ratio of order 10^9 at room temperature.

Keywords: Nanowire FET, quantum mechanical models, non-equilibrium green function, Threshold voltage, Sub-threshold swing

1. Introduction

The demand to scale down MOSFET to increase the chip density with high performance has forced the researcher to look for another device as MOSFET has reached its physical limit [1]. In 2010, Cheung et al. stated that the subthreshold swing of MOSFETs can never be below 60mV/decade at room temperature [2]. The further scaling of the MOSFET channel roughly below 65nm begins to exhibit

quantum phenomena shows high leakage source to drain OFF current and control of gate is lost over the device [3-5]. Moreover, the limitation of the sub-threshold swing will lead to high leakage current even in the OFF state resulting in static power dissipation which finally may result in the thermal runaway of the electronic device [6, 7]. To maintain pace with Moore's Law and pack more and more transistors together, the researcher has been working beyond conventional semiconductor technology [8]. Since the main aim is a small-sized transistor with high performance and low power consumption, many changes in MOSFET structure and MOSFET-like structure were done and but with persistent short channel effects, the parasitic capacitance was observed and very little improvement in the subthreshold swing was achieved [9-11]. In case if the device succeeded in low SS then the ON/OFF current ratio was compromised. The novel Nanoscaled semiconductor devices like nanotube TFETs, Nanowire FET and CNT, etc. are very promising for future electronic systems [12-14]. But the study and simulation of the nanoscaled devices are challenging as at nanoscale regime, the transistor operates near the ballistic limit, electron-hole pairs are generated by the band to band tunneling despite thermal emission and show quantum effects [15, 16].

The classical models of the simulation are optimal for the bulk device but for the mesoscopic and nanoscopic electronics devices, quantum mechanical models are required. Therefore, to model quantum confinement effects, the Self-consistent Schrodinger-Poisson model which uses the 1D NEGF method for computation of current is invoked and ultra-thin silicon channel cylindrical NWFET is designed by considering the nanowires to be a 1-D nanostructure. Then, the impact of work function variation, oxide thickness variation, and temperature variation are investigated to analyze device performance.

2. Device Design and Simulation Model

The 3D-designed structure of cylindrical nanowire FET (CNWFET) is shown in Fig. 1(a). The diameter of the cross-section is chosen as 3 nm (2 nm Si + 1nm SiO₂). The shown Fig. 1(b) is of the two-dimensional structure of the designed CNWFET which has been used for current simulation and is

derived from cutting the three-dimensional structure along the Y-Z plane. The vertical length of the proposed NWFET is 50 nm with a channel length of 30 nm and drain and source region length is 10 nm each. The source and drain are doped with an N-type uniform doping profile of $1 \times 10^{18}/\text{cm}^3$ and $1 \times 10^{20}/\text{cm}^3$ whereas the channel is doped with a P-type doping profile of $1 \times 10^{15}/\text{cm}^3$. The various design parameters of the device are mentioned in Table 1.

Fig. 1(a) Three-dimensional structure of proposed Cylindrical Nanowire FET (CNWFET) (b) Two-dimensional structure of proposed Cylindrical Nanowire FET (CNWFET)

Table I: various design parameters of proposed cylindrical NWFET

S. No.	Design Parameters	Values
1	Channel length	30 nm
2	Gate work function	4.7 eV
3	SiO ₂ thickness	1 nm
4	Si layer thickness	2 nm
6	Source doping Concentration	n-type $1 \times 10^{15}/\text{cm}^3$
7	Drain doping Concentration	n-type $1 \times 10^{20}/\text{cm}^3$
8	Channel doping Concentration	p-type $1 \times 10^{15}/\text{cm}^3$

Since the diameter of the designed device is 3 nm, it requires quantum mechanical models for its accurate simulation. The Self-consistent coupled Schrödinger Poisson model uses Schrodinger relation to obtain the density of state and Poisson equation to derive the potential which is further used in solving Schrödinger equations. The one-dimensional quantum confinement (say Y-axis), 1D Schrodinger equation (1) is used.

$$-\frac{\eta}{2} \frac{\partial}{\partial x} \left(\frac{1}{m_y^v(x, y)} \frac{\partial \psi_{iv}}{\partial x} \right) + E_c(x, y) \psi_{iv} = E_{iv} \psi_{iv} \quad (1)$$

The equation (1) is solved to get Eigen state energies $E_{iv}(x)$ and wave function $\psi_{iv}(x, y)$ at each node perpendicular to X-axis. Here, $E_c(x, y)$ is the band edge energy. The $m_y^v(x, y)$ represents effective mass in the Y direction and it should be noted these effective mass are dimension dependent and varies with the direction. The general Poisson equation is given by

$$\nabla(\epsilon \nabla V) = -\rho \quad (2)$$

Where ϵ is material-dependent permittivity, V is the electrostatic potential, and ρ is the charge density. The density of state obtained by solving equation (1) are discrete and are reduced to a sum over bound state energies from integral over energy by applying Fermi-Dirac statistics. Thus the carrier concentrations obtained for 1D confinement is given as

$$N(x, y) = 2 \frac{k_B T}{\pi \hbar^2} \sum_v \sqrt{m_x^v(x, y) m_z^v(x, y)} \sum_{i=0}^{\infty} |\psi_{iv}(x, y)|^2 \ln \left[1 + \exp \left(-\frac{E_{iv} - E_F}{K_B T} \right) \right] \quad (3)$$

The evaluated carrier concentrations from equation (3) are substituted in net charge density in Poisson's relation. Since the net charge density is given by

$$\rho = q[N_{Doping} - N(x, y)] \quad (4)$$

Where q is the absolute electron charge, N_{Doping} is doping atom concentration in the Silicon film and $N_{(x,y)}$ is the calculated electron density. Thus, the potential derived from solving the Poisson equation (3) is substituted back into Schrodinger's equation. This is an iterative process between Schrodinger's and Poisson's equation which continues until convergence and a self-consistent solution of Schrodinger's and Poisson's equation is obtained. A predictor-corrector scheme using the non-equilibrium green function (NEGF) model is used for the stable and oscillation-less iteration process. After multiple iterations, wave functions are obtained and remain constant, where Eigen energies are constantly revised with each iteration and substituted in Poisson's equation. In this scheme, the Poisson equation act as a predictor, and the number of predictor iteration is controlled by the NEGF model.

$$J_n = -q\mu_n N \nabla \phi + qD_n \nabla N \quad (5)$$

The final solution of this self-consistent coupled Schrodinger-Poisson equation is incorporated in the drift-diffusion model (DDM) to obtain the current density and final drain current of the device. Equation (5) is a general drift-diffusion equation. The designed device is simulated in the atlas silvaco tool and during simulation drift-diffusion space model (dd_ms) along with Schrodinger (p.schro) and (ox. schro) are utilized to consider floating body effects and quantum confinements in cylindrical NWFET. Generation-recombination phenomena like Shockley-Read-Hall (srh), impact ionization, band to band tunneling and Auger models are also here.

3. Results and Discussions

To study the effect of various device design parameters on the performance of the device, drain current, electric field, Potential, are plotted through simulation. To analyze the impact of device design parameters

on the performance of the device, the parameters such as silicon dioxide thickness (T_{ox}), temperature, and gate work function are also varied.

A. Transfer and Output Characteristics

The transfer characteristics (I_D - V_{GS}) of the proposed cylindrical NWFET device including the design parameter mentioned in Table 1 are plotted in Fig. 2 for $V_{DS}=1V$. The ON-current (I_{ON}) at $V_{GS}=1V$ and $V_{GS}=1.5V$ is noticed as $6.70 \times 10^{-7} (A/\mu m)$ and $8.67 \times 10^{-7} (A/\mu m)$ whereas the OFF-current (I_{OFF}) is observed as $5.67 \times 10^{-16} (A/\mu m)$ and leads the I_{ON}/I_{OFF} ratio in the range of 10^9 . Fig. 3 shows the output characteristics (I_D - V_{DS}) of the proposed device for $V_{GS}=0.6V$ and inset shows (I_D - V_{DS}) variation for I_D - $V_{GS}=0V$, drain current varies from $2.57 \times 10^{-10} (A/\mu m)$ to $1.13 \times 10^{-7} (A/\mu m)$ for $V_{GS}=0.6V$ and it varies between $1.13 \times 10^{-14} (A/\mu m)$ to $2.8 \times 10^{-16} (A/\mu m)$ for $V_{GS}=0V$.

Fig. 2 the transfer characteristics (I_D - V_{GS}) of the proposed cylindrical NWFET device for $V_{DS}=1V$

Fig. 3 I_D - V_{DS} Characteristics of proposed NWFET at $V_{GS}=0.6$ V and $V_{GS}=0$ V

B. Impact of Temperature Variation

To study the effect of temperature on the designed nanowire FET, the device is simulated at five different temperatures which are 273K, 300K, 310K, 323K, and 373K. The obtained (I_D - V_{GS}) characteristics, electric field, and potential variation at distinct temperatures are shown in Fig. 4. The uniform doping of source, drain, and the channel is maintained constant at $1 \times 10^{15}/\text{cm}^3$ n-type, $1 \times 10^{20}/\text{cm}^3$ n-type, and $1 \times 10^{15}/\text{cm}^3$ p-type respectively. The effect temperature variation is highly observed on I_{OFF} as with increasing temperature the OFF current increases but the I_{ON} is very less affected by temperature variation. In Fig. 4(b), it is observed that the temperature effect on the electric field is minimal and the potential curve tends to shift downward with increasing temperature as shown in Fig. 4(c). The subthreshold swing is 54.4 mV/dec at 273K temperature and on increasing the temperature the SS increases which justifies the fact that sub-threshold swing is a function of temperature [2], $SS(T) \approx \ln 10 \frac{KT}{q}$. The variations of the various performance parameters like threshold voltage (V_{th}), drain induced barrier lowering (DIBL), SS, and I_{ON}/I_{OFF} ratio with temperatures are shown in Table-II; these

values are evaluated at the SiO₂ thickness of 1 nm, and gate work function of 4.7 eV. It can be seen from Table II that the threshold voltage and I_{ON}/I_{OFF} ratio decreases with the temperature whereas DIBL and SS increase with the temperature.

Fig. 4 (a) I_D - V_{GS} characteristics of the proposed NWFET for variable temperature, Fig. 4 (b): Impact of variable temperature on Electric Field(V/cm), Fig. 4(c) Impact of variable temperature on the potential (V)

Table II: Variation of various performance parameters for different temperature

Sl.No.	Temperature(K)	Threshold Voltage (V)	DIBL(V/V)	Sub-threshold Swing(mV/dec)	I _{ON} /I _{OFF} Ratio
1	273	0.602174	5.07873	54.3947	1.00702x10 ⁹
2	300	0.589483	5.57474	57.80	1.16112x10 ⁹
3	310	0.584566	5.76593	61.8041	1.12349x10 ⁹
4	323	0.577842	6.02453	64.4098	9.07174x10 ⁸
5	373	0.55377	7.057	74.443	7.46655x10 ⁷

C. Silicon-Oxide (SiO₂) Thickness Variation

To examine the impact of SiO₂ thickness variation on the device performance, the silicon oxide thickness is varied from 0.5nm to 1nm at constant room temperature and the corresponding I_D-V_{GS} characteristics, electric field variation, and potential variations are plotted in Fig. 5. It can be observed from the I_D-V_{GS} characteristics are shown in Fig. 5 (a) that decreasing the oxide thickness increases both the I_{ON} and I_{OFF} but the increase is minimal. The doping concentration of source, drain, and channel regions are maintained constant at 1x10¹⁵/cm³ n-type, 1x10²⁰/cm³ n-type, and 1x10¹⁵/cm³ p-type respectively. The effect of SiO₂ thickness variation on device parameters such as potential and electric field is shown in Fig. 5 (a) and 5(b) which show augmentation in both electric field and surface potential of the device. The variations of the other performance parameters; V_{th}, DIBL, SS, and I_{ON}/I_{OFF} ratio for various oxide thickness are summarized in Table-III, these values are evaluated at the gate work function of 4.5eV and it is seen that I_{ON}/I_{OFF} ratio is the least for 1nm SiO₂ thickness. And it is also noticed that the impact of SiO₂ thickness variation is negligible on the subthreshold swing but DIBL is significantly varying with varying SiO₂ thickness.

Table III: Variation of various performance parameters for different SiO₂ thickness

Sl.N o.	Silicon-Oxide thickness	Threshold Voltage (V)	DIBL (V/V)	Sub-threshold Swing(mV/dec)	I _{ON} /I _{OFF} Ratio
1	Tox=0.5nm	0.388605	5.5843	59.78	1.28499x10 ⁷
2	Tox=0.7nm	0.332582	2.97449	59.7969	1.58127x10 ⁶
3	Tox=1nm	0.351967	3.91673	59.80	2.68734x10 ⁶

Fig. 5 Variation of the (a) I_D-V_{GS} characteristics (b) Electric field, and (c) Surface potential of the proposed NWFET with various SiO₂ Thickness

D. Metal-work Function Variation

The impact of metal work function on the various performance parameters of the proposed NWFET at room temperature is plotted and summarized in Fig. 6 and Table-IV respectively, the doping concentration of source, drain, and the channel is maintained constant as stated before. The oxide thickness of 1nm is maintained constant. From the I_D - V_{GS} characteristics graph shown in Fig. 6 (a), it is observed that changing the gate work function has enormous effects on device performance. The effect of metal work function variation on device parameters electric field and surface potential is shown in Fig. 6 (b) and Fig. 6 (c) respectively. The variations of the V_{th} , DIBL, SS, and I_{ON}/I_{OFF} ratio for various oxide thicknesses are shown in Table 4; these values are evaluated at room temperature. And it can be noticed that on increasing the metal work function both the electric field and surface potential reduce. A very low threshold voltage is observed at a low work function of 4.4eV but as work function increases the threshold voltage also increases. The I_{OFF} increases with increasing gate work function. The high I_{ON}/I_{OFF} ratio of order 10^9 is obtained at a work function of 4.7eV. Further increasing the gate work function reduces the energy band bending and decreases the electric field. Due to increased I_{OFF} with further increasing work function I_{ON}/I_{OFF} ratio reduces to an order of approximately 10^3 .

Fig. 6 Impact of the metal work function variation on the (a) I_D - V_{GS} characteristics (b) electric field (c) and potential

Table IV: Various performance parameters for different work functions

Sl.No.	Work Function(eV)	Threshold Voltage (V)	DIBL	Sub-threshold Swing(mV/dec)	I _{ON} /I _{OFF} Ratio
1	4.4	0.289483	5.57479	59.8085	1.89x10 ⁵
2	4.5	0.351967	3.91673	59.80	2.68734x10 ⁶
3	4.7	0.589483	5.57474	59.80	1.16112x10 ⁹
4	5.2	1.08935	-12.1039	59.80	2.3325x10 ⁶
5	5.4	1.2886	-14.3178	59.8011	672.443

4. Conclusions

This paper presents the design and performance analysis of ultra-thin cylindrical NWFET. Here, the Self-consistent Schrodinger-Poisson model which uses the 1D NEGF methods for computation of current is invoked to model the quantum confinement effects, and then the 2-D Schrödinger equation is applied to the obtained current. Finally, the impact of temperature, oxide thickness, and metal-work function on various device performance parameters like threshold voltage, sub-threshold swing, DIBL, I_{ON}/I_{OFF} ratio is evaluated along with I_D - V_{GS} characteristics, electric field, and surface potential are investigated. The I_{ON} at $V_{GS}=1$ V and $V_{DS}=1$ V is noticed as 6.70×10^{-7} (A/ μ m) whereas the I_{OFF} is observed as 5.67×10^{-16} (A/ μ m) and leads the I_{ON}/I_{OFF} ratio in the range of 10^9 . A 100 K rise in temperature from 273K to 373K causes an 8% decrement in V_{th} , while 40% and 38 % augment in DIBL and SS. The proposed design shows a high I_{ON}/I_{OFF} ratio and hence will be very helpful in designing high-speed integrated circuits and ultra-thin sensor designing.

Author Contributions All authors have equally participated in the preparing of the manuscript during implementation of ideas, findings results, and writing of the manuscript.

Data Availability Current submission does not contain the pool data of the manuscript but the data used in the manuscript will be provided on request.

Declarations

Conflict of Interest The authors declare that they have no conflict of interest.

Ethical Standard The Authors accepted principles of ethical standard and they have no conflict of interest.

Consent to Participate Informed consent.

Consent for Publication Consent is granted.

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