Π -Shape Silicon Window for Controlling OFF-Current in Junctionless SOI MOSFET

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Research Article

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Abstract

in this paper a modified junctionless transistor is proposed. The aim of the novel structure is controlling off-current using π -shape silicon window in the buried oxide under the source and the channel regions. The π -shape window changes the potential profile in the channel region in which the conduction band energy get away from the body Fermi energy and rebuild an electrostatic potential. Beside the significant reduced off-current, on current has acceptable value in the novel Silicon Region Junctionless MOSFET (SR-JMOSFET) than Conventional Junctionless MOSFET (C-JMOSFET). Moreover, replacing silicon material instead of silicon dioxide in the buried oxide causes reduced maximum temperature in the channel region. In this situation the heat could transfer to the π -shape silicon window and the temperature reduces in the active region, significantly.

The simulation with the two-dimensional ATLAS simulator shows that short channel effects such as subthreshold and DIBL are controlled effectively in the SR-JMOSFET. Also, the optimum values of length and thickness of the π -shape window are defined to obtain the best behavior of the device.

1. Introduction

The junctionless transistors are paid more attention nowadays because the fabrication of these devices is easier than conventional structures [1–3]. In the other words, creating junctions is difficult process in the fabrication and also they are source of current leakage that waste power and heat [4]-[5]. In such devices, the reverse bias voltage to the gate is not applied for the turning off them. The junctionless devices are turned off by full depletion of the channel. Moreover, the difference between the gate material and silicon layer of the active region is caused depletion [6].

Junctionless transistors are applied in the thin film silicon to have lower leakage current. But, using this technology in the acceptable silicon thickness makes considerable challenges for design and fabrication [7–10]. One of the vital challenges in such junctionless transistors is reducing leakage current [11]. Low leakage current is result of reducing silicon layer of the active region. But, reduction of this area is more complicated, because using narrow silicon active region destroys the electrical parameters of the MOSFET.

In the other vision, using SOI technology for the junctionless devices reduces leakage current, parasitic capacitance and short channel effects. However, the buried oxide under the active region has low thermal conductivity than silicon and acts as a barrier for heat direction through the substrate [12–16].

In this paper, we have focused on the controlling off-current and thermal performance of the SOI Junctionless MOSFET (JMOSFET). The goal of the new structure is using silicon window in the buried oxide. The shape of this silicon layer is very important to have optimal electrical parameters. Our simulation shows that π -shape silicon layer is the suitable structure. Because, other shapes of the silicon windows reduce on-current extensively. In the novel Silicon Region Junctionless MOSFET (SR-JMOSFET) both off and on currents have acceptable values than Conventional Junctionless MOSFET (C-JMOSFET).

Using a silicon window under the left side of the channel causes thinner width by creating a new depletion region. In the other words a new depletion region occurs between the channel and the silicon window due to the different doping density. So, off-current is reduced significantly due to the new depletion region and the different behavior of the potential in the channel region. Moreover, lattice temperature and maximum temperature in the channel are controlled better than the conventional MOSFET. So, heat could be transferred easily in the silicon region under the channel and the source regions. Reduced maximum temperature is effective for carriers and drain current to achieve better performance of the device.

In order to obtain the optimum electrical parameters of the proposed structure, the length and thickness of the π -shape window is chosen. Also, the comparison of the proposed structure with π -shape, rectangular shape and cubic shape is done in terms of the off and on currents to show the acceptable performance of the SR-JMOSFET.

The paper is organized as follows. Section 2 describes the schematic of the proposed structure and the values applied in the simulation. The results for electrical parameters in comparison with conventional one are describe in Sect. 3. Finally the paper is concluded in Sect. 4.

2. Device Structure And Simulation

The schematic of the proposed silicon region in the junctionless SOI-MOSFET is shown in Fig. 1. It is clear that the BOX under the source and a part of channel is filled with silicon material which has a π -shape. The doping concentration of the π -shape silicon region is the same as the substrate. As it is illustrated in Fig. 1, the length of the silicon region has three parts: top length which is characterized by (L_T), the middle length has L_M label and the left/right length has L_F/L_R symbol. Also, the thickness of the π -shape silicon region is divided to the high thickness (t_H) and low thickness (t_L). The thickness of the buried oxide is considered as t_{BOX} in this figure. All the important parameters values of the proposed structure used in the ATLAS simulation are shown in Table 1 [17]. In the simulation the thicknesses of the π -shape silicon region are fixed to the $t_H=30$ nm and $t_L=15$ nm. It is important to note that the proposed structure and conventional one are the same with 30 nm channel length except the new structure has the π -shape silicon region in the left side of the buried oxide.

In the simulation, uniform doping concentrations throughout the channel and source/drain regions are considered. Also, a hydrodynamic carrier transfer model is applied to consider increasing non-local transport effects caused by drastic changes in the high electric field along small gate length. The recombination process is used using Shockley-Read-Hall mechanism [18]. Moreover, band gap narrowing and mobility model includes both doping and transverse-field dependence, are considered in the ATLAS simulation. The dependency of mobility on perpendicular field, impurity concentration, and temperature is derived by Lombard model. Also, the quantum effect is used by Bohm quantum potential (BQP) model in the simulation.

3. Results And Discussion

The main physical mechanism of the proposed structure could be explained using surface potential profile of the SR-JMOSFET compared to the conventional junctionless MOSFET. As it is clear in Fig. 2, the surface potential has different behavior in the channel region of the SR-JMOSFET. This effect is due to the interface of the channel in the left side with the silicon region. This new situation of the SR-JMOSFET causes that the conduction band energy get away from the body Fermi energy and rebuild an electrostatic potential. In another vision, a part of the channel that has the interface with π -silicon region creates a new depletion region due to the different doping concentration of these two parts. The effect of the new depletion region can be shown in the channel thickness that is important for the direction of carries in the OFF current. In Fig. 2, the surface potential is simulated in $V_g = 0$ V and $V_d = 1$ V for the both of the new and conventional structures. The main difference of the SR-JMOSFET with C-JMOSFET is the higher potential barrier of the new structure. In this situation, less carries can overcome this barrier that causes low leakage current in SR-JMOSFET. This mechanism controls leakage current in junctionless MOSFET effectively.

Electron velocity is plotted in the horizontal position of the active region in Fig. 3. It is clear that the electrons in the proposed structure have higher velocity than the conventional one. The difference is more in the channel region. This behavior is due to the new depletion region which reduces the channel widths in the left side. So, this new device is a useful candidate in high frequency switches application.

The drain current is simulated for the both structures in this study in Fig. 4. Two main points are derived from this figure. Low leakage current of the proposed structure is due to the reduced channel widths. Using π -shape silicon in the buried oxide is useful for decreasing off-state current of the junctionless transistor. But, beside this effective reduction in the leakage current, on-state current also decreases. Using design consideration for the π -shape silicon layer is useful to have suitable values for the off and on currents. Moreover, there is a main reason for considering π -shape for the silicon layer under the source and channel. The off current and on-current of the proposed structure with π -shape for the silicon window, rectangle silicon layer and cubic silicon layer are compared in Table 2. It is clear that higher thickness of the silicon window reduces off current, significantly. However, on-current decreases in the junctionless structure in which the performance of the device reduces. So, considering π -shape for the silicon layer of the junctionless structure have suitable values for both off current and on-current.

There is a significant challenge for the transistors based on the SOI technology. The buried oxide under the active layer acts as a barrier for the temperature direction from the silicon region to the substrate. In this situation, lattice temperature increases and in the higher voltages, the effect of high temperature is more evidence in electrical parameters values. In the proposed structure, a silicon window is replaced with part of buried oxide under the source region and part of the channel. In Fig. 5, the lattice temperature of the SR-JMOSFET and C-MOSFET are compared. It is obvious that the new structure has lower lattice temperature and especially in the high drain voltage the difference is more evidence.

Beside the benefits of using buried oxide in the MOSFETs, maximum lattice temperature in the channel is another drawback of the SOI technology. In the proposed structure, maximum lattice temperature reduces that leads to better control on the carriers which participate through the current. In Fig. 6, maximum lattice temperature is plotted for different channel lengths in $V_d=V_g=1$ V.

Subthreshold swing (SS) can be derived by the inverse logarithmic slope in sub-threshold slope drain current:

$$SS = \left(\frac{\partial \log_{10} I_D}{\partial V_{GS}} \right)^{-1} \quad (1)$$

in the room temperature (300 K), SS is 60 mV/dec, but a typical experimental SS for the scaled MOSFET is about 70 mV/dec and it is slightly degraded due to the short channel effects.

In the proposed structure, SS is less than that of conventional junctionless structure due to the silicon region under the channel region that reforms the depletion region in the channel. So, lower SS of the SR-JMOSFET in different channel lengths is obtained in Fig. 7.

Another parameter that gives significant information about short channel effect is DIBL. In Fig. 8, DIBL is plotted for both structures in this study. The DIBL is calculated using following equation:

$$DIBL = \frac{V_{th}^{dd} - V_{th}^{low}}{V_{dd} - V_d^{low}} \quad (2)$$

where, V_{th}^{dd} is the threshold voltage measured at supply voltage, V_{th}^{low} is the threshold voltage measured at a very low drain voltage (typically 0.05 V). V_{dd} is the supply voltage and V_d^{low} is the low drain voltage. Low value of the SR-JMOSFET is obtained because of using π -shape silicon layer that changes the potential curve in the channel. So, the proposed structure has good performance and it is reliable in the nano scale regime.

As it is mentioned before, the π -shape silicon region has important effect on the off and on currents. So, in the design of the proposed structure, the length of the top layer and middle layer (As it is shown in Fig. 1) should be considered carefully. Increasing the top length of the SR-JMOSFET reduces on-current clearly as it is shown in Fig. 9. But, increasing the middle length of the silicon region decreases the off current considerably as it is plotted in Fig. 10. In the design of the proposed structure, the top length of

the π -shape silicon region is about 1.6 times higher than the middle length and the appropriate lengths for the simulation are $L_T = 50$ nm and $L_M = 30$ nm

4. Conclusion

In this paper a new junctionless transistor is proposed in which off current is controlled effectively. A new structure that is named as Silicon Region Junctionless MOSFET (SR-JMOSFET) is compared with Conventional Junctionless MOSFET (C-JMOSFET) with ATLAS simulation. The results show that a silicon region changes the width of the channel region and also the potential has different behavior in this structure. So, off-current reduces significantly and the on-current has acceptable value. Beside the controlling electrical parameters of the SR-JMOSFET, thermal characteristics are improved in this structure. The silicon window prevents squeezing heat in the channel region and the heat could be transferred to the π -shape region easily and the maximum temperature of the device reduces. Moreover, the π -shape silicon region is compared with rectangular and cubic shape to show better performance of the proposed device. Also, device consideration is applied to have optimum parameters of the proposed transistor.

Declarations

Ethics approval and consent to participate: Not applicable.

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Authors' contributions:

Mahsa Mehrad: Conceptualization, Writing -original draft, Software.

Meysam Zareieeee: Conceptualization, writing, review & editing.

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References

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- [1] J. P. Colinge, et al., "Nanowire transistors without junctions," *Nature nanotechnology*, vol. 5 (3), pp. 225-229, 2010.
-
- [2] H. Bennett, W. L. Charles, "Statistical comparisons of data on band-gap narrowing in heavily doped silicon: electrical and optical measurements," *Journal of applied physics*, vol. 55, pp. 3582-3587, 1984.
-
- [3] C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge, "Junctionless multigate field-effect transistor," *Applied Physics Letter*, vol. 94, pp. 053 511-1- 053 511-2, 2009.
-
- [4] A. Kranti, C. W. Lee, I. Ferain, R. Yu, N. D. Akhavan, P. Razavi, and J. P. Colinge, "Junctionless nanowire transistor: properties and design guidelines," in *Proc. IEEE 34th Eur. Solid-State Device Res. Conf.*, pp. 357-360, 2010.
-
- [5] C. W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J. P. Colinge, "Performance estimation of junctionless multigate transistors," *Solid State Electron*, vol. 54, pp. 97-103, 2010.
-
- [6] A. Garg, B. Singh, Y. Singh, "Dual gate junctionless FET on SOI for high frequency analog applications," *Silicon*, 2020. <https://doi.org/10.1007/s12633-020-00609-9>.
-
- [7] M. Bavir, A. Abbasi, A. A. Orouji, "Reducing the drain leakage current in a double-gate junctionless MOSFET using the electron screening effect," *Journal of Electronic Materials*, vol. 5. 2021.
-
- [8] D. Madadi, A. A. Orouji, "Scattering mechanisms in beta-Ga₂O₃ junctionless SOI MOSFET: investigation of electron mobility and short channel effects," *Materials Today Communications*, vol. 26, 2021.
-
- [9] Kh. Tamersit, "Anovel band to band tunneling junctionless carbon nanotube field effect transistor with lightly doped pocket: proposal, assessment and quantum transport analysis," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 128, 2021.
-
- [10] D. Madadi, A. A. Orouji, "Investigation of tied double gate 4H-SiC junctionless FET in 7 nm channel length with a symmetrical dual p⁺ layer," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 28, 2020.
-
- [11] D. Madadi, A. A. Orouji, "beta Ga₂O₃ double gate junctionless FET with an efficient volume depletion region," *Physics Letters A*, vol. 412, 2021.
-
- [12] M. Mehrad, M. Zareiee, "Improved device performance in nano scale transistor: an extended drain SOI MOSFET," *ECS Journal of Solid State Science and Technology*, vol. 5, M74, 2016.
-
- [13] M. Zareiee, "A new architecture of the dual gate transistor for the analog and digital applications," *AEU-International Journal of Electronics and Communications*, vol. 100, pp. 114-118, 2019.
-
- [14] M. Zareiee, "Modifying buried layers in nano-MOSFET for achieving reliable electrical characteristics," *ECS Journal of Solid State Science and Technology*, vol. 6, M75, 2016.
-
- [15] M. Mehrad, "Reducing floating body and short channel effects in nano scale transistor: inserted P⁺ region SOI-MOSFET," *ECS Journal of Solid State Science and Technology*, vol. 5, M88, 2016.
-
- [16] M. Mehrad, "Application of N⁺ buried layer in reducing lattice temperature of nano-scale MOSFET," *ECS Journal of Solid State Science and Technology*, vol. 5, M158, 2016.
-
- [17] Device simulator ATLAS, Silvaco International; 2019.
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Tables

Table 1: Device parameters of the proposed SR-JMOSFET.

Device parameters	value
Channel length	30 nm
Drain/source length	40 nm
Silicon thickness	10 nm
Buried oxide thickness	40 nm
Drain/source Doping concentration	$1 \times 10^{20} \text{ cm}^{-3}$
Channel doping concentration	$1 \times 10^{19} \text{ cm}^{-3}$
Substrate doping concentration	$1 \times 10^{18} \text{ cm}^{-3}$
π -shape silicon doping concentration	$1 \times 10^{18} \text{ cm}^{-3}$
Top length of π -shape silicon	50 nm
Middle length of π -shape silicon	30 nm
Left length (Right Length)	10 nm
high thickness of π -shape silicon	30
low thickness of π -shape silicon	15
Gate oxide thickness	1 nm

Table 2. The comparison of the π -shape, rectangle and cubic shapes of silicon window in terms of off and on currents.

Device Structure	Off-current (A/ μm)	On-current (A/ μm)
π -shape silicon window	8×10^{-8}	7×10^{-4}
Rectangle silicon window	2×10^{-9}	1×10^{-6}
Cubic silicon window	9×10^{-8}	6×10^{-5}

Figures

Figure 1

Schematic cross section of the proposed Silicon Region Junctionless MOSFET (SR-JMOSFET).

Figure 2

Potential profile along the horizontal position in the $V_G=0$ V and $V_D=1$ V.

Figure 3

Electron velocity of the proposed SR-JMOSFET and C-JMOSFET in the horizontal position of the structures.

Figure 4

Drain current versus gate voltage of the SR-JMOSFET and C-JMOSFET.

Figure 5

Comparison of the lattice temperature in the proposed structure and conventional transistor.

Figure 6

Maximum lattice temperature for different channel lengths of the proposed structure and conventional transistor.

Figure 7

Comparison of the subthreshold swing in different channel length of the SR-JMOSFET and C-JMOSFET.

Figure 8

DIBL versus channel length for the proposed structure and conventional transistor.

Figure 9

Drain current versus top length of the π -shape silicon region in SR-JMOSFET in $V_g = 0.5$ V and $V_g = 1$ V.

Figure 10

Drain current versus middle length of the π -shape silicon window in SR-JMOSFET.