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A Rigorous Analysis of Self-Heating Effects in Nanoscale Dielectric Pocket Double-Gate-All-Around (DP-DGAA) MOSFETs

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Abstract—Dielectric Pocket Double-Gate-All-Around (DP-DGAA) MOSFETs are one of the preferred choices for ULSI applications because of significantly low off-current, reduced power dissipation, and high immunity to short channel effect. However, DP-DGAA MOSFETs suffer from self-heating owing to the unavailability of proper heat take-out paths. In this paper, the electrothermal (*ET*) simulations have been performed with hydrodynamic and thermodynamic transport models to analyze the self-heating effects (*SHEs*) in DP-DGAA MOSFETs. The electrothermal characteristics against various device parameters such as spacer length, device thickness, thermal contact resistance, and drain voltage have been investigated. The effect of *SHE* on the drive current has also been evaluated. Further, the impact of thermal contact resistance and ambient temperature variations of the device on *SHE* and thermal noise have been analyzed using Sentaurus TCAD simulator.

Index Terms—Thermal noise; Thermal contact resistance; Ambient temperature; Lattice temperature; Electrothermal; Drain current; Phonons

1. Introduction

In recent years, information and communication technologies have been developed aggressively with the sustainable progress in MOS technology. The last decade's micrometre (μm) technology of field-effect transistors (FETs) have now been replaced with the nanometre technology node delivering high computing speed for smaller device dimensions [1]. But, the downscaling of device dimensions is achieved at the cost of degraded short channel effects immunity (*SCEs*) [2-3], which restrain the goal of achieving high performance with smaller power dissipation, especially in *Off*-state. Multigate MOS structures provide better control over the channel, among which, Gate-All-Around (GAA) structures are seen as the most competent one [4-6]. They exhibit superb electrostatic control over the channel, less influenced by short channel effects (*SCEs*), and superior packing density with steep subthreshold characteristics [7-8]. However, in our previous investigation, the Dielectric Pocket (DP) GAA and Double-gate-all-around (DGAA) have been shown as potential candidates to achieve high performance and ultra-low power dissipation due to reduced off-state current [9-10].

Nowadays, high power dissipation causes the electronic chips with high MOS density to suffer from self-heating problems. With the shrinking in device dimensions, there is unbalanced scaling of device parameters and supply voltages that cause high electric fields ($\sim 1\text{MV/cm}$) near the channel-drain junction [11]. This high electric field energizes the charge carriers to higher energy levels, and hence they become hot carriers. An ample number of hot carriers in the channel provoke the self-heating problem in the device [12-16]. The self-heating effects (*SHEs*) severely deteriorate the device performance owing to mobility reduction and must be investigated [17]. The saturation drain current is also affected by the *SHEs* significantly, which results in mitigated thermal noise effects [18-19]. Further, electrothermal issues like the wide variation in ambient temperature and increase in hot-carrier injection tend to degrade device performance.

Various researchers have investigated the self-heating problem in silicon-based GAA MOSFETs [20-23]. *Park et al.* [20] studied the electrothermal (ET) effects and degradation of drain current in GAA MOSFETs with vertically stacked multiple silicon-based nanowire channels. An ultrafast high-resolution thermoreflectance (TR) imaging technique was reported by *Shin et al.* [21] for investigating the increase in local surface temperature and high-resolution measurements by heating and cooling at constant time. The device performance degradation by the electrothermal (ET) conductivity was studied by *Kompala et al.* [22] and attributed to the lower thermal conductivity of gate oxide, spacer region material, and higher thermal contact resistance (R_{tc}). *Pala et al.* [23] studied the effect of self-heating with quantum confinement effects (QCEs) in the Tri-Gate transistor. To date, the influence of ambient temperature (T_{Amb}), drain voltage (V_{DS}), and device parameters such as spacer length, spacer conductivity, device length, and thermal contact resistance on carrier temperature, lattice temperature, along with its effect on thermal noise has not been investigated in detail for DP-DGAA MOSFETs.

In the present work, a detailed study of variation in the lattice temperature and carrier temperature-induced degradation against ambient temperature (T_{Amb}), drain voltage (V_{DS}), and various device parameters of DP-DGAA MOSFET using electrothermal (ET) simulations have been carried out. The work also includes the effect of self-heating on thermal noise. The remaining part of this work is ordered as follows: Section II reports the device architecture and models used for simulation. Results and discussion have been described in section III, which includes the heat transport and thermal behavior of DP-DGAA MOSFETs with various device parameters, and at last, section IV summarizes the work in brief.

2. Device Simulation Setup with Calibration

The three-dimensional (3D) schematic of DP-DGAA MOSFET for the simulation-based investigation is presented in Fig. 1. In this configuration, the silicon-based nanotube channel

region has been covered by thin oxide layers and inserted between inner and outer gates. On the both gates, contact metal is used named Tungsten Nitride with a 4.7eV work function [24]. The contact metal of source and drain are used as Molybdenum (*Mo*). All other physical parameters of DP-DGAA MOSFET design for simulations are listed in Table I, and the thermal parameters used for electrothermal (*ET*) simulations are listed in Table II. The Sentaurus 3D TCAD device simulator [25] has been used to simulate the proposed DP-DGAA device structure. Hydrodynamic (*HD*) and Thermodynamic (*TH*) transport models have been used for carrier and heat transport respectively. The density gradient model is applied for solving the quantum confinement effects (*QCEs*) of the charge carriers in the channel region. For the electrothermal (*ET*) simulations, the all-dependent thermal conductivity (T_C) model [11,25] is applied for Silicon. The Lombardi (*CVT*), Philips unified mobility, and high field saturation models have been used to simulate the temperature, carrier concentration, and carrier-to-carrier scattering dependent carrier mobility. The constant thermal contact resistance value at an isothermal ambient temperature of 300K has been used for device terminals' thermal boundary conditions. In Fig. 2, the simulation models are calibrated with the experimental data from Refs. [26] and [11].

3. Results and Discussion

A. Lattice and Carrier Temperature Variations

The carrier energy significantly increases with an increase in the drain-to-source voltage (V_{DS}), and consequently, there is an increase in equivalent carrier temperature (T_C). The carriers with high energy suffer from scattering with lattice atoms, and the heat is transferred to the crystal lattice. Thus, the carrier temperature (T_C) is significantly higher than the lattice temperature (T_L) and ambient temperature (T_A) (i.e., $T_C \gg T_L > T_A$). In Fig. 3, the variation of the optimum value of lattice and carrier temperature against V_{DS} at gate-to-source voltage (V_{GS}) = 1V is

shown. The optimum carrier temperature (T_{Cmax}) and the optimum lattice temperature (T_{Lmax}) increases slowly against V_{DS} up to 0.1V because of low-field transport (*LFT*) [11]. However, above 0.1V, the T_{Lmax} and T_{Cmax} increase more significantly from 304K to 420.7K and 382K to 2694.3K because of high-field transport (*HFT*) [11]. Hence, the carrier temperature enhances, and carriers go through energy relaxation with optical phonons. Fig. 4 demonstrates the variation of the maximum lattice temperature (T_{Lmax}) and maximum electron temperature (T_{Cmax}) versus different spacer lengths (L_{SP}) at $V_{DS} = V_{GS} = 1V$. The up-scaling of spacer length (L_{SP}) with a fixed channel length results in extended gaps between source and drain contacts with the channel, and casts two effects, namely: (a) the electric field gets weaker along the channel length at constant V_{DS} and V_{GS} . Consequently, the energy of charge carriers and T_{Cmax} are reduced significantly. (b) decrease in heat dissipation through the cooling sinks (metallic contacts of S/D) of the device, which causes rise in maximum lattice temperature (T_{Lmax}). It can be observed in Fig. 4 that when the L_{SP} is increased from 5nm to 25nm, the T_{Lmax} increases from 332.9K to 420.7K (~26.3% increase), and T_{Cmax} decreases from 2962.6K to 2694.3K (~9.05% decrease). The plot in Fig. 5 shows the variation of T_L and T_C along the device length at $V_{DS} = V_{GS} = 1V$. The T_L varies from 392.4K to 415.7K, with a 420.68K peak value in the drain region. On the other hand, the T_C varies from 423.8K to 648.4K, with a 2676.9K peak value at the interface of channel and drain.

B. Output Characteristics and Thermal Noise under SHE

The impact of self-heating effects on the output characteristics is shown in Fig.6. Self-heating causes the frequent scattering of hot carriers near the drain side, owing to which populated carriers suffer from degraded charge carrier mobility in the channel region. The degradation results in the downfall of drain saturation current with the increase of V_{DS} for the given value of V_{GS} . According to Fig. 6, the current reduces under self-heating effect (SHE) approximately by 9.93% at $V_{GS} = V_{DS} = 1V$ and $t_{si} = 6nm$ in DP-DGAA MOSFET, whereas for $t_{si} = 8nm$ the

reduction is 12.66% owing to the increased drain current and enhancement of phonon scattering in the channel region. The plot in Fig. 7 depicts the variation of thermal noise in the channel with SHEs and without SHEs against V_{DS} for $V_{GS} = 1V$. In general, thermal noise depends on the conductivity of the channel. However, under the *SHEs*, channel conductivity mitigates significantly due to hot carrier scattering, and thermal noise goes down by 74.7% compared to normal conditions at $V_{DS} = 1V$ and $t_{si} = 6nm$. For $t_{si} = 8nm$, the thermal noise goes down by 77.12% as compared to the case of without *SHEs*.

C. Effect of Thermal Contact Resistance (R_{tc}) on SHE

Fig. 8 shows the variation of lattice temperature against device length for V_{DS} and $V_{GS} = 1V$ for different contact thermal resistances (R_{tc}). Lattice temperature is the maximum in the drain region, i.e., 420.68K owing to the highest lattice scattering of hot carriers for $R_{tc} = 5 \times 10^{-5} cm^2 KW^{-1}$. The lattice temperature also depends on R_{tc} . Low R_{tc} allows dissipation of more heat from the device and helps to decrease the lattice temperature. When R_{tc} reduces from $5 \times 10^{-5} cm^2 KW^{-1}$ to $1 \times 10^{-5} cm^2 KW^{-1}$, the maximum lattice temperature of the drain sinks from 420.67K to 338.53K. Fig. 9 shows the variation of maximum lattice temperature against thermal conductivity of spacer for V_{DS} and $V_{GS} = 1V$ for different contact thermal resistances (R_{tc}). A high conductive spacer provides the precise heat flow path from the device. Fig. 9 verifies that with the increase of the thermal conductivity of the spacer from 0.014 to 0.185W/K-cm at $R_{tc} = 5 \times 10^{-5} cm^2 KW^{-1}$, the lattice temperature decreases from 420.7K to 409K. The variation of drain current against V_{DS} at $V_{GS} = 1$ is displayed in Fig. 10. The high value of contact thermal resistance (R_{tc}) does not easily pass the heat from the device and provokes the high phonon scattering, and thus deterioration in mobility and drain saturation current occurs. Further, the downfall of around 7.2% in drain saturation current at $V_{DS} = 1V$ with the increase in R_{tc} from $1 \times 10^{-5} cm^2 KW^{-1}$ to $5 \times 10^{-5} cm^2 KW^{-1}$ can be noticed in the figure. Fig. 11 depicts the variation of thermal noise against V_{DS} at $V_{GS} = 1V$ for different values of R_{tc} . The increasing amount of V_{DS} deteriorates the

channel conductance, and thermal noise is diminished accordingly. A lower value of thermal contact resistance (R_{tc}) improves the drain current and channel conductivity due to less phonon scattering. An enhanced amount of channel conductivity increases the thermal noise in the channel. As R_{tc} increases from $1 \times 10^{-5} \text{ cm}^2 \text{ KW}^{-1}$ to $5 \times 10^{-5} \text{ cm}^2 \text{ KW}^{-1}$, thermal noise varies from $2 \times 10^{-25} \text{ A}^2/\text{Hz}$ to $6.6 \times 10^{-26} \text{ A}^2/\text{Hz}$ as shown in the figure.

D. Effect of Ambient Temperature Variations

Fig. 12 demonstrates the variation of the maximum lattice temperature (T_{Lmax}) versus ambient temperature (T_{Amb}) for various values of R_{tc} . The T_{Lmax} increases from 420.7K to 517.6K ($\sim 23.03\%$ increase) with the rise of T_{Amb} from 300K to 400K for $R_{th} = 5 \times 10^{-5} \text{ cm}^2 \text{ KW}^{-1}$. Fig. 13 shows the variation of the drain current (I_D) versus ambient temperature (T_{Amb}) for different values of R_{tc} . At $R_{tc} = 5 \times 10^{-5} \text{ cm}^2 \text{ KW}^{-1}$, the I_D decreases from 137 μA to 126 μA ($\sim 8.02\%$ decrease) for rise in T_{Amb} from 300K to 400K as the lateral electric field degrades the carrier mobility. The variation of thermal noise against ambient temperature at $V_{GS} = V_{DS} = 1\text{V}$ for different values of R_{tc} is depicted in Fig. 14. It is to be noted that thermal noise is indirectly related to the ambient temperature. At $R_{tc} = 5 \times 10^{-5}$, with the variation in T_{Amb} from 300K to 400K, the thermal noise increases by approximately 10.05%. Fig. 15 demonstrates the cutline plot of the variation in lattice temperature (T_L) against device channel length at $V_{GS} = V_{DS} = 1\text{V}$ for various T_{Amb} values (300K to 400K in a step of 20K). The drain lattice temperature (T_L) is observed to be higher than the channel and source regions because the large electric field in the drain region renders high probability of carrier scattering near the drain region. However, the T_L increases with an increase in T_{Amb} .

4. Conclusion

In this paper, the self-heating effects (*SHEs*) have been investigated in the Dielectric Pocket Double-Gate-All-Around (DP-DGAA) MOSFETs, and its implications are observed on

Thermal Noise. Because of *SHEs*, the saturation drain current reduces by 9.93% when the channel thickness is 6nm, however when the channel thickness is increased to 8nm the decrement in the current is found to be 12.66%. The thermal noise decreases from 74.7% to 77.12% at the same channel thickness variation. The lattice temperature increases with increasing thermal contact resistance; on the other hand, the drain current and thermal noise significantly reduce upon increasing the thermal contact resistance. The lattice temperature and thermal noise also increase by increasing the ambient temperature, but the drain current reduces monotonously. Moreover, the maximum lattice temperature increases with extension in source and drain length, but the electron temperature is reduced significantly. Thus, source and drain extension length and thermal contact resistance can be used as design parameters to mitigate the effects of self-heating.

Declarations

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Authors' contributions: All authors have made equal contributions to the conception, design, analysis and interpretation of results in the manuscript. The authors have been involved in drafting the manuscript critically for important intellectual content; and have given unanimous approval of the version to be published. Each author has participated sufficiently in the work to take public responsibility for appropriate portions of the content. All the authors have read and approved the final manuscript.

REFERENCES

1. Moore More: International Roadmap for Devices and Systems (IRDS). https://irds.ieee.org/images/files/pdf/2017/2017IRDS_ES.pdf, 2017 (Accessed 09 March 2021).

2. Kim, Y-B., Challenges for Nanoscale MOSFETs and Emerging Nanoelectronics, Trans. On Electronics and Electronic materials 11 (2010) 93-105.
<https://doi.org/10.4313/TEEM.2010.11.3.093>.
3. Song, Y., Choi, W. Y., Park, J. H., Lee, J. D., and Park, B. G., Design optimization of Gate-all-around (GAA) MOSFETs, IEEE Trans. on Nanotech. 5(3) (2006) 186-191.
<https://doi.org/10.1109/TNANO.2006.869952>.
4. Colinge, J. P., Multiple-gate SOI MOSFETs, Solid-state Electronics 48 (2004) 897-905.
<https://doi.org/10.1016/j.sse.2003.12.020>.
5. Colinge, J. P., Multiple-gate SOI MOSFETs, Microelectronics Engineering 84 (2007) 2071-2076. <https://doi.org/10.1016/j.mee.2007.04.038>.
6. Colinge, J. P., FinFET and other multi-gate transistors, In New York: Springer-Verlag. ISBN 978-0-387-71751-7
7. Jimenez, D., Jimenez, J. J. Saenz, Iniguez, B., Sune, J., Marsal, L. F., Pallares, J., Modeling nanoscale gate-all-around MOSFETs, IEEE Electron Device Letter 25(5) (2004) 314-316. <https://doi.org/10.1109/LED.2004.826526>.
8. Lu, W., Xie P., Lieber, C. M., Nanowire transistor performance limits and applications, IEEE Trans. Electron Devices 55(11) (2008) 2859-2876.
<https://doi.org/10.1109/TED.2008.2005158>.
9. Awasthi, H., Kumar N., Purwar, V., Gupta, R., and Dubey, S., Impact of temperature on analog/RF performance of dielectric pocket gate-all-around (DPGAA) MOSFETs, Silicon (July 2020). <https://doi.org/10.1007/s12633-020-00610-2>.
10. Purwar, V., Gupta, R., Kumar, N., Awasthi, H., Dixit V. K., Singh, K., Dubey, S., and Tiwari, P. K., Investigating linearity and effect of temperature variation on analog/RF performance of dielectric pocket high-k double gate-all-around (DP-DGAA)

MOSFETs, Appl. Phys. A 126 (August 2020) 746. <https://doi.org/10.1007/s00339-020-03929-0>.

11. Kumar, A., Srinivas, P. S. T. N., and Tiwari, P. K., An insight into self-heating effects and its implications on hot carrier degradation for silicon-nanotube-based double gate-all-around (DGAA) MOSFETs, IEEE Journal of Elect. Device Society 7 (Nov. 2019) 1100-1108. <https://doi.org/10.1109/JEDS.2019.2947604>.
12. Rhyner, R. and Luisier, M., Minimizing self-heating and heat dissipation in ultrascaled nanowire transistors, Nano Letters 16 (2016) 1022-1026. <https://doi.org/10.1021/acs.nanolett.5b04071>
13. Jiang, H., Shin, S., Liu, X., Zhang, X. and Alam, M. A., Characterization of self-heating leads to universal scaling of HCI degradation of multi-fin SOI FinFETs, Proceedings of International Reliability Physics Electronics Symposium (2016) 2A.3.1-2A.3.7. <https://doi.org/10.1109/IRPS.2016.7574506>
14. Shrivastava, M., Agrawal, M., Mahajan, S., Gossner, H., Schulz, T., Sharma, D. K. and Rao, V. R., Physical insight toward heat transport and an improved electrothermal modeling framework for FinFET architectures, IEEE Transactions on Electron Devices 59 (2012) 1353-1363. <https://doi.org/10.1109/TED.2012.2188296>.
15. Nakagome, Y., Takeda, Y., Kume, H., and Asai, S., New observation of hot-carrier injection phenomena, Japanese Journal of Applied Physics 22 (1983) 99. <https://doi.org/10.7567/JJAPS.22S1.99>
16. Venkateswarlu, S., Sudarsanan, A., Singh, S. G. and Nayak, K., Ambient Temperature-Induced Device Self-Heating Effects on Multi-Fin Si n-FinFET performance, IEEE Transactions on Electron Devices 65 (2018) 2721-2728. <https://doi.org/10.1109/TED.2018.2834979>

17. Braccioli, M., Curatola, G., Yang, Y., Sangiorgi, E., Fiegna, C., Simulation of self-heating effects in different SOI MOS architectures, *Solid-State Electron.* 53(4) (2009) 445-45. <https://doi.org/10.1016/j.sse.2008.09.020>.
18. Jin, W., Chan, P. C. H., and Lau, J., Physical thermal noise model for SOI MOSFET, *IEEE Trans. on Elect. Devices* 47(4) (2000) 768-773. <https://doi.org/10.1109/16.830992>.
19. Gola, D., Singh, B., Srinivas, P. S. T. N., and Tiwari, P. K., Thermal noise models for trigate junctionless transistors including substrate bias effects, *IEEE Trans. on Elect. Devices* 67(1) (2020) 263-269. <https://doi.org/10.1109/TED.2019.2953084>.
20. Park, J. Y., Lee, B. H., Chang, K. S., Kim, D. U., Jeong, C., Kim, C. K., Bae, H., and Choi, Y. K., Investigation of Self-heating effects in gate-all-around MOSFETs with vertically stacked multiple silicon nanowire channels, *IEEE Trans. on Electron Devices* 64(11) (2017) 4393-4399. <https://doi.org/10.1109/TED.2017.2749324>.
21. Shin, S. H., Wahab, M. A., Masuduzzaman, M., Maize, K., Gu, J., Si M., Shakouri, A., Ye P. D., and Alam, M. A., Direct observation of self-heating in III-V Gate-all-around Nanowire MOSFETs, *IEEE Trans. on Electron Devices* 62(11) (2015) 3516-3523. <https://doi.org/10.1109/IEDM.2014.7047088>.
22. Kompala, B. K., Kushwaha, P., Agarwal, H., Khandelwa, I S., Duarte, J-P., Hu, C., and Chauhan, Y. S., Modeling of nonlinear thermal resistance in FinFET, *Jpn. J. Appl. Phys.* 55(4S) (2016) 04ED11. <https://doi.org/10.7567/JJAP.55.04ED11>.
23. Pala, M. G. and Cresti, A., increase of self-heating in nanodevice induced by surface roughness: A full quantum study, *Journal of Appl. Phys.* 117 (2015) 084313. <https://doi.org/10.1063/1.4913511>.

24. Jiang, P. C., Lai, Y. S. and Chen, J. S., Dependence of crystal structure and work function of $W\text{N}_x$ films on the nitrogen content, Appl. Phys. Letters, 89 (2006) 122107.
<https://doi.org/10.1063/1.2349313>.
25. Sentaurus Device User Guide, Version N-2017.09, Synopsys, Mountain View, CA, USA, 2016.
26. Fahad, H. M., Smith, C. E., Rojas, J. P., and Hussain, M. M., Silicon nanotube field effect transistor with core-shell gate stacks for enhanced high-performance operation and area scaling benefits, Nano Lett. 11 (2011) 4393-4399.
<https://doi.org/10.1021/nl202563s>.

Table-1: Device parameters used for DP-DGAA MOSFET simulation.

SI. No.	<i>Parameter</i>	<i>Symbol</i>	<i>Value</i>
1	Channel length	L_C	20nm
2	Source/Drain doping	N_D	10^{20} cm^{-3}
3	Channel doping	N_A	10^{15} cm^{-3}
4	Oxide thickness	t_{ox}	1nm
5	Channel thickness	t_{si}	6nm, 8nm
6	Inner gate radius	T_c	4nm
7	Metal work-function	ϕ_M	4.7 eV
8	Dielectric pocket length	DP_L	4nm
9	Dielectric pocket thickness	DP_D	2nm, 4nm
10	Spacer Length	L_{SP}	5-25 nm
11	Source/Drain Contact Length	L_{SC}/L_{DC}	5 nm
12	Thermal Contact Resistance	R_{tc}	1×10^{-5} - $1 \times 10^{-4} \text{ cm}^2 \text{KW}^{-1}$

Table-2: Thermal conductivity parameters used for device simulation using Ref. [11,14].

SI. No.	<i>Material</i>	<i>Thermal conductivity (W/K-cm)</i>
1	Channel Region (Si)	0.25
2	Source/Drain Region (Si)	0.62
3	SiO_2	0.014
4	Si_3N_4	0.185

(a)

(b)

Fig. 1: (a) Three-dimensional (3D) schematic of DP-DGAA MOSFET, (b) Two-dimensional (2D) cross-sectional schematic view of DP-DGAA MOSFET.

(a)

(b)

Fig. 2: Comparison of transfer characteristics of 3D TCAD simulation with measured experimental data Ref. [26] for DGAA MOSFET with the same device parameters of Ref. [26]. and (b) Ref. [11] for DGAA MOSFET with the same device parameters.

Fig. 3: Variation of peak value of lattice and electron temperature (T_{Lmax} and T_{Cmax}) versus drain-to-source voltage (V_{DS})

Fig. 4: Variation of peak value of lattice and electron temperature (T_{Lmax} and T_{Cmax}) against spacer length (L_{SP})

Fig. 5: Variation of lattice and electron temperature (T_L and T_C) along the device length (nm)

Fig. 6: Comparison of output characteristics of DP-DGAA MOSFET versus V_{DS} with SHE and without SHE for different channel thickness (t_{si})

Fig. 7: Comparison of thermal noise of DP-DGAA MOSFET versus V_{DS} with *SHE* and without *SHE* for different channel thicknesses (t_{si})

Fig. 8: Variation of lattice temperature (T_L) along the device length (nm) for various values of thermal contact resistances (R_{tc})

Fig. 9: Variation of peak value of lattice temperature versus changing thermal conductivity of spacer for various values of R_{tc}

Fig. 10: Variation of the output characteristics against drain bias for different values of R_{tc}

Fig.11: Variation of the thermal noise against drain bias for different values of R_{tc}

Fig. 12: Variation of the peak value of lattice temperature ('Hot Spot') against increasing ambient temperature (T_{Amb}) for various values of R_{tc}

Fig. 13: Variation of the drain current against increasing ambient temperature (T_{Amb}) for various values of R_{tc}

Fig. 14: Variation of the thermal noise against ambient temperature (T_{Amb}) for various values of R_{tc} .

Fig. 15: Variation of lattice temperature (T_{L}) along device channel length (nm) for different values of ambient temperature (T_{Amb})