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Utkarsh Upadhyay

NIT Jalandhar: Dr BR Ambedkar National Institute of Technology

Ashish Raman

NIT Jalandhar: Dr BR Ambedkar National Institute of Technology

RAVI RANJAN (✉ ranjan.ravi80@gmail.com)

Dr BR Ambedkar National Institute of Technology <https://orcid.org/0000-0003-4423-3474>

Naveen Kumar

NIT Jalandhar: Dr BR Ambedkar National Institute of Technology

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Overlapped Gate-Source/Drain H-shaped TFET: Proposal, Design and Linearity Analysis

Utkarsh Upadhyay¹, Ashish Raman¹, Ravi Ranjan^{1*} and Naveen Kumar¹

* ranjan.ravi80@gmail.com Electronics and Communication Engineering , Dr.B.R. Ambedkar NIT Jalandhar, India 144011

¹Electronics and Communication Engineering , Dr.B.R. Ambedkar NIT Jalandhar, India 144011

Abstract

In this paper, the proposed design of H-shaped TFET has been discussed. This design is providing a high I_{on}/I_{off} ratio with better I_{on} . HfO_2 is used for better tunneling current. With this device, Different parameters such as unit parameter, analogue parameter, and linearity parameter have been studied and investigated the output of the H-TFET. As unit parameters, the electric field, electric potential, energy band diagram, and non-local band-to-band tunneling rate (BTBT) have all been observed. Second and third-order harmonics distortion (HD2, HD3), third-order current intercept point (IIP3), third-order intermodulation distortions (IMD3), and second and third-order voltage intercept point (VIP2, VIP3) are evaluated as linearity parameters that characterize the device's distortions and linearity. We obtained $I_{on}=1.6 \times 10^{-4}$ A/ μm , $I_{off}=2.1 \times 10^{-19}$ A/ μm , $I_{on}/I_{off}=7.6 \times 10^{14}$, threshold voltage $V_t=0.3449$ V.

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1. Introduction

We all required a device which has low power consumption, high speed and low area. This requirement is done by scaling of device. Scaling below nanoscale has some drawbacks ex. high power dissipation, short channel effect (SCE) [1]. So, we need a device which have less effected from SCE. Scaling the supply voltage in the case of MOSFETs will reduce power consumption [2]. The effective voltage determines the drain to source current, which can be improved by scaling the threshold voltage. The leakage current increases exponentially as the threshold voltage (V_{th}) is scaled up [3]. Owing to the inability to scale the subthreshold swing (SS) under the boltzmann limit of 60 mV/decade at room temperature [4], the physical geometry of the devices is quickly scaled down, but the power supply of the devices is not scaled down in the very same manner [3]. To address the shortcomings of traditional MOSFETs, a new operating theory has been tested using a particular kind of transistor construction, non-silicon-based materials [3]. So we take TFET for that which have a good I_{on}/I_{off} [5] ratio with low subthreshold swing. Because of the band-to-band tunneling (BTBT) process in TFETs, they have a lower ON-current (I_{on}) than traditional MOSFETs [1]. Low I_{on} , high SSavg, high V_t , small I_{on}/I_{off} , ambipolar currents, and drain driven current improvement due to large silicon bandgap are all disadvantages of standard Si-TFETs [6][7]. Nanotube TFETs have good RF performance. In respect of drive current capacity, energy loss, and area, the NT structure is superior [8][9]. However, if it is to be used in digital devices, the reverse gate bias condition, i.e. ambipolar current, must be reduced [10]. Due to indirect bandgap [6] semiconductor and scattering phenomena, the band-to-band tunneling (BTBT) efficiency in silicon is lower. The current in a MOSFET [1] is measured by the thermionic emission of free charge carriers.

$$I_{thermionic} = e^{v_{gs}/\eta VT}. \quad [1]$$

But It is primarily from BTBT in TFET [5].

$$I_{BTBT} = AE^2 e^{-B/E}. \quad [2]$$

Here from the above equation (2), we understand that the band-to-band tunneling (BTBT) current is exponentially dependent on electric field.

Different novel architectures [11], such as dual gate architecture TFETs, have been developed to enhance the existing drive capabilities (I_{on}) of TFETs [1]. For the improvement in current in TFET, we use different types of structures and architectures of TFET, H-shaped TFET is also one of those structure. The current in TFET is mainly dependent on band to band tunneling current.

II. DEVICE STRUCTURE AND SIMULATION PARAMETERS

Fig.1. 2D structure of proposed design

The proposed structure of Overlapped gate-source/drain H-shaped TFET is shown in fig1. In this design, we have gate is surrounded by channel for more tunneling. Gate is controlling tunneling in both directions. Tunneling is occurring in vertical direction. HfO_2 [12] is used instead of SiO_2 for better I_{off} current. When a gate voltage is applied, electrons are start tunneling from source to channel. Gate is overlapped by the channel. Overlapped area by gate on channel is responsible for the controllability of gate and hence it effects the tunneling rate of carriers.

TABLE I. OPTIMIZED PARAMETERS USED FOR SIMULATION

Parameters	Symbols	Values
Source concentration	N_S	$1 \times 10^{20} \text{ cm}^{-3}$
Channel concentration	N_C	$1 \times 10^{15} \text{ cm}^{-3}$
Drain concentration	N_D	$2 \times 10^{19} \text{ cm}^{-3}$
Source Thickness	w_c	2 nm
Gate oxide thickness	t_{ox}	1 nm
Channel thickness	w_c	2 nm
Gate thickness	g_t	5 nm
Drain length	L_D	20 nm
Channel length	L_C	30 nm
Source length	L_S	20 nm
Gate length	L_G	30 nm
HfO_2 length	-	70 nm

The doping parameters for this device for different sections are shown in Table 1. We take heavily doped p+ source for enhancing I_{on} current, with lightly doped p-channel and moderately doped n+ drain to reduce leakage current. The gate electrode work function is about 4.5 eV. The device parameters channel thickness (w_c), source/drain thickness and gate oxide thickness (t_{ox}), Source/drain length (L_s/L_D), channel length (L_C) are shown in Table I. We use ATLAS Silvaco TCAD tool for the simulation of this design [13]. The tunnelling current for a degenerated P-N junction can be correctly modelled using the non-local BTBT approach in both forward and reverse bias conditions. In the “MODEL” sentence, we used “BBT.NONLOCAL” to allow this model. In addition to the “BBT.NONLOCAL” parameter being defined in the “MODEL” argument, In the region containing a single P-N junction, where quantum tunnelling is required, a mesh must be specified. The non-local BTBT model depicts correct charge carrier tunnelling [14] in the system, with tunnelling occurring at the Source-Channel interface. For proper tunnelling, fine (light) meshing is needed at the Source-Channel interface. At the Source-Channel terminal, quantum meshing (qt mesh) is also performed. For proper tunnelling, the effective mass of an electron is taken 0.22 m_e and the effective mass of a hole is 0.12 m_h [13]. Quantum meshing is carried out in both the x and y directions. In Fermi –Dirac carrier diffusion equations, the Fermi formula is used.

III. SIMULATION RESULTS AND DISCUSSION

The exact type of behaviour of H-TFET can be seen in device parameters like electron/hole concentration, electric field variation, potential variation energy band diagram, and nonlocal band to band tunnelling rate (BTBT).

It is obvious that no tunnelling is feasible in the OFF state, so I_{off} is very weak, while tunneling is possible in the ON state. In fig.2(a), energy band diagram [15] is shown which describes where the tunnelling is possible. At $V_{DS} = 0.5$ V. The OFF state [$V_{DS} > 0$ V and $V_{GS} = 0$ V] is seen in red, while the ON state [$V_{DS} > 0$ V and $V_{GS} > 0$ V] is seen in blue. Caused by the sudden transition in the doping profile from the source to the channel area, the electric field is high [16].

Tunneling range is larger in the OFF state than it is in the ON state. As supply voltage ($V_{DS} = 0.5$ V) is applied, the energy band diagram on the source side is higher than on the drain side. In the ON condition, the drain to source voltage (V_{DS}) raises the valance band (VB) just above conduction band (CB) at the source, tunnelling distance narrows, and further tunnelling at the source-channel interface is possible. The electric potential change along the channel of the H-TFET is seen in fig. 2(b). Source side potential is low, while at the drain, it is high. The power supply and work function of the source and drain metal contacts determine the potential variance through the system. The electric field variations for the Off and ON states is seen in fig. 2(c). At the source-channel terminal, the electric field is at its peak. For the Off state, the tunnelling width is larger and the depletion width is also larger, resulting in a smaller electric field than in the ON state. The electron Band-To-Band Tunneling (e-BTBT) together with channel length can be seen in fig. 2(d). This plot is straight around zero for the Off, indicating that there is no tunnelling occurs, whereas in the ON-state, there is still a significant rise in tunnelling rate near the source channel contact. The figure shows why I_{off} is still so low and I_{on} is really high.

We can get the transfer characteristics by the help of ATLAS Silvaco TCAD tool. The transfer characteristics is shown in fig.2(e). The figure illustrates the drain field is current (I_{DS}) Vs. gate voltage (V_{GS}) at $V_{DS} = 0.5$ V. When the switch is turned on, the drain current is 1.6×10^{-4} A/ μm . The tunnelling width is very short and the electric field is very large at the source channel interface, therefore current is higher. The output characteristics of the proposed device is shown in fig.2(f). Figure 4 depicts the relationship between drain current (I_{on}) and V_{DS} . In the log scale, the I_{on} varies in accordance with the drain voltage. The I_{ON} current value is 1.6×10^{-4} A/ μm . The I_{on}/I_{off} current ratio is in the order of 10^{14} .

First we took some default parameters like oxide material, channel length (L_C), channel thickness(w_c), oxide thickness(t_{ox}). Further we modified parameters to get better results in I_{on} current, I_{off} current and I_{on}/I_{off} ratio.

A. Effect of variation of Oxide Material

First we change oxide material and see which material gives best result. We keep other parameters as unchanged like channel length is 25nm, channel thickness is 10nm, oxide thickness is 2nm for this analysis. In fig.3(c), we can see how transfer character characteristics changes with the oxide materials. Since oxide materials are dielectric and have different dielectric constants, the current value can change. HfO_2 ($k=25$), Al_2O_3 ($k=8$), SiO_2 ($k=3.6$). For HfO_2 , we found that the optimal values of I_{on} , I_{off} and I_{on}/I_{off} are 3.41×10^{-06} A/ μm , 5.76×10^{-18} A/ μm and 5.92×10^{11} A/ μm respectively.

Fig.2. Variation in (a)Energy band diagram (b)Potential (c)Electric field (d)Nonlocal BBT e- Tunneling Rate w.r.t channel length axis (e) Transfer characteristics of proposed TFET (f) Output characteristics of proposed TFET

B. Effect of variation of Channel Length

After oxide material, we change the channel length from 20nm to 40 nm with 5 nm step and optimized result. For this analysis we take HfO_2 as oxide material and keep other parameters constant w_c and t_{ox} as 10nm and 2nm respectively. $I_d - V_{\text{gs}}$ characteristics graph for different values of channel length(L_c) is shown in fig.3(a). By increasing the L_c , I_{off} current will decrease for low V_{gs} values from 0.0 to 0.2 V. The overall $I_{\text{on}}/I_{\text{off}}$ is also increased till $L_c=30$ nm. the highest $I_{\text{on}}/I_{\text{off}}$ obtained at $L_c=30$ nm shown in fig.3(b). For $L_c=30$ nm, we obtained optimal value for I_{on} , I_{off} and $I_{\text{on}}/I_{\text{off}}$ as $3.46 \times 10^{-6} \text{ A}/\mu\text{m}$, $7.8 \times 10^{-19} \text{ A}/\mu\text{m}$ and $4.43 \times 10^{12} \text{ A}/\mu\text{m}$ respectively.

Fig.3.(a)Effect of gate length on I_{DS} - V_{GS} curve. . (b) Effect of gate length on I_{ON}/I_{OFF} ratio . (c)Effect of oxide material on I_{DS} - V_{GS} curve

C. Effect of variation of Channel Width

We try to optimize channel width after we got optimized value for channel length $L_c = 30$ nm, keep this constant for this analysis. We varies w_c from 2 to 6 nm and 10 nm. In fig.4(a), we can see the transfer characteristics of current for different value of w_c . The optimized values at $w_c = 2$ nm for I_{on} , I_{off} and I_{on}/I_{off} are $6.25 \times 10^{-05} A/\mu m$, $1.45 \times 10^{-18} A/\mu m$ and $4.28 \times 10^{13} A/\mu m$ respectively.

D. Effect of variation of Oxide Thickness

We also check optimize value of oxide thickness (t_{ox}) after we got optimized value for channel width. We keep all parameters constant for this analysis. We take two values for t_{ox} 1 nm and 2 nm, and see the variation in drain current in fig.4(b), we can see the transfer characteristics of current for different value of t_{ox} . The optimized values at $t_{ox} = 1$ nm for I_{on} , I_{off} and I_{on}/I_{off} are $1.6 \times 10^{-4} A/\mu m$, $2.1 \times 10^{-19} A/\mu m$, 7.6×10^{14} respectively.

E. Effect of variation of Work Function

We further vary the work function of metal for optimizing the value of I_{on}/I_{off} and SS_{avg} (Subthreshold slope). We found that at work function equal to 4.5 eV, we obtained optimized value for I_{on}/I_{off} and SS_{avg} as 7.6×10^{14} and 32.34 mV/dec respectively. The variation of I_{on}/I_{off} ratio and Subthreshold slope (SS_{avg}) as a function of work function is given in fig.4(c) and fig.4(d) respectively.

Table.2 present a comparison of analog parameters for the various TFET configurations proposed earlier. As we add more improved techniques to get the improved results in our proposed structure, the table shows the increase in I_{on} , I_{off} , I_{on}/I_{off} and SS_{avg} .

Fig.4.(a) Effect of channel width on I_{DS} - V_{GS} curve (b) Variation of t_{ox} with V_{GS} (c) Effect of work function on I_{on}/I_{off} ratio (d) Effect of work function on Subthreshold slope (SS_{avg})

F. RF Parameter Analysis

The parasitic capacitance of the device, including gate capacitance (C_{gg}), gate-drain capacitance (C_{gd}), and cut off frequency (f_T), have been used to assess Frequency response. A rate over which the short circuit current gain

Table.2. COMPARISON OF ANALOG PARAMETERS OF VARIOUS TFET

Parameters Designs	I_{on} ($A/\mu m$)	I_{off} ($A/\mu m$)	I_{on}/I_{off}	SS_{avg} (mV/d ec)
Proposed structure	1.6×10^{-4}	2.1×10^{-19}	7.6×10^{14}	32.34
GAA-TFET[17]	2.58×10^{-8}	7.59×10^{-17}	3.41×10^8	36.24
NT-TFET[18]	5.0×10^{-6}	4.5×10^{-19}	1.1×10^{13}	60
CSNT-TFET [19]	3.1×10^{-6}	4.4×10^{-13}	7.0×10^8	33
GAA-TFET [20]	5.0×10^{-5}	5.0×10^{-10}	10^5	70
LG-TFET [21]	4.7×10^{-7}	8.7×10^{-15}	5.4×10^7	45.7
L-TFET [11]	1.0×10^{-6}	7.3×10^{-15}	1.3×10^8	42.8
TMG-TFET [22]	8.9×10^{-6}	9.3×10^{-14}	9.6×10^7	39.4

achieves unit value is known as the cut-off frequency. This reflects the device's transit time. A connection among f_T , C_{gg} , and g_m becomes $f_T = g_m/2C_{gg}$.

C_{gg} is really the gate to gate capacitor, whereas g_m seems to be the transconductance. Some visual fluctuations of the suggested TFET's cut-off frequency (f_T) or 3-dB frequency are shown in Fig.5. The efficiency for a device at higher frequency being restricted with its cut-off frequency; therefore, the high cut-off frequency will always be desirable. With such a higher cut-off frequency, such device may easily be used for wider band uses. For moreover, its cut-off frequency changes in proportion to the transconductance. Since the improvement in g_m overrides the small increase in C_{gg} , our figure showed how f_T rises as V_{GS} proceeds. The f_T graph, meanwhile, continues to decline once

Fig.5. Variation of (a) f_T , (b) C_{GS} , (c) C_{GD} and (d) C_{gg} as a function of V_{GS}

attaining a peak due to a decline in g_m as well as an increase in C_{gg} value. In analogue circuit applications, transconductance (g_{m1}) is used to relate changes in output current to changes in applied voltage. At constant drain voltage, transconductance (g_{m1}) is defined as the rate of change of drain current w.r.t gate to source voltage. The benefit of a higher transconductance value is that the device's amplification gain would be higher [23].

The expression for g_{m1} , g_{m2} and g_{m3} are given below [16],

$$g_{m1} = \frac{dI_{DS}}{dV_{GS}} \quad \text{at constant } V_{DS} \quad (3)$$

$$g_{m2} = \frac{dg_{m1}}{dV_{GS}} \quad \text{at constant } V_{DS} \quad (4)$$

$$g_{m3} = \frac{dg_{m2}}{dV_{GS}} \quad \text{at constant } V_{DS} \quad (5)$$

In fig.6, transconductance (g_{m1}), second order transconductance (g_{m2}) and third order transconductance (g_{m3}) are shown which are taken at different values of V_{GS} from -0.3V to 1.0V. This analysis is observed at two V_{DS} values i.e. 0.1V and 0.5V.

Fig.6. Variation in (a) g_{m1} , (b) g_{m2} and (c) g_{m3} w.r.t. V_{GS}

G. Linear Parameter analysis

The distortions, and linearity of the system for analogue circuit application are shown by linearity parameters such as HD2, HD3, IIP3, IMD3, VIP2, and VIP3. To see the proper behaviours of proposed device, linearity parameters are very important parameters. The harmonics distortion (HD2, HD3) is high in the transition field, i.e. when switching from ON to OFF. After switching HD2 and HD3 are decreases with increments in V_{GS} value. Variation of HD2 and HD3 at two drain voltage values i.e. $V_{DS} = 0.1V$ and $0.5V$ is shown in fig.7(a) and fig.7(b). We can see that distortion is more at higher V_{DS} value.

The equation for HD2 and HD3 are given below [24]:

$$HD2 = \frac{1}{2} \times V_i \times \frac{\frac{dg_{m1}}{dV_G}}{2g_{m1}} dBm \quad (6)$$

$$HD3 = \frac{1}{4} \times V_i^2 \times \frac{\frac{d^2g_{m1}}{dV_G^2}}{6g_{m1}} dBm \quad (7)$$

Here V_i and g_{m1} are input signal amplitude and transconductance respectively. R_s is source resistance.

At a given operating frequency, the voltage intercept point (VIP) reflects the input voltage during which the 1st and 3rd harmonics can have the same amplitude. VIP2 and VIP3 are 2nd and 3rd order voltage intercept points respectively. Their expression for calculation are shown below:

$$VIP2 = 4 \times \frac{g_{m1}}{g_{m2}} V \quad (8)$$

$$VIP3 = \sqrt[3]{24 \times \frac{g_{m1}}{g_{m3}}} V \quad (9)$$

By the help of VIP3, we can calculate IMD3 (3rd order intermodulation modulation distortion). The amplitude modulation (AM) of a signal with more than one frequency, also known as multi-tone modulation, is defined by IMD3. IMD3 has a value of -14.7561 dBm in our design. By the help of IIP3, we can examine whether the 3rd order harmonics distortions signal amplitude is the same as the reference signal. The IIP3 should have a high value. In our design, IIP3 has a value of -53.8426 dBm at $V_{DS}=0.5V$. The expression for IMD3 and IIP3 are shown below [24]:

$$IMD3 = \left(\frac{9}{2} \times (VIP3)^3 \times g_{m3}\right) 2 \times R_s \text{ dBm} \quad (10)$$

$$IIP3 = \frac{2}{3} \times \frac{g_{m1}}{g_{m3} \times R_s} \text{ dBm} \quad (11)$$

The linearity parameters are shown in fig. 7.

Fig.7. Variations in (a) HD2, (b)HD3, (c)IMD3, (d)IIP3, (e)VIP2, (f)VIP3 with V_{GS} at drain voltage $V_{DS}=0.1V$ and $0.5V$.

IV. CONCLUSION

This paper reveals the proposed H-shaped nanotube tunnel field effect transistor (H-NT-TFET) architecture, which has a higher drain current than other TFET architectures. The device's drain current (I_{on}) is 1.6×10^{-4} A/ μm , and its OFF current (I_{off}) is 2.1×10^{-19} A/ μm , this proposed design exhibit a high I_{on}/I_{off} current ratio, $I_{on}/I_{off} = 7.6 \times 10^{14}$ and threshold voltage $V_t = 0.3449$ V at $V_{DS} = 0.5$ V. By the help of linear parameters, we can say that this proposed design is also used in analog application. This device exhibit harmonic distortion parameters HD2 and HD3 values about 6.69×10^{-3} dBm and 6.8×10^{-4} dBm respectively. Other parameters IMD3 and IIP3 having value about -14.7561 dBm and -53.8426 dBm respectively at $V_{DS} = 0.5$ V. VIP2 and VIP3 has value of 7.466667 V and 1.912366 V respectively at $V_{DS} = 0.5$ V.

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Consent for publication: NA

Availability of data and materials: YES

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Authors' contributions

Utkarsh Upadhyay: Simulation, TCAD Software, Writing- Original draft preparation.

Ashish Raman: TCAD Software, Writing- Original draft preparation.

Ravi Ranjan: Simulation, Data curation and Revision.

Naveen Kumar: Simulation, TCAD Software, Logical-Methodology, conceptualization.

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Compliance with Ethical Standards section

Disclosure of potential conflicts of interest: No conflicts to report.

Research involving Human Participants and/or Animals: NA

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