Mind-Shift: An Method for Power and Energy Reduction inApplication Mapping onto Network-o-Chip architectures

yasin asadi (yasinasadi@hotmail.com)
Islamic Azad University Central Tehran Branch https://orcid.org/0000-0001-8956-6403

Research Article

Keywords: WiNoC, NoC, Mapping, Power, Energy, IoT, WSN

Posted Date: August 24th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-841863/v1

Mind-Shift: An Method for Power and Energy Reduction in Application Mapping onto Network-o-Chip architectures

Yasin Asadi
Department of Computer Engineering, Faculty of Technical and Engineering,
Islamic Azad University Central Tehran Branch, Tehran, Iran.
yasinasadi@hotmail.com

Abstract – Network-on-chip (NoC) is an efficient interconnection designing method for solving the limitations of buses in connecting IP cores. Power consumption is one of the most important issues in this area, solving this problem can lead to a more reliable and efficient design of NoC. Besides, there is another problem which is the More's law is reaching an end. In this paper, we used a new approach, which improves designing points, so we can design NoC architecture more efficiently based on previous designs. Briefly, this method adds one step before the overall change of architecture which tests if the current design can be improved if we change some internal characteristics. For validation, we applied this method by using wire NoC, and changing its bottlenecks, and make them more efficient by using mapping and adding antennas for wireless communication. While this method seems simple at the first sight, but the result can help many designing, which are vital for industries, and technologies like Wireless Sensor Networks (WSN) and Internet of Things (IoT) devices. Briefly, this method can be used in NoC architectures and make them more efficient in a new style for new purposes. The results compared with the basic designing method with the new improved method; power and Energy improvements are respectively 25% and 46% with mapping and wireless improvements and approximately 60% more than traditional NoC in comparison with the basic method in this approach. This method also paves the way for green computing by avoiding producing more chemicals and products from a reusability perspective.

Keywords WiNoC, NoC, Mapping, Power, Energy, IoT, WSN.

1. Introduction

According to the exponential growth in the number of transistors over time which can be integrated into an IC [1], we can integrate several computing systems in one single chip called SoC[1]. The exponential growth makes it possible to integrate many IP-cores[2] in one chip but the traditional bus, which used as a communication backbone for SoCs was not able to handle lots of communication in several IP-cores, but NoC[3]came up with the idea of network communications in many cores and it is still an efficient solution. It proposes the design of modular and scalable communication architectures where various IP-cores are connected to a router-based network using appropriate Network Interface (NI) [2]. Power is an important issue in technology and of course in NoC systems. One of the critical issues in IP-core designing and implementation which plays a significant role in various characteristics is power. By reducing power in NoC we can lead designing to a

[1] System-on-Chip
[2] Intellectual Property
[3] Network-on-Chip

more productive way that makes an overall efficiency for design and products; however the NoC method itself in communication could make improvements, but it has its own challenges. According to the ITRS report [3], more than 88% of consumed power in a chip is consumed on the interconnections, so NoCs still have their problems such as the power and delay issues in long hops and large networks. Wireless communications have wider bandwidth and less power consumption, which better and practical for large NoCs; making a hybrid combination of wire and wireless makes NoCs more flexible for design. In the meantime advances in integrated circuits technologies emerged small antenna technology on chips which is now developed as WiNoC[1] [4]. Mapping is one of the significant parts of NoC design and implementation it maintains the efficiency and integrity of the applications. Mapping is a NP-hard problem; different heuristic methods tried to solve problems of NoC constraints, some of these methods are Nearest Neighbor (NN) and Best Neighbor (BN) [5], [6] which is used grouping methods for starting node. In [7] SMAP has provided a simulation environment that is capable of generating Task-Graphs (TG) and performing mapping, routing, and scheduling efficiently. The SMAP has a flexible and extendable architecture. In addition, there is a critical concern which is vital to solve for industry, the Moore's law; As a consequence of this observation a scaling algorithm was developed in the 1970s, stating that device feature sizes would decrease by a factor of 0.7 every three years[8]. It is a techno-economic model that has enabled the information technology industry to double the performance and functionality of digital electronics roughly every 2 years within a fixed cost, power and area[9]. The problem that we are about to solve is the power and energy reduction in NoC architecture design; it can make longer the usage life of IoT (Internet of Things) and WSN (Wireless Sensor Networks) devices.

2. Related works

In [10] , an incremental approach proposed that can separate two functional segments, a regional selection that begins with the most contiguous node and to the central manager, the task allocation step that adding other nodes in the chosen region keeps nominated new selecting nodes adjoining to the chosen region and in a repetitive mode. Consequently, mapping is run in a selected area. According to the advanced technologies in current decades in computer architecture[11], it is obvious there should be solutions for solving NoC important problems. In general, mapping methods are categorized into two major groups, dynamic (online) mapping, and static (off-line) mapping; this classification is based on the task allocation for processing in the IP-cores. Dynamic mapping finds the performance bottlenecks and then spread workload on the other processors during the execution of the application so it can balance the workload on the execution of the application. Since static mapping is an off-line method task mapping is executed before running the application. It always tries to set the best assignment of tasks, so the mapping is done one time before the execution. in the consequence of the dynamic nature of online mapping, it causes an increase in the communication overhead in the online method, it causes negative effects on the mapping scenario which is cause delay increment in the overall system, so the off-line method is recommended more [2].

[1] Wireless Network-on-Chip

Typically there are two types of IP-cores in NoC topology which are homogeneous and heterogeneous. There are differences in task allocation in heterogeneous IP-cores while in the homogeneous IP-cores all can perform similar tasks [2]. This part of the work is selected in the core selection phase which all phases are shown in Figure 2. Application-specific NoC flow is shown in Figure 2; an overall Mapping view of the work which can make sense of mapping better. In [12], a mapping algorithm for wireless NoC proposed which is reduces both internal and external congestion. This work is consists of three main sections that start with finding the first node to map, then selecting the first task to be mapped, and then the allocation of the remaining tasks to the remaining nodes. In [13] a scheme is proposed which was efficient and also congestion-aware for WiNoC. It is about proposing a congestion-aware platform that reduces internal and external congestions. And also the platform consists of an adaptive routing algorithm that balances utilization of wired and wireless networks a dynamic task mapping approach that tries to minimize congestion probability and a task migration strategy that considers the dynamic variation of application behaviors. In [14] an application mapping method which called TAPP is introduced it is a temperature-aware application mapping while this mapping sacrificing few network performance, it is for many-core processors in NoC designs but it is still an efficient application mapping algorithm to reduce on-chip hotspots. In this paper algorithm "spreads" high-power cores and routers across the chip by performing hierarchical bi-partitioning of the cores and concurrently conducting placement of the cores onto tiles, and achieves high efficiency and superior scalability; this proposed algorithm reduces the temperature and also it has a minimal growth in latency. In [15] an energy efficient method is proposed which is provide this efficiency without performance penalties for wireless NoC and multiple VFI[1] based designs can decrease the energy dissipation in multicore platforms by taking advantage of the varying nature of the application workloads. In this paper, authors explore the paradigm of wireless NoC and demonstrate that by incorporating WiNoC, VFI, and dynamic V/F tuning synergistically, it can be designed energy-efficient multicore platforms without introducing noticeable performance penalty. The proposed approach can achieve between 5.7% and 46.6% EDP[2] savings over the state-of-the-art system and 26.8% and 60.5% EDP savings over a standard baseline non-VFI mesh-based system[15].

An adaptive multi-voltage scaling in WiNoC for high-performance, low power applications is proposed in [16]. In this work authors proposed a novel design methodology for energy-efficient WiNoC using AMS[3], which reduces dynamic power consumption, along with power gating to prevent static power dissipation in routers and wireless interfaces; this approach saves up to 62.50% of static power with less than 1% area overhead. the proposed WiNoC reduces overall packet energy dissipation up to 35% on average compared to a regular WiNoC in different traffic scenarios[16].

In [17] LAWI[4] is proposed, this work is proposed to bridge the widening gap between the communication efficiency and computation requirements of gigascale system-on-chip devices. It comprises of an intelligent router that balances the traffic load across long

[1] Voltage Frequency Island
[2] Energy-Delay Product
[3] Adaptive Multi-Voltage Scaling
[4] Load Balanced Architecture For Wireless Network on Chip

distance transmission and reduces the congestion delay. An efficient low-cost deadlock-free routing scheme LAWIXY has been proposed that reduces the network congestion and improves the performance of the wireless network-on-chip. It is demonstrated that LAWI outperforms its counterpart network architectures and improves performance for larger system sizes [17]. One of the recent methods, which gain interesting achievements, called "opportunistic beamforming in wireless Network-on-Chip" which instead of combating coupling, aims to take advantage of close integration to create arrays within a WNoC. The proposed solution is opportunistic as it attempts to exploit the existing infrastructure to build a simple reconfigurable beamforming scheme. Which despite the effects of lossy silicon and nearby antennas, within-package arrays achieve moderate gains and beamwidths below 90°, a figure which is already relevant in the multiprocessor context [18]. In addition, this method can be applied on the fault tolerance in mapping since we can update the mapping we can impediment enhanced method to make the end device more efficient in performance also fault tolerance has potential for decreasing energy and chip overall heat. As an example in this work [19], they made a good result in decreasing energy consumption by using task mapping and scheduling, so we have to take advantage of using newer methods for older architectures as possible as they can. However, previous researches mostly used conventional NoCs, in this paper we tried to solve the power problem using the wireless mapping method. In [20] there is a literature review of published antennas technologies, characteristics, future challenges and more useful information about antennas in WiNoC. Additionally In [21] there is a wider survey about WiNoC which is presented a more extensive review about the WiNoC architecture; it also mention its problems and challenges including topology, routing, flow control, antenna and reliability.

3. Problem

Duo to the fast-developing technologies mostly in processors used in devices like IoT based devices and WSN based devices like Underwater-WSN (UWSN), they need fast development approach methods for new versions of hardware device. The consolidation of the physical and digital world over the traditional Internet paved the way for the future these technologies. Since the IoT is envisaged as the network model to fill the gap between the cyber and physical world. The core concept of the IoT is to connect the pervasive objects around us, such as Radio Frequency Identification (RFID) tags, mobile devices, sensors and actuators to the Internet through a wired or wireless network. Hence, it enables the objects to interact with each other and their neighbors to enhance the efficiency of the system [22]. The critical parts of these technologies are the IP-core technologies, since the devices in IoT and WSN are mostly remote and have a long up-time life, so we need an approach for helping real-world technologies. For instance, in projects with remote or autonomous robotic devices and new WSN based projects, which have a long distance between nodes, and sometimes out of reach for development, they need such an approach to help them to develop a device with IP-cores, which can update to a new version without hardware architecture. Another example is using this approach for designing WSN devices that spread in vast areas like jungles, seas, or autonomous robots, which planned to send to other planets for exploration missions, etc. WSN devices mostly spread in vast areas like jungles, seas, oceans and meteorological WSN devices.
These devices need a long period of life for working continuously. However, the cost and changing these technologies sometimes are very time consuming; and in some cases very

hard to replaces or substituted by newer architectures. As mentioned before, the end of Moore's law is become a new concern for technology development we have to add this to these issues too. Therefore, the best way is not much changing the physical device in newer versions in case of compatibility, since this change can be considered in newer devices so in a future version of the devices they just need to update a better method such as mapping for IP-cores. Besides, WSNs are among the most emerging technologies, thanks to their great capabilities and their ever-growing range of applications. However, the lifetime of WSNs is extremely restricted due to the delimited energy capacity of their sensor nodes [23]. That is why energy conservation is considered as the most important research concern for WSNs. Radio communication is the utmost energy consuming function in a WSN [23]. Thus, energy-efficient approaches are vital for saving energy and consequently prolong the lifetime of devices in this case WSNs. For this reason, numerous protocols proposed for energy-efficient routing in WSNs. This article offers an approach that makes it possible to have a cumulative view of technological methods and tools to prolonging the life of the device, by decreasing the power and energy. Thus, by using less new devices and creating the devices by the capability of being update or update current devices by new approaches it can be a small but efficient help for environment and green computing too. The problem, which solved in this paper, is the power and energy problems by reducing them in NoC architectures. The approach of this paper can apply in the most NoC and IoT based architectures since the main architecture concepts is similar to each other. We proposed a method to make NoC designs more flexible, while existing architectures are suitable and competent for continue their service, but critical problems like power and energy consumption make it serious to continue their lives. If we can solve power and energy consumption problem they can continue their services. As mentioned before, the end of Moore's law is become a new concern for technology development, and this problem should be solved. Advances in silicon lithography have enabled this exponential miniaturization of electronics, but, as transistors reach atomic scale and fabrication costs continue to rise, the classical technological driver that has underpinned Moore’s Law for 50 years is failing and is anticipated to flatten by 2025[24]. By now, this prediction has proven to be accurate enough that it has become a solid-state electronics industry target that must be met by semiconductor device manufacturers in order to remain competitive[8]. So there should be various solution for solving this problem because we are changing ages a new age of hunger for more computation and the lack of power and energy besides the reaching the end for Moore's law. In this paper, we propose a method that can help devices to continue their life without needing manipulation in the architecture of their IP-cores. As in [9] declared for meeting the requirements of the new devices, such requirements could necessitate a substantial technological shift. This transition will require not years, but decades, so whether the semiconductor roadmap has 10 or 20 years of remaining vitality, researchers must begin now to lay a strategic foundation for change. Therefore, we named this method "Shift-Map" since it is a shift in design thinking.

4. Methodology (better to change to method)

The presented method in our work is simple but effective. Instead of transformation to a new model, we propose to use current architecture design, but with reconsidering in some parts in this case communications, this step not considered as one important step in the

procedure of designing or improving new architectures. This idea can shape a new vision for designing and computer architecture. We propose this method needs to be considered as a step in the procedure of reusability and design of NoC's architecture. The methods goes like this, when there is a need for upgrade the devices particularly in IoT and WSN devices in this case. Mostly the devices can do their tasks well, but there is a shortage of resources, for instance battery capacity shortage, which is the power and energy problem, or in WSN devices, it is more critical since the wireless communications consume lots of battery resource. For solving these kind of problems that are related to power and energy, we suggest to use this method, which we call it "Mind-Shift" because we changed our thinking from older solutions to novel solutions. Mind-Shift method says that if you have power or energy shortage and the system can continue the work with previous architecture design. The first step for problem solving is not to replacing built-in structure and architecture, but change the mapping and resource allocation inside of whole manipulation of the IP-cores architecture, it will help the architecture to perform better and more efficiently than the traditional solutions and architectures. Then we can use other alternative utilities manipulations like wireless communications and other possible alternations if possible due to the device needs. We propose that designers can use this method as a step in their experimental designs too. For instance, when designers are designing an architecture they can check if this method can help them in their development, which most of the times can make effective differences in the designing of the IoT and WSN devices.

In real-world projects, sometimes there are no more room for change the architecture design entirely; and the cost of design high and it is an issue too. Therefore, not only redesigning is not easy but also it is not profitable and time consuming too. Even if entire redesign is possible, obviously the cost of design and production increases. Thus, we propose this method for easier, faster, and time saving solution.

This method makes reusability more practical for the former architectures, which can continue their effective performance life just like before. This method not only make improvements on power and energy, but also it can improve performance of devices too. If IoT or WSN devices has performance and executing issues, we can see if this method can solve the problem at the first place and then we can chose the problem solving technical path for redesign or repairing it. Since this paper is about testing power and energy, other criteria can be researched as future works.

Since NoCs are fast growing and replacing the for SoC architectures. In addition, Early stage performance modeling is a critical step in NoC design for design space exploration and achieving efficient topologies within Time-To-Market (TTM[1])demands[25]. Using this method can be a positive point in real-world economy and production of devices, since it can save lots of time on Time-To-Market (TTM), which is an important criterion that is very important factor in technological advances and today fast growing and competing economy. This paradigm-shift can start a vast impact on technologies that are related to and capable of continuing their services while their construction technology is outdated. Though the IoT and WSN devices are developing very quickly such method

[1] In commerce, time to market (TTM) is the length of time it takes from a product being conceived until its being available for sale. The reason that time to market is so important is because being late erodes the addressable market that you have to sell your product into.(https://en.wikipedia.org/wiki/Time_to_market)

can help designers and companies to release product much faster. Green computing can improve by using this method, not only we can solve energy and power problem but also we can also be effective in the green computing field which by default will be reduced the production of unnecessary devices because now we can upgrade. This is a multidisciplinary method, which can help computer engineering in many phases.
Therefore, we need a method that makes less variation and the best possible impact on design. Since the new technologies are growing fast and most of the computational infrastructures based on many-cores architecture processors, the problem of power is still serious problem, which Mind-Shift is a solution to some of it issues.

5. Proposed work

For validation of this method, we decide to use it in NoC designing which is using in many IoT and WSN architectural design. We want to reduce power and energy in NoC architecture using Mind-Shift approach that introduced. First we impediment a traditional NoC design and then we add a mapping change then we add more changes like antenna and wireless it to so we can validate this method. Traditional NoC is simple just using wire architecture with no wireless and specialized mapping and scheduling, the For Mapping part we used DSM[1] algorithm which is used in [26], this method is using spiral mapping SMAP[7] which is allocated information to IP-cores on NoC for processing. The most important task is located at the central place for mapping and other tasks will be mapped spirally around the central place and it goes to the boundaries of the NoC mesh and it will keep most related cores adjacent together as possible. The purpose of this proposed design is to reduce the power in the NoC in comparison to the previous design, so to achieve the power reduction we decided to implement it in a wireless mapping communication. We choose Mind-Shift (paradigm shift) in shifting the communication to reuse this architecture and reduce power consumption so this architecture can continue its life.
DSM policy is based on a set policy, which is set priorities in the middle of an operation. In order to organize and allocating tasks and communications In the process of Mapping, there is some level which is necessary for Mapping and they are designed in the structure of mapping, this cause an application to be separated into multiple parts which are independently known as a task; Task Graph (TG) makes the tasks intercommunications more clear. The Task Graph consists of various transformation transactions, supposing that IP-cores are ready for mapping in the sequence of their task priority (which should be sequenced) on a mesh network this list should be mapped by the proposed order that determined in advance. The middle IP-cores connections are more than marginal IP-cores which is why produce a PPL (Platform Priority List) this make it possible a central start and also a marginal ending in spiral approach [26], we used wireless antennas in infrastructure these antennas are based on CNTs[2] technology while this is similar to the approach which is presented in [27] but it is using a non-hybrid approach. In this work

[1] Dynamic Spiral Mapping
[2] Carbon Nanotubes

we used wireless application mapping by wireless antennas in order to reduce power and energy.

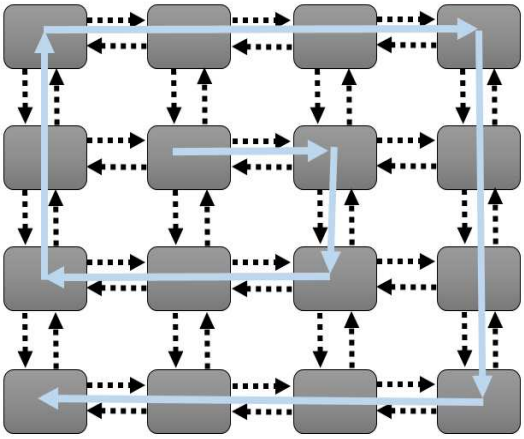

Figure 1. Proposed wireless spiral mapping

In this work, we used a wireless mapping approach in order to reduce the power consumption so it can make a faster communication between IP-cores that caused power reduction. The wireless communication is one of the crucial connections, which carry out wireless mapping. Most mappings do not use it as a means for power reduction so in this case we used it for solving power and energy problem.

5.1 Application mapping

Application mapping regulates how the application is assigned onto the NoC architecture (figure 3). Mapping can be done in different ways depending on the main performance metrics, like optimization energy consumption, execution time, etc. However, there are several platforms with different network topologies, but one simple and most feasible example for NoC can be a 2-D mesh network [13].
We can classify user operations, jobs and tasks in application branch, and an application should be separated to many parts, which is caused to creating a Task Graph (TG); these tasks will allocated to IP-cores and would have a certain task scheduling and clear task communications. A Task-Graph (TG) is made up of sequences of transactions, an example of TG is shown in Figure 3.
In order to allocate the tasks there would be some rules which make this allocation prioritized; these rules are shown below [26]:

1. The tasks that have higher data transfer sizes are placed nearest possible position to each other to satisfy the bandwidth constraint.
2. The tasks which are tightly related should have the least possible Manhattan distance on the mesh platform.
3. The tasks which have the high connection degrees should not be placed on the boundaries. For these tasks, the central area of the mesh is the best candidate

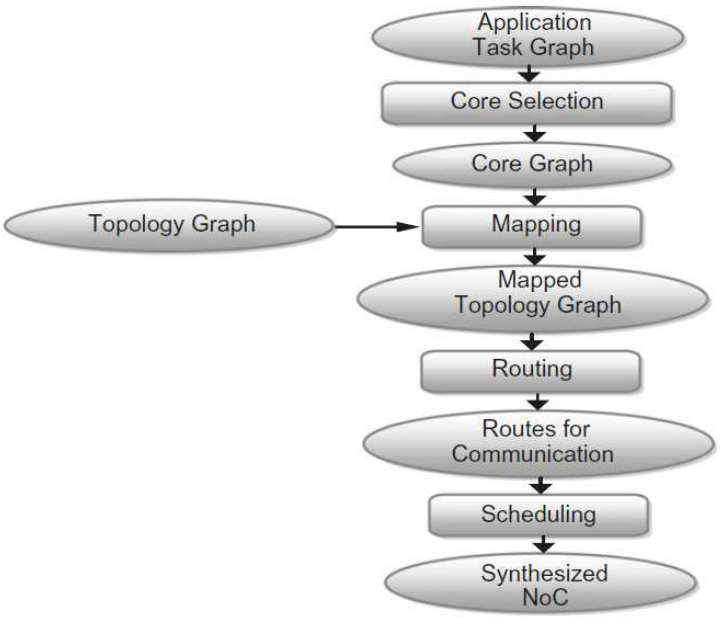

Figure 2: Application-specific NoC design flow [2]

Figure 1 shows the proposed architecture and the mapping method in wireless infrastructure which dots are wireless connections.

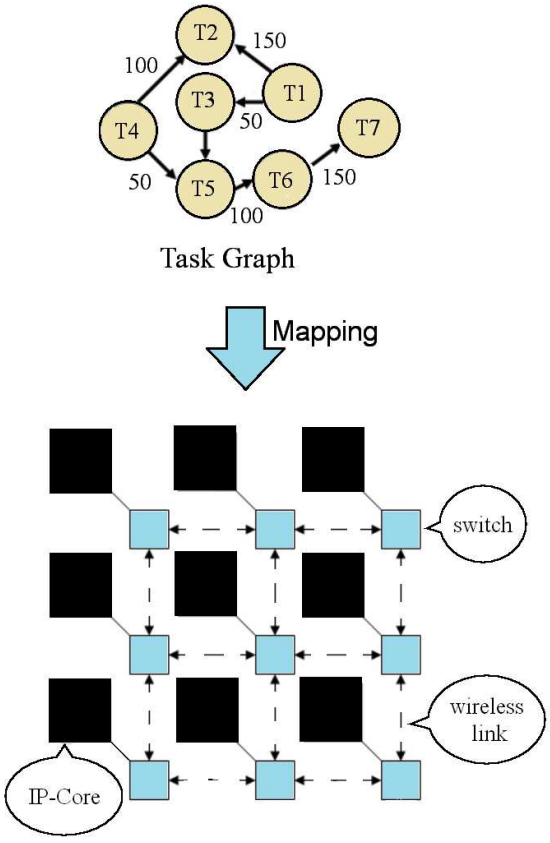

Figure 3: Task Graph symbolic illustration of 2D wireless NoC

2.1 Pseudo codes

In this section we propose pseudo codes of spiral algorithm that is used in wireless method in this work; the following pseudo code is about choosing nodes pseudo code.

```
1. While there is task to be mapped
2. if ( the task is highly connected AND there is free node for allocation) then
3. node
4. else if ( the task is NOT highly connected AND there is free node for allocation) then
5. choose no central node to be task
6. else if (there is NOT free node for allocation)
7. go suspend and next task will start
8. end
9. return the node to be mapped
```

Figure 4: choosing nodes pseudo code

In this pseudo code, we have shown a brief form of spiral pseudo code which is used in this research:

```
1. while there is no unmapped task map the current task to be mapped to the till the whole current task is
   over
2. the current task to be mapped: choose next task from the task graph in breadth-first order
3. spirally map the task
4. While there is task not done
5. find suitable node then
6. allocate the task then go to next task
7. if the task is done go get the next job in scheduler
8. end
9. the current node to map: choose next node spirally
10. map the current task to be mapped to the till the current task is over
11. end
```

Figure 5: spiral pseudo code

The following information used in simulation and implementation:

- The injection rate is equivalent to the average number of messages in each cycle, which is injected in every node.
- The infrastructure of this research is 10*10 nodes.
- Task graphs which are used for this work are (25, 15, 15, 10) task graphs.
- Scheduling that used in this research is FCFS that it allocates them to nodes.
- For sake of simplicity homogeneous architecture used as system architecture.
- In addition, 2D mesh topology is chosen for topology simplification.

6. Tools

In simulation we used two kinds of simulators OMNeT++ and MATLAB; OMNeT++ is a discrete event simulation environment, OMNeT++ was designed to be as general as possible. OMNeT++ has been used in numerous domains from queuing network simulations to wireless and ad-hoc network simulations, from business process simulation to peer-to-peer network, optical switch and storage area network simulations[28]; also, this simulator supports the NoC and wireless NoC implementation. This simulation

approach is an object-oriented approach, which all objects created independently and they will be linked together then executed in the simulator. Also, MATLAB is another simulator which is used in this work.

7. Scheduling

There are many task-scheduling methods that make a better task allocation possible for task scheduling. While every task scheduling is chosen regard to nature of the application and tasks we here elected one a simple generic application scheduling which makes this research an academic base research with less specific situations so it can be used in other researches simpler, in order to simplification of this research and regarding to simplicity, we used a FIFO scheduling.

8. Result and analysis

In this research, to reduce power with proposed method and spiral NoC Mapping infrastructure, we changed wire spiral mapping method into wireless method. Moreover, we used low antenna technology that fulfills the research objective afterward we compare the results; not only this method could achieve results in power reduction but also it achieved results in energy reduction; the simulation results are discussed below.

8.1 Power and Energy

We compared the base method with the new improving method; average energy comparison results are shown in Figure 6. It shows the improvement in power in spiral and wireless spiral; in this figure, it is obvious that wireless method has improvements by increasing injection rate we have increment in power consumption but still it is less than the wire method. Subsequently, due to improvements, this method was successful and the objectives achieved.

8.2 Power and Energy model

Power model which is used in this work is presented in [29]:

$$\mathbf{P} = \sum_{r \in PE} P_{r_{buf}} + P_{r_{arbiter}} + P_{r_{crossbar}} + P_{r_{link}} \quad (1)$$

Where P_{r_buf} is the average buffer power consumption including both dynamic and static power, $P_{r\_arbiter}$ is the average power consumption in the routing computation, $P_{r\_crossbar}$ is the average crossbar traversal power consumption, and P_{r_link} is the average link power consumption between neighboring routers. In [30] a power model has presented which energy of one-bit transmission is:

$$E_{bit} = E_{sbit} + E_{lbit} \quad (2)$$

Where E_{sbit} is switch energy consumption for one bit and E_{lbit} is energy consumption for link for one bit. In [30] there is an energy model by assumption of equal energy the consumption for links and switches, we have transportation energy from t_i to t_j as below:

$$E_{bit}^{t_i,t_j} = n_{hops} \times E_{sbit} + (n_{hops} - 1) \times E_{sbit} \quad (3)$$

Where n_{hops} is the number of routers the bit traverses from t_i tile t_j. It is interesting to note that, with (3), the communication energy consumption can be analytically calculated independently of the underlying traffic model (e.g., Markovian, long-range dependence, etc.[31]) provided that the communication volume between any communicating IP pair is known. In [32] used a formula for calculating the total energy; total energy consumption for data transportation is data size in the energy consumption for a link in one bit which is presented in (4).

$$E_{bit}^{ti,tj} = Datasize_{t_i,t_j} \times E_{bit}^{ti,tj} \quad (4)$$

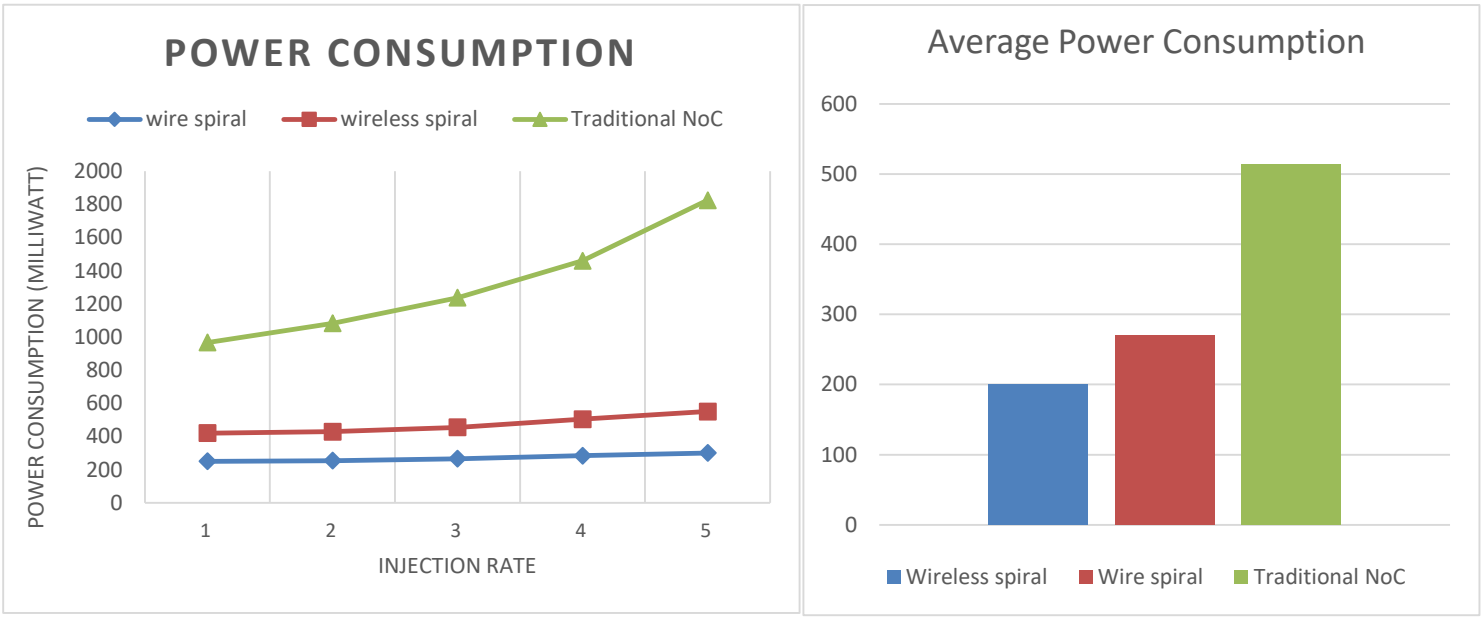

Figure 6: Power consumption comparison and Average power consumption comparison

Average result comparison shows the same result in improvements; these results are shown in Figure 6, this improvement is approximately more than 25% more in this approach rather than wire approach. Energy improvement is approximately more than 46% more in this approach, which is shown in

Figure 7; as it is shown the proposed approach can make enhancement in energy consumption too. It is obvious that improvements approximately 60% more than traditional NoC design which did not use special mapping and wireless improvements.

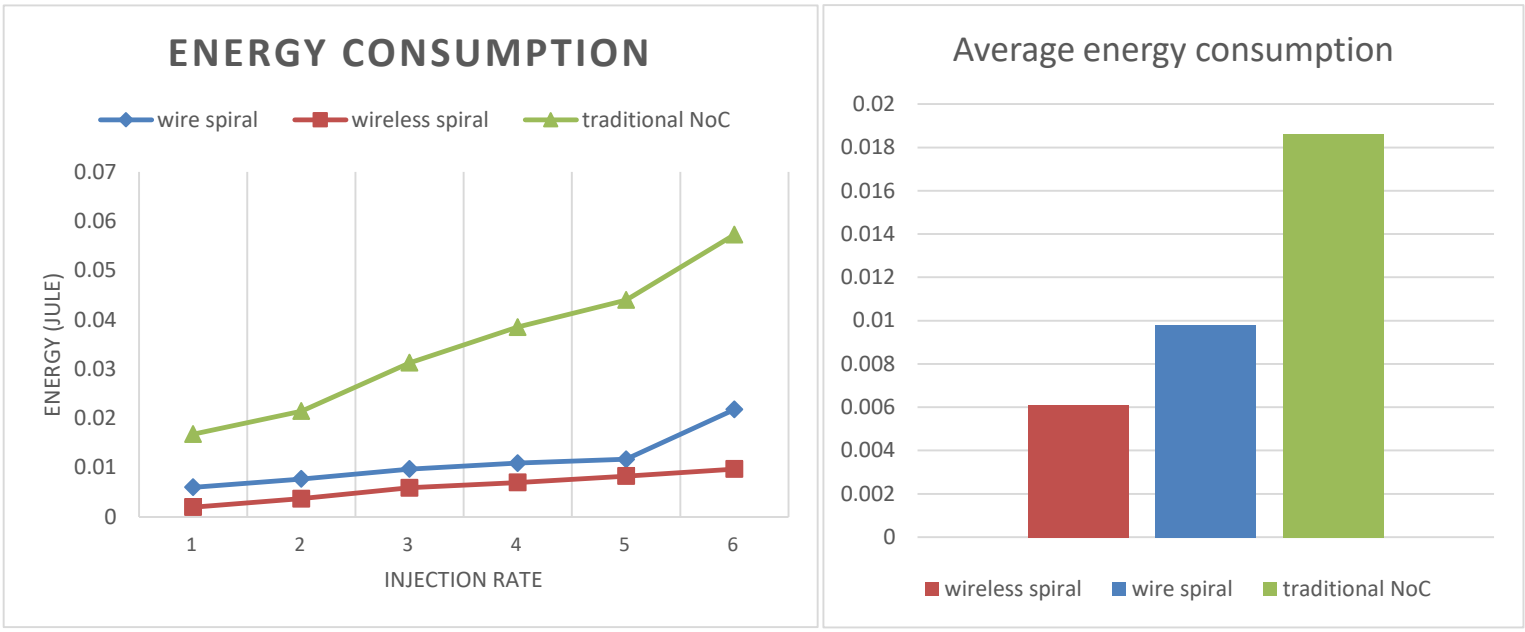

Figure 7: Energy consumption comparison and average energy consumption

These results show the capability of this approach for power, and delay reduction in NoC architecture with other characteristics could be examined with this approach, and we can get more improvements. The graphs also showing the Traditional NoC power and energy consumption for comparison too. As a final point, if this method consider as standardize starting step for architecture design in WSN and IoT devices, it can create a room for future technologies, which will come later in future, and these architectures with such capabilities which Mind-Shift method provide it would be more flexible to technology improvements.

9. Future works

In this research, we achieved improvements in power and energy, which is very important for NoC design. Other factors such as delay and thermal in NoC infrastructure can considered with this approach in future researches. while this approach used for 2-D NoC architectures, other platform can use this method for power and energy improvements like other variations of NoC, 3D NoC and hybrid kind of that like 3D-WiNoC, as primary speculations in 3D-NoC has improvements it can be a case study for future researches. There are many aspects of designing which can improve with this approach in the future works. The technologies that are emerging in the age of end-of-scaling CMOS, silicon photonics are perhaps the most promising to enable a smooth transition toward a new generation of post-CMOS computing systems [33]. Therefore, Mind-Shift method can use with such technologies and gain more efficiency improvements. This approach can be useful in making reusable the architectures for future design of NoC in IoT and WSN

technologies. It will help producing less toxic chemicals in the technology and industry and help to Green Technology because producing less toxic and harmful chemicals results in keep the nature cleaner.

This approach improve NoC architectures to goals of Green computing into more promising horizons, it also equip other new ideas with the advantages of reusability so the technological devices can live longer and also pave the way for new green technological solutions and devices. As a recommendation for future researches, this method can be implemented in routing and scheduling too. By using this method, we can make more efficiency in power and energy in NoC architectures. As mentioned earlier, this method not only is effect the power and energy but also it can improve performance of the devices too. If IoT or WSN devices has performance and executing issues, we can see if this method can solve the problem at the first place and then we can chose the problem solving technical path for redesign or repairing it. It can examined in more extended details in the upcoming researches and papers. This method tested for NoC design in WSN and IoT devices, generalization of this method to more general-purpose processors needs more research and tests that can be done as future works.

10. Conclusion

In this research, we used a creative design method that can make improvements in power and energy for NoC architectures particularly in IoT and WSN related devices. The method is simple but effective; instead of overall changes, we just make important related impactful changes as the first plan for improvements. Due to the fast-developing technologies and usage of technology mostly in processors used in devices like IoT based devices and also WSN based devices, we need fast development approach methods for new hardware's device versions. Since the devices in IoT and WSN are mostly remote and have a long uptime, we need an approach for helping real-world technologies. For instance, in projects with remote or autonomous robots, and new WSN based devices, which are out of reach of technicians for development, they need such an approach to help them to develop a device with IP-cores, which can updated to a new version without hardware architecture. Power is a critical characteristic in NoC design and implementation; solving this issue is one of the most important aspects of NoC design. In this paper, we used a paradigm-shift which can change some design points so we can get more efficient results; the novel part of this work is the usage of a method we called “Mind-Shift”, this method can be used in earlier or current architectures and make them more efficient for a new purpose with new technologies. Since the application mapping is one of the important characteristics, improving it make general improvements in most cases such as power, so we used mapping as a tool for power reduction. Briefly, for validation and comparison of results, we compared the base designing method with the new improved method; power improvement is 25% better and Energy improvement is 46% better than the base method in this approach. We noticed the range of influence of this method in the multidisciplinary and real-world economy and Green Computing too. Using this method can cause reductions in economic expenses too, because using this method influence the time of device production. We recommend this method because of its simplicity, ease, speed, and time-saving. This approach can be used not only in NoC design and implementation but also in the designing and implementation of other chip-

based designs such as WSN, IoT devices too. It is recommended that considering this method as one of the first in designing solutions. This method tested for NoC design in WSN and IoT devices, generalization of this method to more general-purpose processors needs more research and tests that can be done as future works.

11. Declarations

11.1 Availability of Data and Materials

Not applicable

11.2 Competing Interests

The authors declare that they have no competing financial, professional or personal interests that might have influenced the work described in this manuscript.

11.3 Funding

Not applicable

11.4 Acknowledgements

Not applicable

11.5 Abbreviations

Abbreviation	Description
AMS	Adaptive Multi-Voltage Scaling
CNT	Carbon Nanotubes
DSM	Dynamic Spiral Mapping
EDP	Energy-Delay Product
IoT	Internet of Things
IP	Intellectual Property
LAWI	Load Balanced Architecture for Wireless Network on Chip
NI	Network Interface
NoC	Network-on-Chip
SoC	System-on-Chip
VFI	Voltage Frequency Island
WiNoC	Wireless Network-on-Chip
WSN	Wireless Sensor Networks
UWSN	Underwater Wireless Sensor Networks

11.6 Author Information

Yasin Asadi, M.Sc. in computer engineering from Islamic Azad University, Computer engineering researcher, Interested in computer engineering research particularly in Network-on-Chip, IoT, Computer Networking and also interested in Multidisciplinary approaches in computer science related fields, and Professional member of Association for Computing Machinery (ACM) also member of young researchers and elite club, Iran. E-mails: yasinasadi@hotmail.com, asadiy@acm.org

12. Reference

[1] A. J. and H. Tenhunen, *Networks on Chip*. Kluwer Academic Publishers, 2003.

[2] P. K. Sahu and S. Chattopadhyay, "A survey on application mapping strategies for network-on-chip design," *J. Syst. Archit.*, vol. 59, no. 1, pp. 60–76, 2013, doi: 10.1016/j.sysarc.2012.10.004.

[3] S. I. Association and others, "International Technology Roadmap for Semiconductors, 2007," *URL http//www. itrs. net/Links/2006Update/2006UpdateFinal. htm*, 2006.

[4] M. F. Chang *et al.*, "CMP Network-on-Chip Overlaid With Multi-Band RF-Interconnect.pdf," in *High Performance Computer Architecture, 2008. HPCA 2008. IEEE 14th International Symposium on*, 2008, pp. 191–202.

[5] E. Carvalho, N. Calazans, and F. Moraes, "Heuristics for dynamic task mapping in NoC-based heterogeneous MPSoCs," in *Proceedings of the International Workshop on Rapid System Prototyping*, 2007, pp. 34–40, doi: 10.1109/RSP.2007.26.

[6] E. L. de Souza Carvalho, N. L. V. Calazans, and F. G. Moraes, "Dynamic task mapping for MPSoCs," *IEEE Des. Test Comput.*, vol. 27, no. 5, pp. 26–35, 2010.

[7] A. M. S. Saeidi, A. Khademzadeh, "SMAP: An intelligent mapping tool for network on chip, in: International Symposium on Signals, Circuits and Systems (ISSCS)," pp. 1–4, 2007.

[8] L. B. Kish, "End of Moore's law: Thermal (noise) death of integration in micro and nano electronics," *Phys. Lett. Sect. A Gen. At. Solid State Phys.*, vol. 305, no. 3–4, pp. 144–149, Dec. 2002, doi: 10.1016/S0375-9601(02)01365-8.

[9] J. Shalf, "The future of computing beyond Moore's Law," *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 378, no. 2166. Royal Society Publishing, Mar. 06, 2020, doi: 10.1098/rsta.2019.0061.

[10] C. L. Chou, U. Y. Ogras, and R. Marculescu, "Energy- and performance-aware incremental mapping for networks on chip with multiple voltage levels," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 27, no. 10, pp. 1866–1879, 2008, doi: 10.1109/TCAD.2008.2003301.

[11] L. Benini and G. De Micheli, "Networks on Chip: A New Paradigm for System on Chip Design," in *Design Automation and Test in Europe*, 2002, pp. 418–419.

[12] A. Rezaei, M. Daneshtalab, D. Zhao, F. Safaei, X. Wang, and M. Ebrahimi, "Dynamic application mapping algorithm for wireless network-on-chip," *Proc. - 23rd Euromicro Int. Conf. Parallel, Distrib. Network-Based Process. PDP 2015*, 2015, doi: 10.1109/PDP.2015.14.

[13] A. Rezaei, M. Daneshtalab, M. Palesi, and D. Zhao, "Efficient congestion-aware scheme for wireless on-chip networks," in *Parallel, Distributed, and Network-Based Processing (PDP), 2016 24th Euromicro International Conference on*, 2016, pp. 742–749.

[14] D. Zhu, L. Chen, T. M. Pinkston, and M. Pedram, "TAPP: Temperature-aware application mapping for NoC-based many-core processors," in *Proceedings of the 2015 Design, Automation & Test in*

Europe Conference & Exhibition, 2015, pp. 1241–1244.

[15] R. G. Kim, W. Choi, Z. Chen, P. P. Pande, D. Marculescu, and R. Marculescu, "Wireless NoC and Dynamic VFI Codesign: Energy Efficiency Without Performance Penalty," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 24, no. 7, pp. 2488–2501, 2016, doi: 10.1109/TVLSI.2015.2512611.

[16] H. K. Mondal, S. H. Gade, R. Kishore, and S. Deb, "Adaptive multi-voltage scaling in wireless NoC for high performance low power applications," in *Proceedings of the 2016 Design, Automation and Test in Europe Conference and Exhibition, DATE 2016*, 2016, pp. 1315–1320.

[17] P. Mitra, "LAWI: A load balanced architecture for wireless network on chip," in *2016 International Conference on Advances in Computing, Communications and Informatics, ICACCI 2016*, 2016, pp. 349–355, doi: 10.1109/ICACCI.2016.7732071.

[18] S. Abadal *et al.*, "Opportunistic beamforming in wireless network-on-chip," in *Proceedings - IEEE International Symposium on Circuits and Systems*, 2019, vol. 2019-May, pp. 1–5, doi: 10.1109/ISCAS.2019.8702417.

[19] N. Chatterjee, S. Paul, and S. Chattopadhyay, "Task mapping and scheduling for network-on-chip based multi-core platform with transient faults," *J. Syst. Archit.*, vol. 83, pp. 34–56, Feb. 2018, doi: 10.1016/j.sysarc.2018.01.002.

[20] W. Rayess, D. W. Matolak, S. Kaya, and A. K. Kodi, "Antennas and Channel Characteristics for Wireless Networks on Chips," *Wirel. Pers. Commun.*, vol. 95, no. 4, pp. 5039–5056, 2017, doi: 10.1007/s11277-017-4144-0.

[21] S. Wang and T. Jin, "Wireless network-on-chip: A survey," *J. Eng.*, vol. 2014, no. 3, pp. 98–104, 2014.

[22] A. Nauman, Y. A. Qadri, M. Amjad, Y. Bin Zikria, M. K. Afzal, and S. W. Kim, "Multimedia internet of things: A comprehensive survey," *IEEE Access*, vol. 8, pp. 8202–8250, 2020, doi: 10.1109/ACCESS.2020.2964280.

[23] C. Nakas, D. Kandris, and G. Visvardis, "Energy efficient routing in wireless sensor networks: A comprehensive survey," *Algorithms*, vol. 13, no. 3, p. 72, 2020, doi: 10.3390/a13030072.

[24] J. Shalf, "The future of computing beyond Moore's Law," *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 378, no. 2166. 2020, doi: 10.1098/rsta.2019.0061.

[25] S. H. Gade, A. Gangwar, A. Prasad, N. K. Agarwal, and R. Sreedharan, "An Automated Traffic Generation Framework for Performance Evaluation of Networks-on-Chip for Real World Use Cases," in *Proceedings - 2021 IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS 2021*, 2021, pp. 81–83, doi: 10.1109/ISPASS51385.2021.00022.

[26] A. Mehran, A. Khademzadeh, and S. Saeidi, "DSM: A Heuristic Dynamic Spiral Mapping algorithm for network on chip," *IEICE Electron. Express*, vol. 5, no. 13, pp. 464–471, 2008, doi: 10.1587/elex.5.464.

[27] P. P. Pande and K. Chang, "Hybrid Wireless Network on Chip : A New Paradigm in Multi-Core Design," *NoCArc*, pp. 71–76, 2009.

[28] A. Varga and R. Hornig, "AN OVERVIEW OF THE OMNeT++ SIMULATION ENVIRONMENT," in *Proceedings of the First International ICST Conference on Simulation Tools and Techniques for Communications Networks and Systems*, 2008, p. 60, doi: 10.4108/ICST.SIMUTOOLS2008.3027.

[29] J. Kim, D. Park, C. Nicopoulos, N. Vijaykrishnan, and C. R. Das, "Design and analysis of an NoC architecture from performance, reliability and energy perspective," in *2005 Symposium on Architectures for Networking and Communications Systems, ANCS 2005*, 2005, pp. 173–182, doi: 10.1109/ANCS.2005.4675277.

[30] J. Hu and R. Marculescu, "Energy- And performance-aware mapping for regular NoC

architectures," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 24, no. 4, pp. 551–562, 2005, doi: 10.1109/TCAD.2005.844106.

[31] G. V. Varatkar and R. Marculescu, "On-Chip Traffic Modeling and Synthesis for MPEG-2 Video Applications," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 12, no. 1, pp. 108–119, 2004, doi: 10.1109/TVLSI.2003.820523.

[32] S. Saeidi, F. Vardi, and A. Khademzadeh, "Application mapping scenarios onto network on chip based priority lists," in *2009 International Conference on Computer and Electrical Engineering, ICCEE 2009*, 2009, vol. 1, pp. 545–549, doi: 10.1109/ICCEE.2009.185.

[33] K. Bergman, L. P. Carloni, A. Biberman, J. Chan, and G. Hendry, *Photonic Network-on-Chip Design*, vol. 68. Springer, 2014.