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Reconfigurable Multifunctional Ambipolar Polymer Transistors with Improved Switching-off Capability Upon Non-Uniformly Distributed Compensation Potential

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Abstract

Ambipolar field-effect transistors allowing both holes and electrons transport can work in different states, which are attractive for simplifying the device manufactures and miniaturizing the integrated circuits. However, conventional ambipolar transistors intrinsically suffer from poor switching-off capability because the gate electrode is not able to simultaneously deplete holes and electrons across the entire transport channel. Here, we show that the switching-off capability of polymer ambipolar transistor is largely improved by up to 3 orders, through introducing non-uniformly distributed compensation potentials along the channel to synchronically tune the charge transport at different channel locations. Non-uniformly gate-stressed conjugated-polymer@insulator blend film induces non-uniformly trapped charges in the insulators, which consequently generates non-uniform compensation electrical field imposed in the conjugated-polymers. Both n-type and p-type operations with high mobility (2.2 and $0.8\text{ cm}^2\text{s}^{-1}\text{V}^{-1}$ respectively) and high on/off ratio (10^5) are obtained in the same device, and the device states are reversibly switchable, which provides a new strategy for three-level non-volatile memories and artificial synapses.

Silicon based complementary metal-oxide semiconductors (CMOS) logic circuits lay the foundation of modern electronics, where both p-type (hole transport) and n-type (electron transport) unipolar transistors are obtained by precisely controlled doping of intrinsic silicon. However, the conventional doping process such as ion implantation becomes increasingly difficult as the device dimensions decrease, and building CMOS logics with discrete p- and n-doped transistors complicates the device manufacturing process and limits the miniaturization of the circuits¹⁻⁴. Meanwhile, with the booming demand of information processing capability, the traditional computing systems based on von Neumann architecture are encountering great challenges, due to the separation of computing and memory units⁴⁻⁷. Reconfigurable devices with modifiable operating states or multiple functions are quite meaningful for the miniaturization of circuits, by reducing the number of devices, promoting the integration of circuits, and endowing the circuits with versatility^{2,8-10}. In addition, neural-like electronic devices and neuromorphic computing that mimics the human brain provide an efficient information processing method^{4-6,11-16}. Nevertheless, this also places higher demands on the functions of devices and circuits^{8,17}. A single device which can emulate the synapses with the functions of both signal transmission and non-volatile memory is indispensable for neuromorphic electronics^{5,14,18}.

Ambipolar materials, such as one-dimensional semiconductors (e.g., carbon nanotube), two-dimensional semiconductors (e.g., graphene, black phosphorus and transition metal disulfides), and conjugated-polymers, in which both holes and electrons are allowed to transport¹⁹⁻²², are employed to fabricate ambipolar transistors with multiple operations to simplify the fabrication process of CMOS-like logics and miniaturize the integrated circuits²³. However, intrinsically ambipolar transistors could not be completely switched off, because during the device operations, different voltages are necessarily applied to the source and drain electrodes and thus the charge modulations (accumulation and depletion) in the different locations of the transport channel are not synchronic (Fig. 1a)^{3,24}. This condition typically leads to rather shallow V-

shaped transfer characteristics especially when the drain voltage is relatively high. The inconspicuous off-state and low on/off ratio are unfavorable for the design of CMOS-like logic circuits²⁴. Several methods aiming at either modifying the ambipolar materials or optimizing the device structures were proposed to promote the applications of ambipolar materials for high performance transistors and CMOS-like circuits, and among them are two representative examples: 1) Converting ambipolar to unipolar (p-type or n-type) during device fabrication or post-processing to improve the off-state. Particularly, contact engineering, chemical doping and modification of dielectrics are adopted to suppress the ambipolar transport²⁵⁻³¹, which sacrifice the multifunctional operation characteristics of ambipolar transistors. 2) Suppressing the injection and accumulation of electrons (holes) from the drain electrodes in p-type (n-type) working mode through modified device construction and additional control signals to gain a high on/off ratio. In this case, additional electrodes and control signals are necessary to separately control the charge accumulation or depletion in different channel locations^{2,3,28,32-35}, which complicate the fabrication process and weaken the compatibility with the conventional three terminal devices as well as their integrated circuits. Therefore, so far, the state-of-the-art approaches based on the optimizations of materials and device constructions do not reversibly and continuously tune the ambipolar performance satisfactorily especially after the complete fabrication of the device, though the tunability would be crucial for non-volatile memories and artificial synapses.

Actually, besides additional electrodes, any methods (e.g. polarized ferroelectrics and charged electrets) which can provide gradually varied compensation potential to the channel can eliminate the asymmetric potential along the channel under certain gate and drain voltages³⁶⁻³⁹. Therefore, appropriate gate voltage and external compensation potential can be designed to prevent the injection and accumulation of neither holes nor electrons to obtain an off-state with low current (Fig. 1b). In addition, with a gradually varied compensation potential, holes or electrons could be approximately synchronically and symmetrically accumulated along

the channel when the gate voltage deviates slightly from the off-state (Fig. 1b)³⁶.

Taking the above considerations into account, in this work we demonstrate an easily-accessible post treatment to reversibly manipulate the operation of ambipolar transistors upon non-uniformly gate-stressed conjugated-polymer@insulator blends. The switching-off capability is thus improved by 3 orders. The non-uniform gate stress induces non-uniform compensation potential, which effectively tunes the off-state current and consequently contributes to diverse device characteristics and multiple functions, such as ambipolar transistors with reconfigurable on/off ratio, CMOS-like inverters, multi-level non-volatile memories and artificial synapses. Insulator dominated (90%) conjugated-polymer@insulator blend films are used for both charge transport and charge trapping, where the continuous conjugated-polymer networks serve as high-quality transport pathways, and the insulator-matrix could trap holes or electrons acting as electret to provide a built-in compensation electric field to tune the device performance. Both p-type and n-type operations with high on/off ratio (10^5) under high drain voltage are realized in the same ambipolar transistor after the injection of non-uniformly distributed charges into the electrets, and the device states are reversibly switchable. The uniformly and non-uniformly trapped charges leading to different device states provide a new strategy for multi-level non-volatile memories. Three states for both p-type and n-type operation with current ratios of 10^2 , 10^3 and 10^5 to each other are obtained with the retention time exceeding 10^4 s. Furthermore, the non-uniform charge trapping in these reconfigurable ambipolar transistors is applicable for emulating the biological synapses. Both holes and electrons could serve as neurotransmitters to be reversibly injected and trapped in the electret to modulate the drain current representing the variation of post-synaptic signals^{5,14,40}. Compared with the conventional synaptic devices fabricated by unipolar materials, there is no need to prepare the off (on) state in this ambipolar synaptic transistor in advance for the subsequent excitation (inhibition) response, which is of great significance for realizing real-time adjustment of synaptic activity⁴¹.

Results

Simulated characteristics of ambipolar transistors with compensation potential. As shown in Fig. 1c, for the conventional ambipolar transistor under a high drain voltage (-60 V), either holes or electrons are accumulated along the whole channel when the gate voltage is highly negative ($V_G < -60$ V) or positive ($V_G > 0$ V), while both holes and electrons are simultaneously accumulated in the channel when the gate voltages are within the range of $-60 < V_G < 0$ V. The pinch-off region for this conventional ambipolar transistor is quite small. However, when a linearly distributed compensation potential ($V_C(x) = -60x/L$, $0 \leq x \leq L$, L is the channel length) is applied along the channel (Fig. 1d), an obviously wider pinch-off region which are nearly extended through the whole channel appeared as the gate voltage approaches to 0 V, resulting in a quite low off-state current and thus a high on/off ratio of the device. With further increasing the gradient of the compensation potential, the pinch-off region maintains large for a finite gate voltage range (Fig. 1e), which means the low off-state current can be obtained in a larger range of the operation voltages. The corresponding transfer characteristics of the ambipolar transistor with or without compensation potential are shown in Fig. 1f, and with the increase of the gradient of the compensation potential from source to drain, the off-state current can be greatly decreased. Similarly, a linearly varied positive compensation potential along the channel could help suppress the hole current to obtain a high on/off ratio under n-type operation ($V_D = 60$ V) (Supplementary Fig. 1a). As a comparison, for the ambipolar transistor with uniform compensation potentials along the channel, the transfer curves only shift to negative or positive voltages with the off-state current unchanged (Supplementary Fig. 1b, c). In this case, the charge modulations in different channel locations are still not synchronic and the uniform compensation potentials only change the gate voltages for the accumulation or depletion of the charges. However, combining the uniform and non-uniform compensation potentials could not only tune the off-state current but also regulate the value of the gate voltages to achieve the off-

state (Supplementary Fig. 1d, e), which will increase the controllability of the device operations through applying compensation potentials.

Experimentally, we use a conjugated-polymer@insulator blend film based ambipolar transistor as a prototype to demonstrate the modulation of ambipolar transistors by the non-uniform compensation potential provided by the trapped charges in the insulator electret. A small quantity of conjugated-polymers dispersed in the insulator-matrix could effectively improve the device performance (e.g. mobility and stability)⁴²⁻⁴⁶, and more importantly, the insulator-matrix could help store charges and enhance the stability of stored charges for long time retention. The stored charges in the insulator-matrix could change the local potential of the channel, which is equivalent to the compensation potential applied to the channel. The local potential generated by the stored charges in the insulator-matrix is proportional to the charge density, i.e. $V_C(x) = Q_C(x)/C_i$, where $Q_C(x)$ is the density of stored charges at position x and C_i is the capacity per unit area of the dielectric layer. The charges are pre-injected into the insulator-matrix by gate-stress, and through adjusting the gate and drain voltages, the distribution of the injected charges could be modulated to generate different compensation potential profiles along the channel to realize different final device performance. The charge trapping and de-trapping in the insulator-matrix is switchable and reversible, which enables to erase the previous state and reprogram the device for another state³⁹. Moreover, as there are traps for both holes and electrons leading to threshold voltages for the accumulation of mobile charges, the actual pinch-off region of the ambipolar transistor is wider than that shown in Fig. 1c and smaller compensation potentials could effectively lower the off-state current.

Performance of conjugated-polymer@insulator-matrix based transistors. Bottom-gate/top-contact transistors were fabricated on octadecyltrimethoxysilane (OTMS) modified SiO₂/Si substrates⁴⁷, with gold source and drain electrodes. The ambipolar conjugated-polymer poly[2,5-bis(2-decyltetradecyl)pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dione-alt-5,5'-di(thiophen-2-

yl)-2,2'-(E)-1,2-bis(3,4-difluorothien-2-yl)ethene] (PDPP-4FTVT, Fig. 2a) with nearly balanced electron and hole mobility was reported in recent years⁴⁸. Polystyrene (PS, Fig. 2a) is used as the insulator-matrix and blended with the conjugated-polymer to form the active layer in the transistors. Pure conjugated-polymers or the blends with PS were spin-coated onto the substrates from the solution in o-dichlorobenzene (o-DCB). The device fabrication and measurement were processed in a nitrogen filled glovebox. Figure 2b shows the field-effect mobility of the ambipolar transistors with various weight ratios of PDPP-4FTVT blended in PS as the active layer. The transistors with 10% PDPP-4FTVT in the blends (denoted as PDPP-4FTVT_{10%}@PS) show the highest field-effect mobility, which is also higher than that of pure PDPP-4FTVT based transistors. The representative transfer and output characteristics of PDPP-4FTVT_{10%}@PS based transistor are shown in Fig. 2c, d. The saturated field-effect hole mobility (μ_h) and electron mobility (μ_e) extracted from the linear range of $|I_D|^{0.5}$ vs V_G plots are 0.7 and 1.8 cm² s⁻¹ V⁻¹, respectively, and the current on/off ratio is 10² both for p-type (V_D = -60 V) and n-type (V_D = 60 V) operation. The transistor characteristics of pure PDPP-4FTVT and other ratios of blends are shown in Supplementary Fig. 2.

To explore what changed the device performance when blending the conjugated-polymer with PS, UV-vis spectroscopy, grazing incidence wide-angle X-ray scattering (GIWAXS) and atomic force microscope (AFM) were used to characterize the morphology and microstructure of the blend film as well as the pure conjugated-polymer film. Figure 2e shows the absorbance of PDPP-4FTVT and PDPP-4FTVT_{10%}@PS films. For PDPP-4FTVT, there are two absorption peaks at 833 and 743 nm, corresponding to the 0-0 and 0-1 vibrational transitions. For a qualitative analysis, the absorbance was normalized at the 0-1 peak. By comparison, we find that the 0-0 peak shows a higher intensity value and the peak position shifts to a larger wavelength after blending with PS. This phenomenon has been observed in several conjugated-polymer and insulator blends, which demonstrates increased aggregation and ordering of

conjugated-polymers in the insulator-matrix^{42,43,49-54}. The dashed lines in Fig. 2e are the absorbance of PDPP-4FTVT_{10%}@PS film after different time periods of oxygen plasma etching. The absorbance at 195 (A_{195}) and 836 nm (A_{836}) was mainly contributed by the absorption PS and PDPP-4FTVT respectively, which was extracted to reveal the distribution of the two components in the vertical direction of the blend film⁵⁵. As shown in Fig. 2f, A_{195} and A_{836} decayed at a similar rate and the ratio of them (A_{836}/A_{195}) slightly changed with the increase of etching time, except for the top and bottom interface, demonstrating that no obvious vertical phase separations of conjugated-polymers and insulators occurred in the blend film⁵⁵. In addition, GIWAXS, as a well-established protocol for characterizing the crystalline structure of polymers, was used to characterize the nanostructure change of the conjugate-polymer films^{56,57}. Figure 2g shows the 2D GIWAXS patterns as well as the 1D integrated curves, where strong (h00) signal was observed in the out-of-plane direction while only weak (010) signal was observed in the in-plane direction. Based on the diffraction signal, we conclude that edge-on lamellar crystal dominated in the pure PDPP-4FTVT film. By comparison, the PDPP-4FTVT_{10%}@PS film show a weaker (h00) signal than that of pure PDPP-4FTVT film. In addition, a broad halo attributing to the diffraction signal of amorphous PS was also observed in PDPP-4FTVT_{10%}@PS film (Fig. 2g). The weaker diffraction signal in the blend film indicates that the crystallinity of conjugated-polymer has decreased⁴², which can be rationalized by the fact that PS distorted the formation of the long-range ordered crystalline structure in PDPP-4FTVT. Nevertheless, the short-range intermolecular aggregation of the conjugated-polymer chains was not weakened, but increased due to the confinement effect of inert PS matrix according to the vibrational transitions peaks^{43,53,58}. AFM height images (Fig. 2h) exhibit that the surfaces of both pure and blend film were smooth, while the phase images illustrate that the fiber like morphology which attribute to the aggregation of conjugated-polymer chains was formed in the blend film, similar to the reported results of conjugated-polymer and insulator blends^{42,43,49}. Thus, according to UV-vis spectroscopy, GIWAXS and AFM results, the PDPP-

4FTVT chains which extended along the backbone direction form fiber like continuous network with enhanced local aggregation embedded in the amorphous PS matrix. This unique network of conjugated-polymer chains enables high-quality pathways for charge transport, and the insulator-matrix could trap charge acting as electret to modulate the device performance. Another conjugated-polymer P2F⁵⁹ was studied with the same methods, and the device performance as well as the morphology/microstructure varied with similar tendency to PDPP-4FTVT after blended with PS, except that the hole mobility is higher than the electron mobility for all of the transistors with different ratios of P2F in the active layers (Supplementary Fig. 3 and 4).

Modulating the operation of ambipolar transistors by non-uniformly distributed electret charges. To modulate the performance (especially the on/off ratio) of the ambipolar transistors, holes or electrons are injected into the insulator-matrix under both gate and drain voltages to induce uniformly or non-uniformly distributed electret charges along the channel, which provide the built-in compensation field to alter the channel potential. This procedure is regarded as a programming operation to the transistor with the conventional construction. Compared to other reconfigurable transistors with additional electrodes, this method avoids the complicated manufacturing process, and maintains good compatibility with traditional devices and circuits. In the programming process, the gate and drain voltages were adjusted to obtain different final performance. The charge injection procedure was processed at 130 °C to realize efficient injection. The transfer characteristics of PDPP-4FTVT_{10%}@PS and P2F_{10%}@PS transistors measured at 130 °C are shown in Supplementary Fig. 5. A large *butterfly*-shaped hysteresis appeared in the drain current profile with the scan of the gate voltages, which is a typical feature of charge trapping^{9,10,40,60}. Both positive and negative shifts of the transfer curves were observed, which means both electrons and holes could be injected and trapped in the insulators at high temperatures¹⁰. However, charge trapping under high temperature is un-abiding, because the

trapped charges will quickly release when the voltages are removed at high temperature, and the transistor performance would recover to its initial states after cooling to low temperature. To obtain stably trapped charges, the gate and drain voltages were kept as the temperature dropped from 130 °C to below 40 °C. In this case, some of the charges injected at high temperature could be stably trapped at low temperatures, which guarantees reliable electrets to modulate the transistor performance^{36,61}. We firstly investigated the device performance after introducing uniformly trapped charges along the channel, which was realized by stressing the ambipolar transistor with a high gate voltage as well as the source and drain grounded ($V_S = V_D = 0$ V). As shown in Supplementary Fig. 6, introducing uniformly trapped charges only shifted the transfer curves to positive or negative voltages, and the current on/off ratios were almost unchanged. The transfer curve shifts were originated from the trapped charges in the insulator-matrix, which modulated the accumulation and depletion of mobile charges by the electrostatic interaction^{14,55}. Stressing the transistor with positive gate voltages could inject electrons into the insulator-matrix and the trapped electrons will enhance the accumulation of holes while suppress the accumulation of electrons, which shifted the transfer curves to positive voltages. The results turned to the opposite when stressing the transistor with negative gate voltages to inject and trap holes in the insulator-matrix.

To improve the device performance with a high on/off ratio, the trapped charges should be non-uniformly distributed along the channel to generate a gradually varied compensation potential to suppress the unwanted current in the off-state. For n-type operation, holes should be injected and mainly trapped in the vicinity of drain electrodes, which suppress the injection of holes and enhance the injection and accumulation of electrons from the drain. In this case, the on-state current increases and the off-state current decreases, which leads to a remarkable increase of the on/off ratio. As shown in Fig. 3a, b, holes were injected by the bias stress of $V_G = -20$ V & $V_D = 60$ V (inset of Fig. 3a). Under such a voltage setting, the potential difference between gate and drain ($\Delta V_{GD} = -80$ V) was much larger than that between gate and source

($\Delta V_{GS} = -20$ V), and thus more holes were injected from the drain and trapped in the insulator-matrix in the vicinity of drain electrodes after cooling the device to low temperature³⁶. After such a post treatment of bias stress to the ambipolar transistor, the on-state current increased and the off-state shifted to the region of around $V_G = 0$ V with low current ($\sim 10^{-9}$ A). Thus, the current on/off ratio significantly increased from 10^2 to 10^5 . Similarly, to optimize the p-type performance of the ambipolar transistors, electrons were injected and trapped in insulator-matrix by the opposite voltage setting ($V_G = 20$ V & $V_D = -60$ V), and the current on/off ratio also increased to 10^5 (Fig. 3c). The field-effect mobility extracted from the slope of $|I_D|^{0.5}$ vs V_G plots was not notably changed before and after the programming processes for both n-type and p-type operation (Fig. 3b, d), and the obtained μ_e and μ_h are 2.2 and 0.8 $\text{cm}^2 \text{s}^{-1} \text{V}^{-1}$, respectively. The output characteristics in the scanning voltages show no ambipolar current (Supplementary Fig. 7), which is coincident with the transfer curves. Note that for brevity, Figure 3 only shows the transfer curves for the single forward scanning, and the reciprocated and repeated scanning of the transfer curves before and after programming operations are shown in Supplementary Fig. 8. The hysteresis of the transfer curves is not significant and the on/off ratio could be maintained after dozens of scanning cycles, which illustrates that the injected charges were stably trapped and could persistently modulate the device performance. The shape of the transfer curves could be further modulated through controlling the distribution of the trapped charges along the channel by changing the voltage settings in the programming process. As shown in Fig. 3e, f, stressing the ambipolar transistor by $V_G = 10$ V & $V_D = -80$, led to a wider off-state (~ 20 V) in the transfer curve, which was derived from the increased potential difference between source and drain in the bias stress, causing steeper gradient of the trapped charges along the channel. We can conclude that the more uniform the trapped charges are, the less helpful for improving the current on/off ratio (e.g. Supplementary Fig. 6), while the more dramatic increase of the trapped charges along the channel from source to drain is, the more favorable for obtaining a wide off-state with low current. In addition to the distribution gradient

of the trapped charge in the channel, the total quantity of the trapped charges also appreciably impacts the shape of transfer curves. As shown in Fig. 3g, h, the electrons were injected by $V_G = 40$ V & $V_D = -60$ V. The transfer curve shifted more to positive gate voltages while the width of off-state (~ 10 V) was not changed as compared with that in Fig. 3c. This is because the potential difference between source and drain is same with that in Fig. 3c, leading to the same gradient of trapped charges along the channel. However, the increased gate potential injected more electrons along all the channel causing the wider shift of the transfer curves to positive gate voltages. More simply, the programmed transfer curve in Fig. 3g can be regarded as that in Fig. 3c superimposing the uniformly distributed compensation potential along the channel, leading to the overall shifts of the transfer curve to positive gate voltages (Supplementary Fig. 1d, e). Therefore, through controlling the quantity and distribution of the trapped charges along the channel, the threshold voltages and the on-/off-states of the ambipolar transistors could be regulated in this work⁶².

Similar results were obtained from P2F_(10%)@PS based transistors (Supplementary Fig. 9). The transistors based on pure PDPP-4FTVT and pure P2F films show similar tendency of on/off ratio increase after non-uniform charge injection (Supplementary Fig. 10), which might be resulted from the trapped charges at the semiconductor/dielectric interface under biases⁶³. However, the quantity of the trapped charges was smaller and the charges dissipated more easily, leading to the much inferior variation range of the on/off ratio and poor retention characteristics. To demonstrate the universal applicability of this method for ambipolar transistors, p-type and n-type semiconductors stacked bi-layer ambipolar transistors were studied (Supplementary Fig. 11), in which holes and electrons accumulate/transport in different layers^{20,63}. Whether the transport channel is adjacent to or isolated from the electret layer, the non-uniformly injected charges can significantly reduce the off-state current and improve the on/off ratio. Similarly, a graded-potential gate realized by a high-resistance conductive layer within two terminal electrodes was proposed to continuously modulate the channel potential of graphene transistors,

and the electron or hole transport branch of the device could be suppressed to convert ambipolar to unipolar under an appropriate graded-potential³⁵. However, due to the zero bandgap of graphene, the on/off ratio did not increase.

It's worth noting that the opposite charge transport (holes for Fig. 3a and electrons for Fig. 3c, e and g) in the programmed transistors increased dramatically when the gate voltage deviated from the off-state. This means the ambipolarity was maintained in these devices and the intrinsic properties of the opposite charge transport (especially for mobility) were not degenerated in the programming process, which is significant to reprogram the transistor for another state and to reversibly switch the transistor operations for memories (show later). We reviewed the organic materials based ambipolar transistors reported in recent five years, and counted the average electron and hole mobility ($\mu = (\mu_p \times \mu_n)^{0.5}$) and on/off ratios for the transistors with nearly balanced electron and hole mobility ($1 < \mu_p/\mu_n < 5$ or $1 < \mu_n/\mu_p < 5$) under relatively high drain voltage (Fig. 3i and Supplementary Table 1). The on/off ratio of our reconfigurable ambipolar transistors with high mobility are tunable and the programmed high on/off ratio (10^5) is remarkable in those high mobility ($\mu \geq 1 \text{ cm}^2 \text{ s}^{-1} \text{ V}^{-1}$) transistors.

Manipulating the characteristics of single ambipolar transistor is meaningful for improving the performance of logic circuits. Building CMOS-like logics by ambipolar transistors is attractive because the complicated process of preparing p- and n-type transistors could be simplified²⁴. We demonstrate the programmed ambipolar transistors for CMOS-like inverters (Fig. 3j). The voltage transfer characteristics (Fig. 3k) and the signal gain ($dV_{\text{out}}/dV_{\text{in}}$) (Fig. 3l) were optimized when the two transistors were p- and n-programmed respectively due to the improved on/off ratio and subthreshold swing of the single transistor. However, because the opposite charge transport was not completely suppressed to converter the ambipolar transistor to typical p- or n-type unipolar transistors, the voltage transfer characteristics of the inverter were not fully swing from 0 to V_{DD} .

Uniformly and non-uniformly distributed electret charges in ambipolar transistors for multi-level non-volatile memories and artificial synapses. Injecting holes or electrons into polymer electrets to shift the transfer curves can be used to realize memory applications⁶⁴. However, for unipolar transistors, usually only one type of charges could be injected into and trapped in electret, so that the transfer curves can only be unidirectionally shifted, and cannot return to the original state even as the opposite voltage is applied^{55,65,66}. In ambipolar transistors, both holes and electrons could be reversibly trapped and released, which is favorable for reversibly switch the device states for realizing flash-type memories¹⁰. However, uniformly trapped holes or electrons along the channel just shift the transfer curves to negative or positive voltages, and the remained high off-state current lead to low memory ratios⁶⁷. We demonstrate a three-level non-volatile memory based on uniformly and non-uniformly trapped electret charges in the ambipolar transistor. As shown in Fig. 4a, for p-type operation with high drain voltage ($V_D = -60$ V), the drain current is in high level at $V_G = -5$ V due to the strong electron transport (defined as logic “0” state). Introducing uniformly trapped electrons could shift the transfer curves to positive voltages, and the minimum current state shifts to $V_G = -5$ V, which is defined as the programmed logic “1” state. The current ratio of state “0” and “1” exceeds 10^2 . Suppressing the transport of electrons by introducing non-uniformly trapped electrons in the insulator-matrix could further lower the off-state current at $V_G = -5$ V, which is defined as the programmed logic “2” state. The current ratios of state “2” to state “0” and “1” are 10^5 and 10^3 , respectively. In addition, the device could be reset to its initial state after a symmetrical negative gate stress excluding the trapped electrons in the insulator-matrix, no matter whether they were uniformly or non-uniformly trapped along the channel previously. As the ambipolar transport is maintained after the programming process, similar programming processes could be implemented to n-type operation by injecting holes into the insulator-matrix through symmetrical or asymmetrical negative bias stress (Fig. 4b), and the current ratios between state “0”, “1” and “2” are 10^2 , 10^3 and 10^5 respectively. Although holes and electrons could be

reversibly injected into and trapped in the insulator-matrix under higher temperature to let the device work in different states, the trapped holes or electrons are stable and the different memory states can be maintained for more than 10^4 s at room temperature, as shown in Fig. 4c.

Based on charge trapping in the insulator-matrix, we demonstrate the ambipolar transistors for artificial synapses with the function to process information transmission and memory simultaneously. Synapse refers to a structure in which the impulse of one neuron is transmitted to another neuron or to another cell. When the nerve impulses are transmitted to the synaptosomes through the axon, the presynaptic membrane releases neurotransmitters to the synaptic cleft, and the neurotransmitters diffuse to the post-synaptic membrane and bind to protein receptors, causing excitatory or inhibitory changes in the post-synaptic membrane (Fig. 4d)^{14,40,68}. The function of synapse could be emulated in ambipolar transistor with electret, where holes or electrons serving as the transmitters could be trapped in the electret under the gate pulse to convert the gate pulse carried signals into the change of drain current (Fig. 4d)¹⁴. In this synaptic transistor, reading the post-synaptic current at drain and applying the spike pulse at gate electrode are implemented simultaneously, which enables to concurrently perform the signal transmission and self-learning processes. As the drain voltage and gate voltage are applied simultaneously during the pulse, the charges are non-uniformly injected and trapped in the insulator-matrix. The drain current is sensitive to the non-uniformly trapped charges at $V_G = 0$ V, because which could effectively tune the off-state current as demonstrated in Fig. 3, even if the amount of injected charges at room temperature is relatively small.

Depending on whether electrons or holes are trapped in the electret, the gate pulse can induce the increase or decrease of drain current, which is in analogy with the excitatory or inhibitory post-synaptic current (EPSC, IPSC) triggered by the gate signals. As shown in Fig. 4e, at a negative drain voltage ($V_D = -30$ V), the drain current is dominated by electron transport at $V_G = 0$ V, and a pre-synaptic spike of negative pulse (-100 V) is applied to the gate electrode to trigger the EPSC. During the gate pulse, the drain current dramatically increases to a high level

and then slowly decreases. The sharp increase is derived from the sudden accumulation of holes in the transport channel when the pulse front arrives, and some of the holes are gradually injected and trapped in the electret under the negative pulse leading to the decrease. However, when the pulse ends, the current suddenly decreases but cannot return back to the initial value, because the trapped holes in the electret during the pulse increase the accumulated electrons at the pulse base ($V_G = 0$ V). As the trapped holes in the electret release rapidly once the pulse ends and then slowly decay, EPSC decays correspondingly quickly at first and slowly afterwards. The quantity of trapped holes in the electret is dependent on the pulse voltage and pulse width (T_p), while the -100 V pulse with 1 ms width is enough to inject holes into electret, resulting a significant increase of EPSC after the pulse. Similarly, positive pulses could trigger a decrease of drain current as the IPSC (Fig. 4f), by eliminating the trapped holes or injecting additional electrons into the electret. Δ EPSC and Δ IPSC are defined as the difference between the post-synaptic current before the pulse and the current peak value after the spiking pulse, which are proportional to the amount of the trapped holes in the electret. The extracted Δ EPSC and Δ IPSC as a function of the pulse width are shown in Fig. 4g, both of which change rapidly with the pulse width when the pulse width increases from 0.001 s to 0.1 s, which demonstrates the trapped charges in the electret rapidly increase or decrease with the increase of pulse width in a shorter time frame. Nevertheless, longer pulse width can no longer rapidly increase or decrease the amount of trapped charges, so the current change gradually decreases. Δ EPSC and Δ IPSC also increases with the enlargement of the pulse voltage when the pulse width remains constant (Supplementary Fig. 12a, b and c). Therefore, higher pulse voltage and longer pulse duration can result in considerable trapped charges in the electret to effectively change the post-synaptic current, and some of charges trapped in the deep energy level would maintain for longer time. As shown in Supplementary Fig. 12d, the EPSC induced by -100 V pulse for 1 s can remain potentiation for more than 10^3 s. The EPSC is fitted into a double exponential function, as it rapidly decreases at first and then slowly decay with time, which is resulted from

the rapid release of the shallowly trapped charges once the pulse end, and the deeply trapped charges slowly release from the electret. By contrast, when the transistor based on pure PDPP-4FTVT film is used for synapse, the EPSC after the same spiking pulse is much inferior, and quickly returns to the original value exhibiting poor retention characteristics (Supplementary Fig. 12e). As both holes and electrons could be injected into and trapped in the electret by the gate voltages to modulate the drain current for different levels, there is no need to prepare the off (on) state for the subsequent excitation (inhibition) response in advance. That means, for the device discussed above, electrons could be injected into and trapped in the electret to induce a decreased post-synaptic current for realizing suppression firstly (Supplementary Fig. 12f), and especially for high drain voltages, the electron current of the transistor is in high level and positive pulse spikes could effective lower it (Supplementary Fig. 12g, h).

Synaptic transmission plasticity refers to the short-term and long-term changes in synaptic transmission efficiency caused by repeated activities of pre-synaptic neurons, where the short-term plasticity (STP) is usually caused by a short string of presynaptic stimulation, with duration usually within milliseconds to minutes, including facilitation, depression, etc⁵. Paired-pulse facilitation/depression (PPF/PPD) is the change in the synaptic response induced by the pairs of double-pulse stimulation with the same stimulus intensity and the interval of milliseconds, and the measures are defined as $PPF/PPD = (A_2 - A_1)/A_1 \times 100\%$, where A_1 and A_2 are the peak values of EPSC or IPSC after the first and the second pulse, respectively. As shown in Fig. 4h, $A_2 > A_1$ and PPF decreases with the pulse interval time (Δt) increase. PPF and Δt are fitted into $PPF = C_0 + C_1 \exp(-\Delta t/t_1) + C_2 \exp(-\Delta t/t_2)$, where C_0 , C_1 , and C_2 are constants, and $t_1 = 66$ ms, $t_2 = 633$ ms are the relaxation time constants for the short-term and long-term part of the synaptic transistor, which are coincident with that of biological synapses⁴⁰. PPD is shown in Supplementary Fig. 12i, and the values are relatively small and less Δt dependent than the PPF, because the trapped holes are easily released during the first pulse. STP will transform to long-term plasticity (LTP) with permanent change in synaptic behaviors after repeated

stimulations⁵. The retention characteristics of EPSC reflect the memory effect of the synaptic transistors, including short-term memory (STM) and long-term memory (LTM)¹⁴. As shown in Fig. 4i, the EPSC after a single short pulse stimulus is much lower and quickly decays to the original state, which is analogous to the STM of brain after a transient and mild stimulation. The STM transforms to LTM when the stimulations are persistent or repeated, as the EPSC is substantially enhanced after 10 or 50 consecutive identical pulses and retains for longer time at high values. Long-term potentiation and depression (LTP, LTD) are also accomplished in the synaptic transistor, which is useful features for neuromorphic computing^{17,40,68}. Figure 4j shows the PSC of the synaptic transistor after a series of excitatory spikes and inhibitory spikes. During the excitatory spiking pulses (-100 V , $T_p = 0.1\text{ s}$ and $\Delta t = 0.1\text{ s}$), the PSC gradually increases with the pulse number increase, and then decrease under the application of inhibitory spiking pulses (60 V , $T_p = 0.1\text{ s}$ and $\Delta t = 0.1\text{ s}$). It is noted that the PSC decreases rapidly under the beginning of the inhibitory spikes, which means some of the injected holes by negative pulse are shallowly trapped and they will quickly release under the positive inhibitory spiking pulses.

Discussion

In conclusion, taking two model ambipolar polymer field-effect transistors as examples, we demonstrate modulating the on/off ratio of ambipolar transistors for multiple functions through introducing uniformly and non-uniformly distributed compensation potential along the transport channel. The compensation potential is experimentally generated by uniform or non-uniformly distributed electret charges, which are symmetrically or asymmetrically injected into the insulator electrets through adjusting the gate and drain voltages. The off-state current can be effectively decreased by up to 3 orders after injecting non-uniformly distributed charges into the electret. Both n-type and p-type operations with high on/off ratio (10^5) under high drain voltage are realized and the device states are reversibly switchable. Based on uniformly and non-uniformly distributed electret charges, three-level non-volatile memories with long-term

retention characteristics are demonstrated under both n-type and p-type operation. The non-uniform charge trapping under both gate and drain voltages is implemented to emulate synapses in the ambipolar transistors, where the gate serves as the pre-synapse, and both holes and electrons could be trapped in the electrets under the gate pulse generating a change of drain current to emulate the EPSC or IPSC. Short-term and long-term synaptic behaviors including facilitation, depression and memory are demonstrated.

Methods

Materials. PDPP-4FTVT and P2F were synthesized as the reported methods.^{48,59} PS (Mw = 2000 kDa) was purchased from Sigma-Aldrich. OTMS was purchased from Tokyo Chemical Industry.

Device Fabrication. The device fabrication was processed in a nitrogen filled glovebox. Bottom-gate/top-contact transistors were fabricated on SiO₂/Si substrate, where SiO₂ (300 nm) was used as dielectric layer and the n-type doped Si served as gate electrode. The surface of SiO₂ was modified by OTMS using the reported methods⁴⁷. PDPP-4FTVT and P2F was dissolved in o-DCB with a concentration of 2 mg/mL and spin-coated (1000 rpm) on OTMS modified SiO₂/Si substrate. PDPP-4FTVT or P2F was blend with PS with different weight ratio and dissolved in o-DCB with a total concentration of 10 mg/mL, and the spin-coated (2000 rpm) on OTMS modified SiO₂/Si substrate. All the spin-coated films were annealed at 200 °C for 10 min. Gold was used as source and drain electrodes and was deposited on the active layer with a thickness of 50 nm by thermal evaporation in a vacuum chamber ($< 10^{-4}$ Pa).

Device and Film Characterization. The absorbance of polymer films was measured using a PE Lambda 35 UV/Vis/NIR Spectrophotometer and the films were spin-coated on OTMS modified fused quartz glasses. The blend films were treated in a plasma cleaner (FEMTO) at 30 Pa to remove the materials of the film from top to bottom and the absorption spectra were

performed after oxygen plasma treatment to obtain the sublayer absorbance. The AFM images were obtained from an Asylum Research Cypher. GIWAXS measurements with synchrotron light were undertaken at the microfocus endstation of P03 beamline at PETRA III of the Deutsches Elektronen Synchrotron (DESY), Germany. The GIWAXS data were analyzed with the software of DPDAK and GIXSGUI^{56,69}. The transistor, inverter, memory and synapse characteristics were measured in a nitrogen filled glovebox using an Agilent Keysight B2902A Precision Source/Measure Unit. To modulate the on/off ratio of ambipolar transistors by post introduced uniformly or non-uniformly distributed electret charges along the channel, the programming procedures were processed as follow steps in a nitrogen filled glovebox: 1) Measuring and recording the intrinsic performance of the ambipolar transistor; 2) Heating the ambipolar transistor to 130 °C with a certain gate and drain voltages applied (e.g. $V_G = -20$ V and $V_D = 60$ V for Fig. 3a), and maintaining at 130 °C for 2 minutes. 3) Stop heating and waiting for the temperature to drop to below 40 °C with the gate and drain voltages applied. 4) Measuring and recording the final performance of the ambipolar transistor. In the programming process, the gate and drain voltages were changed to obtain different final performance. The mobility (μ_p or μ_n) was extracted from $I_D = W/2LC_i\mu(V_G - V_T)^2$, where $W = 3$ mm is the channel width, $L = 0.3$ mm is the channel length, V_T is the threshold voltage and $C_i = 11.5$ nF/cm² is the capacitance per unit area of SiO₂ (300 nm) dielectric layer.

Device Simulation. A one-dimension model was established to simulate the carrier transport in our proposed reconfigurable ambipolar transistor. The current in the transistor channel should meet

$$V_D - V_S = -I_D \int_0^L \frac{dx}{eWP(x)\mu}, \quad (1)$$

where V_S and V_D are the electric potentials applied to the source and drain electrode, I_D is the current in the channel, e is the elemental charge, x is the distance from the source, L and W are the channel length and channel width of the transistor, μ is the carrier mobility (μ_e for electrons

and μ_p for holes) and $P(x)$ is the areal carrier density (both holes and electrons for our ambipolar device) in the channel at the position x , which can be derived from the plate capacitor model as,³⁶

$$P(x) = C_i [V(x) - V_G] = -C_i \left[I_D \int_0^x \frac{dx'}{eWP(x')\mu} - V_S + V_G \right], \quad (2)$$

where $V(x)$ is the electric potential at the position x in the channel, V_G is the gate voltage and C_i is the capacity per unit area of the dielectric layer,

For our simulation, we have

$$L = 0.3 \text{ mm}, W = 3 \text{ mm}, \mu_p = 0.7 \text{ cm}^2 \text{ s}^{-1} \text{ V}^{-1}, \mu_e = 1.8 \text{ cm}^2 \text{ s}^{-1} \text{ V}^{-1}, C_i = 11.5 \text{ nF cm}^{-2}.$$

We solved equations (1) and (2) numerically to obtain the transfer characteristics of the device.

For simulating the ambipolar transistors with a compensation potential $V_C(x)$,

$$P(x) = C_i [V(x) - V_G - V_C(x)] = -C_i \left[I_D \int_0^x \frac{dx'}{eWP(x')\mu} - V_S + V_G + V_C(x) \right], \quad (3)$$

Experimentally, the compensation potential $V(x)$ was provided by the stored charges in the insulator electrets, and the local potential generated by the stored charges in insulator-matrix is proportional to the charge density, i.e. $V_C(x) = Q_C(x)/C_i$, where $Q_C(x)$ is the density of stored charges per unit area. Therefore, equation (3) is transformed to

$$P(x) = C_i [V(x) - V_G - V_C(x)] = -C_i \left[I_D \int_0^x \frac{dx'}{eWP(x')\mu} - V_S + V_G \right] - Q_C(x), \quad (4)$$

Note that to avoid the presence of $P(x) = 0$ positions along the channel which would diverge the integrand in equations (1) and (2), (3) or (4), we define a small voltage value $V_a = 0.03 \text{ V}$ such that the carrier density was set to be $C_i V_a$ when the $P(x)$ is smaller than $C_i V_a$.

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Author contributions

G. L. conceived the research. P. W. designed the experiments and wrote the manuscript. X. W. and W. Z. did the device simulation. X. L. fabricated the transistors. P. Z. carried out the GIWAXS results. Y. D. provided the materials. N. Q., S. H. and L. B. gave the experimental assistance and discussed the results. All the authors read and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information is available for this paper at

Fig. 1 Mechanism of ambipolar transistor with improved switching-off capability upon compensation potential, which could be generated by gate-stress-induced electrets. **a** Schematic working states of conventional ambipolar transistor, where the left and right part of the ambipolar semiconductor layer could not simultaneously switching-off, leading to a poor switching-off capability of the device. S, D and G represent the source, drain and gate electrodes, respectively. **b** Schematic working state of the ambipolar transistor under compensation fields (E), where the channel potential gradient could be eliminated by the compensation fields to achieve a critical state where neither holes nor electrons are accumulated across the entire semiconductor layer, and during gate scanning, approximately uniformly distributed of holes or electrons could be realized under appropriate gate voltages. **c-e** Simulated charge density (Q) distribution of ambipolar transistor without compensation field (**c**), and with compensation potential of $V_C(x) = -60x/L$ (**d**), and $V_C(x) = -80x/L$ (**e**) at position x along the channel under different gate voltages and a constant drain voltage ($V_D = -60$ V) ($0 \leq x \leq L$). **f** Simulated transfer characteristics ($V_D = -60$ V) of the ambipolar transistor under compensation fields with different potential gradient along the channel. The inset is the compensation potential applied along the channel.

Fig. 2 Transistor performance and morphology of PDPP-4FTVT and PDPP-4FTVT_{10%}@PS thin films. **a** Chemical structures of ambipolar conjugated-polymer PDPP-4FTVT and insulator polymer PS. **b** Field-effect hole and electron mobility of the ambipolar transistors based on PDPP-4FTVT and PS blends. **c** Representative transfer and **d**) output characteristics of PDPP-4FTVT_{10%}@PS transistor. **e** Absorbance of PDPP-4FTVT and PDPP-4FTVT_{10%}@PS films. The dash lines are the absorbance of PDPP-4FTVT_{10%}@PS films after different time of oxygen plasma etching. The inset is the absorbance spectra of PDPP-4FTVT and PDPP-4FTVT_{10%}@PS films normalized at the 0-1 vibrational transitions peak. **f** Plasma etching time-dependent the absorbance at 195 nm (A_{195} , mainly contributed by PS) and 836 nm (A_{836} , mainly contributed by PDPP-4FTVT), as well as the ratio (A_{836}/A_{195}), showing no obvious vertical phase separations of conjugated-polymers and insulators in the blend film. **g** Typical GIWAXS data (2D pattern and 1D radially-integrated data) of PDPP-4FTVT and PDPP-4FTVT_{10%}@PS thin films. The blue and orange curves are attributed to the PDPP-4FTVT and PDPP-4FTVT_{10%}@PS data, respectively. **h** AFM height and phase images of PDPP-4FTVT and PDPP-4FTVT_{10%}@PS thin films.

Fig. 3 Modulating the operation of PDPP-4FTVT_{10%}@PS transistors by non-uniformly distributed compensation potential. In this work, the compensation potential is experimentally generated by non-uniformly distributed electret charges which were pre-injected from source and drain electrodes. **a, b** Transfer characteristics of the transistor under n-type operation, with electret charges injected by $V_G = -20$ V & $V_D = 60$ V. **c-h** Transfer characteristics of the transistor under p-type operation, with electret charges injected by $V_G = 20$ V & $V_D = -60$ V (**c, d**), $V_G = 10$ V & $V_D = -80$ V (**e, f**), and $V_G = 40$ V & $V_D = -60$ V (**g, h**). The insets of **a, c, e** and **g** are the schematics of injecting holes or electrons into the insulator-matrix by gate and drain voltages, and the red arrows are the electric fields perpendicular to the film thickness direction. **i** Statistics of the average electron and hole mobility ($\mu = (\mu_p \times \mu_n)^{0.5}$) and on/off ratio of organic ambipolar transistors with nearly balanced electron and hole mobility ($1 \leq \mu_p/\mu_n < 5$ or $1 \leq \mu_n/\mu_p < 5$) under relatively high drain voltage reported in recent five years. **j** Schematic of CMOS-like inverter based on n-programed (n-pro) and p-programed (p-pro) ambipolar transistors. **k** Voltage transfer characteristics and **l** corresponding gain (dV_{out}/dV_{in}) of the inverter.

Fig. 4 Uniformly and non-uniformly distributed electret charges in ambipolar transistors for multi-level non-volatile memories and artificial synapses. **a** Transfer characteristics of PDPP-4FTVT_{10%}@PS transistor after 1 pro ($V_G = 80$ V & $V_D = 0$ V), 2 pro ($V_G = 20$ V & $V_D = -60$ V) and rest ($V_G = -60$ V & $V_D = 0$ V) processes. **b** Transfer characteristics of PDPP-4FTVT_{10%}@PS transistor after 1 pro ($V_G = -90$ V & $V_D = 0$ V), 2 pro ($V_G = -20$ V & $V_D = 60$ V) and reset ($V_G = 80$ V & $V_D = 0$ V) processes. **c** Retention characteristics of PDPP-4FTVT_{10%}@PS transistor before and after 1 pro ($V_G = 80$ V & $V_D = 0$ V) and 2 pro ($V_G = 20$ V & $V_D = -60$ V) processes. **d** Schematic illustration of the ambipolar transistor with trapped charges in electret for artificial synapse. **e** EPSC generated by -100 V pre-synapse pulse with variety of pulse widths for potentiation. **f** EPSC generated by 80 V pre-synapse pulse with variety of pulse widths for depression. **g** Pulse width dependent Δ EPSC and Δ IPSC, extracted from **e** and **f**. **h** PPF ($= (A_2 - A_1)/A_1$) as a function of the pulse interval time (Δt). **i** EPSC and the decay characteristics after the stimulation of 1, 10 and 50 pre-synapse gate pulse (-80 V, $T_p = 0.1$ s and $\Delta t = 0.1$ s). **j** PSC during 50 excitatory and 50 inhibitory spiking pulses for LTP and LTD. The PSC was extracted from the peak value of the post-synaptic current after each pulse.

Figures

Figure 1

Mechanism of ambipolar transistor with improved switching-off capability upon compensation potential, which could be generated by gate-stress-induced electrets. a Schematic working states of conventional ambipolar transistor, where the left and right part of the ambipolar semiconductor layer could not simultaneously switching-off, leading to a poor switching-off capability of the device. S, D and G represent the source, drain and gate electrodes, respectively. b Schematic working state of the ambipolar transistor under compensation fields (E), where the channel potential gradient could be eliminated by the compensation fields to achieve a critical state where neither holes nor electrons are accumulated across the entire semiconductor layer, and during gate scanning, approximately uniformly distributed of holes or electrons could be realized under appropriate gate voltages. c-e Simulated charge density (Q) distribution of ambipolar transistor without compensation field (c), and with compensation potential of $VC(x) = -60x/L$ (d), and $VC(x) = -80x/L$ (e) at position x along the channel under different gate voltages and a constant drain voltage ($V_D = -60$ V) ($0 \leq x \leq L$). f Simulated transfer characteristics ($V_D = -60$ V) of the ambipolar transistor under compensation fields with different potential gradient along the channel. The inset is the compensation potential applied along the channel.

Figure 3

Modulating the operation of PDPP-4FTVT10%@PS transistors by non-uniformly distributed compensation potential. In this work, the compensation potential is experimentally generated by non-uniformly distributed electret charges which were preinjected from source and drain electrodes. a, b Transfer characteristics of the transistor under n-type operation, with electret charges injected by $V_G = -20$ V & $V_D = 60$ V. c-h Transfer characteristics of the transistor under p-type operation, with electret charges injected by $V_G = 20$ V & $V_D = -60$ V (c, d), $V_G = 10$ V & $V_D = -80$ V (e, f), and $V_G = 40$ V & $V_D = -60$ V (g, h). The insets of a, c, e and g are the schematics of injecting holes or electrons into the insulator matrix by gate and drain voltages, and the red arrows are the electric fields perpendicular to the film thickness direction. i Statistics of the average electron and hole mobility ($\mu = (\mu_p \times \mu_n)^{0.5}$) and on/off ratio of organic ambipolar transistors with nearly balanced electron and hole mobility ($1 \leq \mu_p/\mu_n < 5$ or $1 \leq \mu_n/\mu_p < 5$)

under relatively high drain voltage reported in recent five years. j Schematic of CMOS-like inverter based on n-programmed (n-pro) and p-programmed (p-pro) ambipolar transistors. k Voltage transfer characteristics and l corresponding gain ($|dV_{out}/dV_{in}|$) of the inverter.

Figure 4

Uniformly and non-uniformly distributed electret charges in ambipolar transistors for multi-level non-volatile memories and artificial synapses. a Transfer characteristics of PDPP-4FTVT10%@PS transistor after 1 pro ($V_G = 80$ V & $V_D = 0$ V), 2 pro ($V_G = 20$ V & $V_D = -60$ V) and rest ($V_G = -60$ V & $V_D = 0$ V) processes. b Transfer characteristics of PDPP-4FTVT10%@PS transistor after 1 pro ($V_G = -90$ V & $V_D = 0$ V), 2 pro ($V_G = -20$ V & $V_D = 60$ V) and reset ($V_G = 80$ V & $V_D = 0$ V) processes. c Retention characteristics of PDPP-4FTVT10%@PS transistor before and after 1 pro ($V_G = 80$ V & $V_D = 0$ V) and 2 pro ($V_G = 20$ V & $V_D = -60$ V) processes. d Schematic illustration of the ambipolar transistor with trapped charges in electret for artificial synapse. e EPSC generated by -100 V pre-synapse pulse with variety of pulse widths for potentiation. f EPSC generated by 80 V pre-synapse pulse with variety of pulse widths for depression. g $\Delta EPSC$ vs Pulse Width. h PPF vs Δt . i EPSC vs Time for LTM and STM. j PSC vs Pulse Number for potentiation and depression.

g Pulse width dependent Δ EPSC and Δ IPSC, extracted from e and f. h PPF ($= (A2 - A1)/A1$) as a function of the pulse interval time (Δt). i EPSC and the decay characteristics after the stimulation of 1, 10 and 50 pre-synapse gate pulse (-80 V, $T_p = 0.1$ s and $\Delta t = 0.1$ s). j PSC during 50 excitatory and 50 inhibitory spiking pulses for LTP and LTD. The PSC was extracted from the peak value of the post-synaptic current after each pulse.

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