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Research Article

Keywords: homojunction TFETs, heterojunction TFETs, device performances, ab-initio quantum transport simulation

Posted Date: September 21st, 2021

DOI: https://doi.org/10.21203/rs.3.rs-848428/v1

Version of Record: A version of this preprint was published at Journal of Computational Electronics on March 28th, 2022. See the published version at https://doi.org/10.1007/s10825-022-01867-z.

Device Simulation of the GeSe Homojunction and vdW GeSe/GeTe Heterojunction TFETs for High-performance Application

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Abstract

Compared with a 2D homogeneous channel, the introduction of a 2D/2D homojunction or heterojunction is a promising method to promote the performance of a TFET mainly by controlling the tunneling barrier. We simulate the 10-nm-L_g double-gated GeSe homojunction TFETs and vdW GeSe/GeTe heterojunction TFETs using the *ab initio* quantum transport calculations. Two constructions are considered for both the homojunction and heterojunction TFETs by placing the BL GeSe and vdW GeSe/GeTe heterojunction as the source or drain while the channel and the remaining drain or source use ML GeSe. The on-state current (I_{on}) of the optimal *n*-type BL-ML GeSe source homojunction TFET and the optimal *p*-type vdW GeSe/GeTe drain heterojunction TFET are 2320 and 2387 μA μm^{-1}, respectively, which are 50% and 64% larger than I_{on} of the ML GeSe homogeneous TFET. Inspiringly, the device performances (I_{on}, intrinsic delay time τ, and power delay product PDP) of both the optimal *n*-type GeSe homojunction and *p*-type vdW GeSe/GeTe heterojunction TFETs meet the requirement of the International Roadmap for Device and Systems high-performance device for the year of 2034 (2020 version).

Keywords: homojunction TFETs; heterojunction TFETs; device performances; *ab-initio* quantum transport simulation

Introduction

With the continuous reduction of the device scale, it is critical to reduce the power consumption of integrated circuits, which can be achieved by lowering the power supply voltage of the basic field-effect transistor (FET) [1-4]. Compared to a conventional FET, the tunnel FET (TFET) could realize a sudden change of the switch with a sub-thermionic steep subthreshold slope (*SS*) of less than 60 mV/dec due to the avoidance of thermionic charge transport, so that a TFET is more efficient to reduce the supply voltage. However, conventional TFETs have one main bottleneck, *i.e.*, small on-state current (I_{on}), so that to obtain a high-enough I_{on} is a major challenge for TFET application. To use a two-dimensional (2D) channel instead of a three-dimensional one is a valid scheme to promote the I_{on} of a TFET [5-23] mainly due to the enhanced electrostatic control by the atomic-thin body and the reduced scattering by the free-of-dangling-bond surface. To further introduce a homojunction or heterojunction architecture [15-21] in a TFET is a convincing scheme to continuously promote the I_{on} compared to a homogenous 2D channel. Experientially, 2D TFETs have been fabricated based on transition metal chalcogenides (TMD) and black phosphorene (BP) with good I_{on} and *SS* [24-31]. Inspiringly, a much higher I_{on} is observed on BP homojunction TFETs than their homogenous counterparts from experiment [29-31] and theory [18-20]. The improved I_{on} by the homojunction arises from the narrower bandgap of a thicker-layer/bulk BP so that the tunneling barrier is narrowed.

ML GeSe is an emerging semiconductor [32] with puckered honeycomb network like BP. Different from the instability of BP, ML GeSe has good stability [33, 34], which is conducive to the realization of practical devices. In addition, the medium bandgap [34-38], anisotropic electronic properties [34, 38, 39], and high carrier mobility [38, 40, 41] of ML GeSe enable it an attractive channel for TFETs [9, 11, 22]. Also, the bandgap of 2D GeSe is layer controlled where a thicker-layer GeSe has a smaller bandgap like BP [35]. Besides a thicker layer, a smaller bandgap can also be obtained by a van der Waals (vdW) heterojunction [42]. Encouraged by the good character of 2D GeSe and the positive performances of BP homojunction TFETs, the performances of the GeSe homojunction and heterojunction TFETs are much expected, especially when compared to the requirements of the International Roadmap for Device and Systems (IRDS, 2020 version) [43].

In this work, we study the device performances of the double-gated (DG) GeSe homojunction TFETs and vdW GeSe/GeTe heterojunction TFETs with L_g =10 nm by using the *ab initio* quantum transport method. The position of the homojunction or heterojunction in a device configuration is first studied. The optimal *n*-type device is the BL-ML GeSe source homojunction TFET and the optimal *p*-type device is the vdW GeSe/GeTe drain heterojunction TFET with optimal I_{on} of 2320 and 2387 μA μm^{-1}, respectively, which are 50% and 64% larger than I_{on} of the ML GeSe TFET. Then we select the optimal devices to further study the device performance limit with V_{dd}. Inspiringly, the device performances (I_{on}, intrinsic delay time τ, and power delay product PDP) of both the optimal *n*-type GeSe homojunction and *p*-type vdW GeSe/GeTe heterojunction TFETs can meet the requirement of the IRDS [43] high-performance (HP) device for the year 2034 at V_{dd} = 0.5 V.

Models and methods

We build the ML GeSe, ML GeTe, bilayer (BL) GeSe, and vdW GeSe/GeTe structures (see Figure 1 (a-d)) and optimized them by the density functional theory (DFT) with the Quantum ATK package (2020 version) [44, 45]. The generalized gradient approximation of Perdew–Burke–Ernzerh (GGA-PBE) is used to describe the exchange and correlation potential [46]. The vdW interaction between the adjacent layers of BL GeSe and vdW GeSe/GeTe is considered with the Grimme DFT+D2 correction. We choose a norm-conserving pseudopotential of 'SG15' with 'Medium' basis set, a density mesh cutoff energy of 100 Ha, and an electron temperature of 300 K. The Monkhorst-Pack *k*-point sampling is 31 × 31 × 1 [47]. The maximum force and energy convergence criteria are 5×10^{-3} eV/Å and 10^{-5} eV, respectively.

We build the DG GeSe homojunction TFETs and vdW GeSe/GeTe heterojunction TFETs with L_g =10 nm (see Fig.2 (a) and (b)). Two constructions are considered for both the homojunction and heterojunction TFETs by placing the BL GeSe and vdW GeSe/GeTe as the source or drain while the channel and the remaining drain or source use the ML GeSe. The source and drain electrode is *p*- and *n*-doped with a concentration of 1~5×10^{13} cm^{-2}. The device performances are studied with the supply voltage (V_{dd}) of 0.3~0.65 V and the IRDS (2020 version) requirements for HP device [43] with the off-state current (I_{off}) of 0.1 μA μm^{-1} are used

as a standard.

The device performances are investigated with the density functional theory (DFT) method coupled with nonequilibrium Green's function (NEGF) using the ATK package (2020 version) [44, 45]. The device simulation *k*-point mesh for the central region is 31 × 1 × 151 which is the only different setting parameter from the above settings. The transmission coefficient $T(E)$ is acquired by averaging $T(E,k_x)$ over 61 k_x-points along the periodic direction, where $T(E,k_x)=Tr[G^r\cdot\Gamma_S(E,k_x)\cdot G^a\cdot\Gamma_D(E,k_x)]$. The current I (V_{ds}, V_g) is calculated from T (E) with the Landauer–Buttiker equation: [48]

$$I(V_{DS},V_g)=\frac{2e}{h}\int_{-\infty}^{+\infty}\{T(E,V_{DS},V_g)[f_S(E-\mu_S)-f_D(E-\mu_D)]\}dE$$

Here, $G^{r/a}$ is the retarded/advanced Green's function, $\Gamma_{S/D}(E,k_x)=i(\sum_{S/D}^{r}(E,k_x)-\sum_{S/D}^{a}(E,k_x))$ the line width function with self-energy, $f_{S/D}$ Fermi–Dirac distribution function, and μ_S/μ_D electrochemical potential of the source/drain (S/D).

Results and discussions

The relaxed puckered atomic configurations of ML GeTe, ML GeTe，BL GeSe, and vdW GeSe/GeTe heterojunction are shown in Figure 1 (a-d) with the side and top views, and the corresponding cell lengths are 4.21/4.01 Å, 4.36/4.28 Å, 4.27/3.95 Å, and 4.25/4.12 Å along the armchair (Γ-X)/zigzag (Γ-Y) directions. Figure 1 (e-h) displays the band structures, and anisotropic electronic characters are seen. The ML GeSe and BL GeSe are semiconductors with direct bandgaps of 1.13 eV and 0.99 eV, respectively, while ML GeTe is an indirect semiconductor with a bandgap of 0.78 eV. From the projected band structures, the vdW GeSe/GeTe heterojunction has a type-I band alignment with a narrower indirect bandgap of 0.39 eV which is mainly contributed by the ML GeTe component. The electron/hole effective masses are 0.15/0.16, 0.09/0.12, 0.14/0.14, and 0.10/0.09 m_0 for ML GeSe, ML GeTe, BL GeSe, and vdW GeSe/GeTe heterojunction along the zigzag direction, respectively, which are smaller than those of 0.23/0.30, 0.24/0.21, 0.23/0.25, and 0.34/0.56 m_0 along the armchair direction.

The cell lengths, bandgaps, and effective masses are well consistent with previous works [11, 33, 35, 38]，see Table 1.

We first make clear whether the position of the homojunction or heterojunction, *i.e.* role as the source or drain, could impact the device performance. The transfer characteristics of the 10-nm-L_g GeSe homojunction TFET and vdW GeSe/GeTe heterojunction TFET are given in Figure 2. The I_{on} values are extracted from the transfer characteristics at the point $V_{gon} = V_{goff} + V_{dd}$ for an *n*-type device and $V_{gon} = V_{goff} - V_{dd}$ for a *p*-type device, and benchmark of I_{on} with the ML GeSe (this work), ML GeTe [11] , ML SnS [9], ML SnSe [9] , ML GeS [9], ML WTe_2 [9], ML Arsenene [10], ML Antimonene [10], ML Bismuthene [10], ML BP [9], vertical BP [8] TFETs and the IRDS HP devices for the year 2022 (2020 version) are given in Table 2. The GeSe homojunction TFET has a higher I_{on} when the BL GeSe is used as the source, while it's the opposite case for the vdW GeSe/GeTe heterojunction TFET where a higher I_{on} is obtained when the heterojunction is used as the drain. Also, I_{on} of the *n*- and *p*-type devices show a discrepancy, and the highest I_{on} of the *n*- and *p*-type devices are 2320 and 2387 μA μm^{-1} acquired in the BL-ML GeSe source homojunction TFET and the vdW GeSe/GeTe drain heterojunction TFET, respectively, which are 50% and 64% higher than I_{on} of 1548 and 1458 μA μm^{-1} of the ML GeSe TFET (this work) due to the narrower tunneling barrier arises from the homojunction and heterojunction, and outperform I_{on} of the most reported 2D TFETs [8-11] (101~1667 μA μm^{-1}) except for the ML GeTe [11] (2342 μA μm^{-1}) and ML BP [7] (2422 μA μm^{-1}) TFETs and the IRDS HP device (912 μA μm^{-1}) for the year 2022. The *n*-type branch of the BL source homojunction TFET and the *p*-type branch of the vdW GeSe/GeTe drain heterojunction TFET are selected as the optimal devices.

To give an intuitional view to interpret the improved I_{on} and the discrepancy of *n*- and *p*-type branch for the optimal devices, we give the on-state local device density of states (LDDOS) and spectral currents of the *n*- and *p*-type BL-ML GeSe source homojunction TFET and the vdW GeSe/GeTe drain heterojunction TFET in Fig. 3. For the GeSe homojunction TFET, the narrowest transport tunneling barrier (indicate with short yellow dash lines in Fig. 3) comes from the BL-ML homojunction for the *n*-type branch, which is obviously narrower compared with that of the *p*-type branch which comes from the homogenous ML-ML junction. A similar

phenomenon is seen for the vdW GeSe/GeTe heterojunction TFET, where a narrower transport tunneling barrier comes from the vdW GeSe/GeTe-ML GeSe heterojunction is seen for the *p*-type branch. Thereupon, a higher visible peak in the spectral current is seen in the *n*-type GeSe homojunction and the *p*-type vdW GeSe/GeTe heterojunction, which explains the higher I_{on}. The narrower tunneling barrier arises from the smaller bandgap of the BL GeSe source and the vdW GeSe/GeTe drain than the ML GeSe source or drain.

The electrostatic gate control ability is studied with the subthreshold swing (*SS*) and transconductance (g_m). The *SS* is defined as the linear relationship of V_g to lg I_d in the subthreshold region, $SS = \frac{\partial V_g}{\partial \lg I_d}$, while the g_m is the linear relationship of I_d to V_g, $g_m = \frac{dI_d}{dV_g}$.

The *SS* of the *n*-type BL-ML GeSe source homojunction TFETs and the *p*-type vdW GeSe/GeTe drain heterojunction TFETs are 60 and 58 mV dec^{-1}, respectively, which is smaller than the *SS* values of the ML GeTe [11], ML SnSe [9], and ML Bismuthene [10] TFETs and the required 82 mV/dec of the IRDS [43] HP devices for the year 2022 and break/equal the thermal limit of 60 mV/dec of the conventional FETs (see Table 2). Compared to the ML GeSe TFET (this work) with *SS* of 51~59 mV/dec, the *SS* of the homojunction and heterojunction devices become slightly worse, implying a tiny decline of gate control in the subthreshold area. The g_m values are 8.73 and 8.64 mS μm^{-1} for the optimal *n*- and *p*-type homojunction and heterojunction devices, respectively, which are much higher than the g_m of 5.38~5.46 mS μm^{-1} of the ML GeSe TFET (this work), implying a much better gate control in the superthreshold area. In combination with the LDDOS, we conclude that the obvious improved I_{on} arises from the enhanced gate control ability in the superthreshold region because that the narrowed tunneling barrier from the BL GeSe source and vdW GeSe/GeTe drain plays a dominant role.

The device dynamic performance metrics, *i.e.*, intrinsic delay time $\tau = \frac{C_g \cdot V_{dd}}{I_{on}}$ and power delay product $PDP = C_g \cdot V_{dd}^2$, are another two important parameters of transistors. τ represents the switching speed and PDP represents the energy consumption. In the formula, $C_g = \frac{O_{on} - Q_{off}}{W \cdot V_{dd}}$ is the intrinsic gate capacitance, not include the parasitic capacitances, where $Q_{on/off}$ is the channel charge for the on/off state and W is the periodic device width. All values of the C_g, τ,

and PDP are 0.086~0.100 fF μm^{-1}, 0.029~0.058 ps, and 0.042~0.055 fJ μm^{-1}, respectively, which are quite smaller than the values of 0. 394 fF μm^{-1}, 0.32 ps, and 0.216 fJ μm^{-1} of the IRDS [43] HP devices for the year 2022 (see Table 2). The τ values of the optimal *n*- and *p*-type devices are 0.029 and 0.031 ps, respectively, which are much smaller than the most reported 2D TFETs [9-11] (0.037~0.17 ps) expect for the ML Bismuthene [10] (0.005 ps), ML BP [7] (0.025 ps), and vertical BP [8] (0.029 ps) TFET, indicating a super-good behavior of the homojunction and heterojunction TFETs in switching speed. The PDP values of optimal *n*- and *p*-type devices are 0.049 and 0.055 fJ μm^{-1}, respectively, which outperform those of the ML Antimonene [10], ML Arsenene [10], and ML WTe_2 [9] TFETs (0.103~0.17 fJ μm^{-1}), and comparable to the other report 2D TFETs (0.027~0.054 fJ μm^{-1}) [7-11], indicating a good behavior of the homojunction and heterojunction TFETs in energy consumption.

We then study the performances of the optimal *n*-type GeSe homojunction TFET and optimal *p*-type vdW GeSe/GeTe heterojunction TFET under a lower V_{dd} of 0.3~0.65 V, and the transfer characteristics are given in the bottom right panel in Figure 2 (a) and (b), respectively. We benchmark I_{on}, τ, and PDP of the optimal homojunction and heterojunction devices against the ML GeSe TFETs [11] and the IRDS [43] HP devices (2020 version) in Fig. 4 and Table 3. The decreasing I_{on}, growing τ, and decreasing PDP with V_d indicate the descend of switching speed and energy consumption simultaneously. Compared to the ML GeSe TFETs [11], I_{on} of the GeSe homojunction TFETs and the vdW GeSe/GeTe heterojunction TFETs have improved for all V_{dd}, yet the improved extent descends with the decreasing V_{dd}. At V_{dd} = 0.5/0.65 V, the I_{on} values of the homojunction and heterojunction TFETs are 852/1709 and 893/1553 μA μm^{-1}, respectively, which are higher than those of 924 and 760 μA μm^{-1} of the IRDS HP devices for the year 2028 and 2034, respectively. When the V_{dd} continues to decrease to 0.3/0.4 V, the I_{on} values of the homojunction and heterojunction TFETs are 171/446 μA μm^{-1} and 199/472 μA μm^{-1}, respectively, which reach 22%/59% and 26%/62% targets of the IRDS HP devices for the year 2034. The τ values of the GeSe homojunction TFETs and the vdW GeSe/GeTe heterojunction TFETs are 0.027~0.127 ps and 0.034~0.130 ps, respectively, while the PDP values are 0.007~0.031 fJ μm^{-1} and 0.008~0.034 fJ μm^{-1}, respectively, which all meet the targets of 0.268 ps and 0.112 fJ μm^{-1} of the IRDS HP devices for the year 2034.

The *SS* of the GeSe homojunction TFETs and the vdW GeSe/GeTe heterojunction TFETs are 55~56 and 49 ~ 54 mV/dec at V_{dd} = 0.3~0.65 V, respectively, which are smaller than the required 75 and 70 mV/dec of the IRDS HP devices for the year 2028 and 2034 and all break the thermal limit of 60 mV/dec of the conventional FETs, but larger than those of 38~45 mV/dec of the ML GeSe TFETs [11] (see Table 3), implying a decline of gate control in the subthreshold region. The g_m of the GeSe homojunction TFETs and the vdW GeSe/GeTe heterojunction TFETs are 1.29~6.83 and 1.45~5.58 mS μm^{-1}, larger than those of 1.27~3.99 mS μm^{-1} of the ML GeSe TFETs [11], implying an enhancement of gate control in the superthreshold area.

Conclusions

The device performances of the 10-nm-L_g DG GeSe homojunction TFETs and vdW GeSe/GeTe heterojunction TFETs are investigated using the *ab initio* quantum transport method. The I_{on} of the *n*-type BL-ML GeSe source homojunction TFET and the *p*-type vdW GeSe/GeTe drain heterojunction TFET are 2320 and 2387 $\mu A\ \mu m^{-1}$, respectively, which are 50% and 64% larger than I_{on} of the ML GeSe TFET, showing the advantage of imposing homojunction or heterojunction in a TFET configuration. Inspiringly, both the optimal *n*-type GeSe homojunction and *p*-type vdW GeSe/GeTe heterojunction TFETs meet the requirement of the IRDS [43] HP device for the year 2034 (2020 version) at a low V_{dd} of 0.5 V. We expect that the excellent performance of the GeSe homojunction and GeSe/GeTe heterojunction TFET could accelerate future relevant experimental study.

Conflicts of interest

There are no conflicts to declare.

Acknowledgment

This work was supported by the Beijing Natural Science Foundation of China (No. 4212046), the National Natural Science Foundation of China (Nos. 11704008 and 91964101), the Support Plan of Yuyou Youth, and the fund of high-level characteristic research direction from North China University of Technology.

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Table 1. The relaxed cell lengths a/b, bandgaps E_g, and effective masses m_e^a, m_h^a, m_e^z, and m_h^z of the ML GeSe, ML GeTe, BL GeSe, and vdW GeSe/GeTe heterojunction compared with former works [11, 33, 35, 38].

	a (Å)	b (Å)	E_g (eV)	m_e^a (m_0)	m_h^a (m_0)	m_e^z (m_0)	m_h^z (m_0)
ML GeSe	4.21	4.01	1.13	0.23	0.30	0.15	0.16
Ref. [11]	4.27	3.99	1.18	0.22	0.29	0.13	0.14
Ref.[33]	4.26	3.99	1.11	0.23	0.33	0.14	0.16
ML GeTe	4.36	4.28	0.78	0.24	0.21	0.09	0.12
Ref.[11]	4.37	4.28	0.80	0.23	0.17	0.10	0.12
Ref.[38]	4.40	4.24	0.88	0.28	0.23	0.07	0.1
BL GeSe	4.27	3.95	0.99	0.23	0.25	0.14	0.14
Ref.[35]	4.32	3.98	1.02	—	—	—	—
GeSe/GeTe	4.25	4.12	0.39	0.34	0.56	0.10	0.09

Table 2. The device performances of the BL-ML GeSe homojunction TFETs and vdW GeSe/GeTe heterojunction TFETs for HP application (V_{dd} = 0.74 V) compared with the ML GeSe (this work), ML GeTe[11] , ML SnS[9], ML SnSe[9], ML GeS[9], ML WTe_2 [9], ML Arsenene[10], ML Antimonene[10], ML Bismuthene[10] , ML BP[7] , Vertical BP[8] TFETs and the IRDS[43] HP devices for the year 2022 (2020 version). We take L_g = 10 nm, which is smaller than the IRDS required L_g of 16 nm. Here, I_{on}: on-state current; *SS*: subthreshold swing; g_m: transconductance; C_g: total channel capacitance, not include the parasitic capacitances; τ: intrinsic delay time; PDP: power delay product.

	Type	I_{on} ($\mu A\ \mu m^{-1}$)	*SS* ($mV\ dec^{-1}$)	g_m ($mS\ \mu m^{-1}$)	C_g ($fF\ \mu m^{-1}$)	τ (ps)	PDP ($fJ\ \mu m^{-1}$)
BL-ML GeSe source homojunction	*p*	1970	57.9	6.85	0.091	0.034	0.050
	n	2320	60.0	8.73	0.089	0.029	0.049
BL-ML GeSe drain homojunction	*p*	1934	53.1	7.67	0.088	0.034	0.048
	n	1959	73.5	6.22	0.077	0.029	0.042
GeSe/GeTe source heterojunction	*p*	1807	65.9	6.68	0.086	0.035	0.047
	n	1047	68.9	5.26	0.082	0.058	0.045
GeSe/GeTe drain heterojunction	*p*	2387	57.9	8.64	0.100	0.031	0.055
	n	1850	69.6	6.49	0.088	0.035	0.048
ML GeSe (this work)	*p*	1458	50.6	5.38	0.099	0.050	0.054
	n	1548	58.8	5.46	0.095	0.045	0.052
ML GeTe [11]	—	2342	70	—	—	0.037	0.041
ML SnS [9]	—	359	37	0.80	—	0.14	0.039
ML SnSe [9]	—	1667	65	4.39	—	0.042	0.052
ML WTe_2 [9]	—	240	39	—	0.052	0.159	0.133
ML GeS [9]	—	297	30	0.57	—	0.17	0.037
ML Arsenene [10]	—	101	55	—	0.026	0.11	0.17
ML Antimonene [10]	—	173	50	—	0.01	0.067	0.103
ML Bismuthene [10]	—	1153	96	—	0.008	0.005	0.032
ML BP [7]	—	2422	58	—	0.081	0.025	0.05
Vertical BP [8]	—	1500	39	4.30	—	0.029	0.027
IRDS HP 2022 [43]	—	912	82	—	0.394	0.328	0.216

Table 3. The device performances of the optimal *n*-type GeSe homojunction TFETs and optimal *p*-type vdW GeSe/GeTe heterojunction TFETs for HP application compared with the ML GeSe TFET [11] and the IRDS[43] requirements (2020 edition) for HP applications. Here, V_{dd}: supply voltage; I_{off} = 0.1 μA μm^{-1}; I_{on}: on-state current; *SS*: subthreshold swing; g_m: transconductance; C_g: total channel capacitance, not include the parasitic capacitances; τ: intrinsic delay time; and PDP: power delay product.

	V_{dd} (V)	I_{off} (μA μm^{-1})	I_{on} (μA μm^{-1})	*SS* (mV dec^{-1})	g_m (mS μm^{-1})	C_g (fF μm^{-1})	τ (ps)	PDP (fJ μm^{-1})
GeSe homojunction	0.65	0.1	1709	56.0	6.83	0.072	0.027	0.031
GeSe/GeTe heterojunction	0.65	0.1	1553	48.5	5.58	0.081	0.034	0.034
ML GeSe [11]	0.65	0.1	1200	38	3.99	0.044	0.024	0.019
ITRS HP 2028 [43]	0.65	0.1	924	75	—	0.37	0.260	0.156
GeSe homojunction	0.50	0.1	852	55.3	3.34	0.074	0.043	0.019
GeSe/GeTe heterojunction	0.50	0.1	893	52.7	3.43	0.105	0.059	0.026
ML GeSe [11]	0.50	0.1	624	45.4	3.12	0.047	0.037	0.012
IRDS HP 2034 [43]	0.55	0.1	760	70	—	0.37	0.268	0.112
GeSe homojunction	0.40	0.1	446	54.9	2.61	0.070	0.063	0.011
GeSe/GeTe heterojunction	0.40	0.1	472	53.5	2.67	0.083	0.071	0.013
ML GeSe [11]	0.40	0.1	351	43.3	2.20	0.052	0.059	0.008
GeSe homojunction	0.30	0.1	171	54.4	1.29	0.072	0.127	0.007
GeSe/GeTe heterojunction	0.30	0.1	199	51.8	1.45	0.087	0.130	0.008
ML GeSe [11]	0.30	0.1	146	40.9	1.27	0.053	0.107	0.005

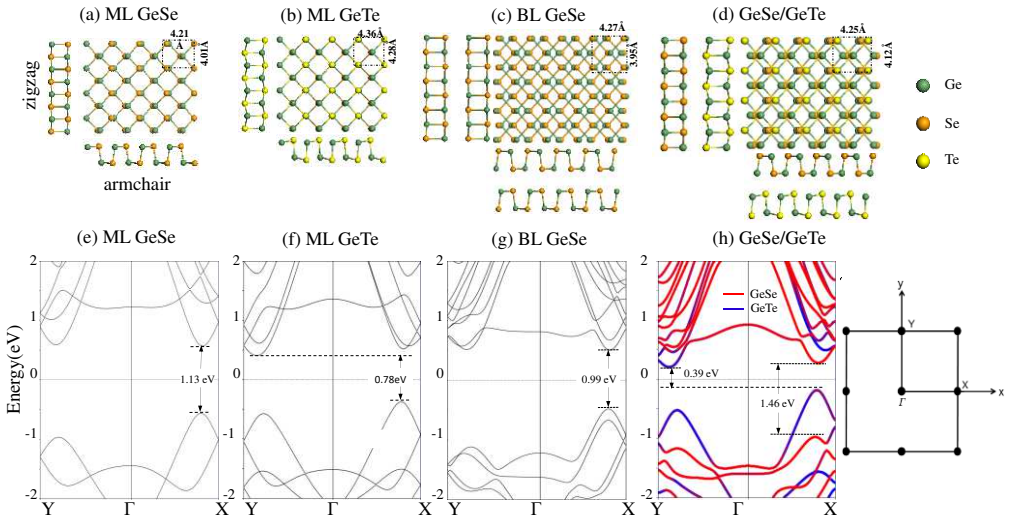

Figure 1. (a-d) The geometry and (e-h) band structures of the ML GeSe, ML GeTe, BL GeSe, and vdW GeSe/GeTe heterojunction. Green ball: Ge atom; Gold ball: Se atom; Yellow ball: Te atom.

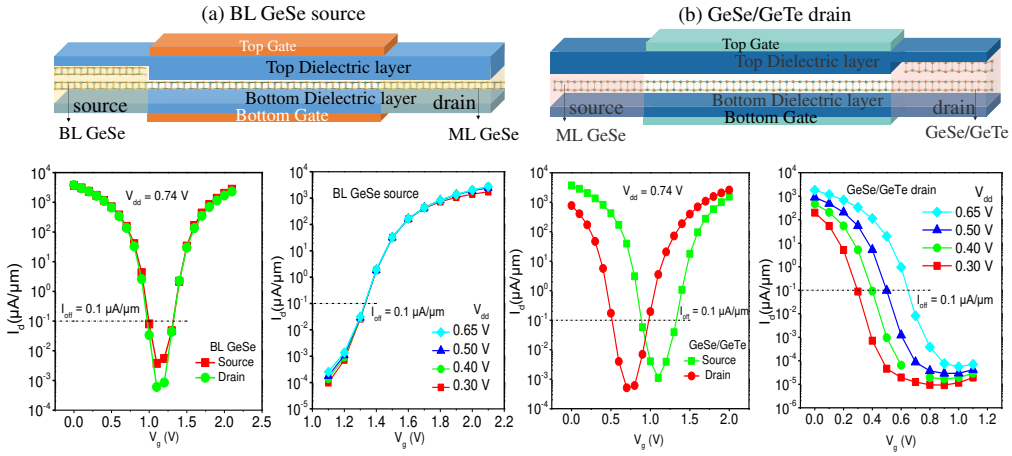

Figure 2. Device models and transfer characteristics of (a) the 10-nm-L_g BL-ML GeSe homojunction TFET and (b) vdW GeSe/GeTe heterojunction TFETs at V_{dd} of 0.3~0.74 V.

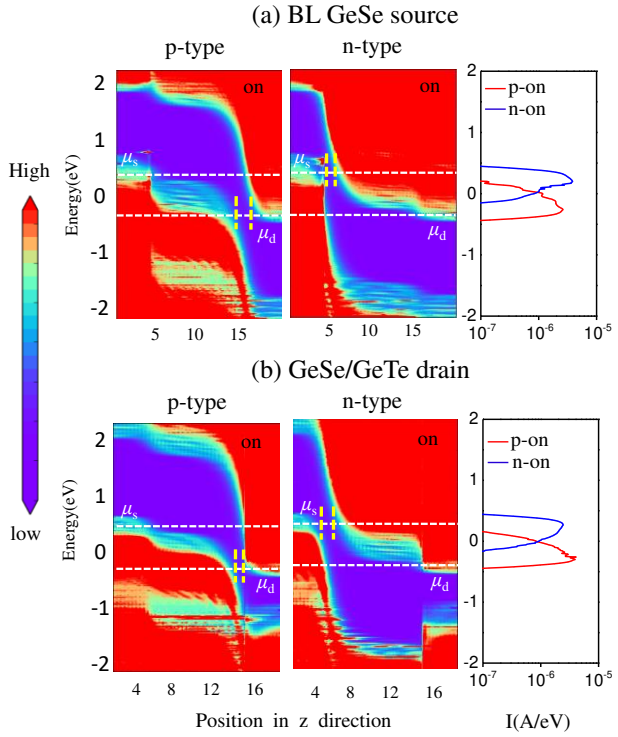

Figure 3. The on-state local device density of states (LDDOS) and spectral currents of the *n*- and *p*-type branch of the (a) BL-ML GeSe source homojunction TFET and (b) vdW GeSe/GeTe drain heterojunction TFET for HP application. Here, L_g = 10 nm, N_S/N_D = 5/5×10^{13} cm^{-2}, and V_{dd} = 0.74 V. The short yellow dash lines indicate the narrowest tunneling barrier for the on-states.

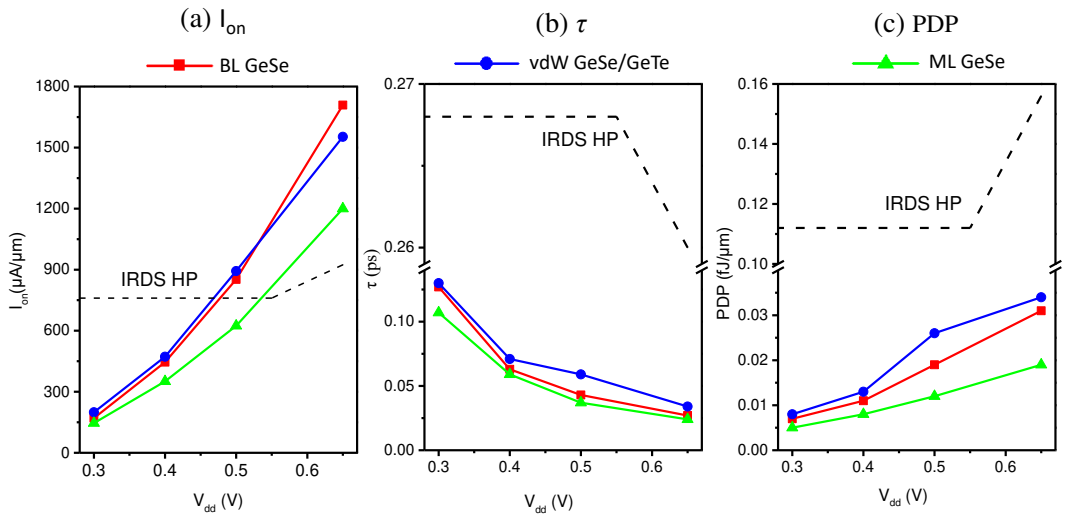

Figure 4. (a) I_{on}, (b) τ, and (c) PDP of the optimal *n*-type GeSe homojunction TFETs and optimal *p*-type vdW GeSe/GeTe heterojunction TFETs. The IRDS [43] requirements (2020 edition) for HP applications and those of the ML GeSe TFETs [11] are given for comparison.

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