Design and Analysis of CNTFET based VLSI Interconnects by Using PVT Variation

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Design and Analysis of CNTFET based VLSI Interconnects by Using PVT Variation

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Abstract: -With the quick progress in the area of digital electronics results in miniaturization of semiconductor Industries. In Deep Sub Micron regime, because of leakage current, power consumption is turn out to be a major issue; hence constant efforts are being made by the researchers for investigating the various ways to minimize this. There are various methods available for the same and out of several available methods use of Carbon Nano-tube technology is a promising way to design low power circuits efficiently. Here new techniques are introduced for the reduction of leakage power. Here in this work, comparison of the main performance parameters of Copper on chip nano-interconnect with CNTFET has been done. We have measured the impact of I_{ON} and I_{OFF} current by applying Process variation in CU and CNT- Interconnects with the variation of Tubes at 32nm technology and analysed the performance of the digital circuits with scaling of technology. The different kind of simulation outcomes indicates that by applying 10% of deviation from normal value in different device characteristics parameters such as Length of Gate (L_{Tube}) of the Tube, Width (W_{Tube}) of the Tube, Threshold Voltage (V_{th}) of the Tube, Thickness (t_{ot}) of Tube and Source & Drain Doping concentration with Cu and CNTFET interconnects for NFET and PFET with the variation of tubes from 1 to 16. All the experimental outcomes are achieved by using HSPICE simulator using SPICE model of CU and CNT at 27°C temperature by using 32nm Berkley Predictive Technology module.

Keywords: - I_{ON} and I_{OFF} , CNTFET, Mean, Standard Deviation, power consumption.

1. Introduction

In the past near about 40-45 years back, the fastest chips were able to accommodate less than 10000 transistors only. Example includes MOTOROLA 6800 microprocessor series developed in the middle of 1970 in which the transistor size was near about 6.0 micrometer. With the continuous scaling of the feature size in present era chips known as Very Large Scale Integration (VLSI), we can integrate more than 10 billion of transistors on a single chip

and we are able to achieve feature size less than 15 nm. Power consumption, Area requirement, leakage current and time to the market are some of the issues with the VLSI circuits and people are continuously trying to optimize these parameters through the various technological developments from time to time. As per the prophecy made by the Gordon Moore in the year 1965, number of devices or components on a single silicon chip turn out to be doubles in approximately 18-24 months from the present time [1,4].

Carbon Nano tube (CNT) is having excellent electrical and mechanical properties due to its exceptional band structure. Because of exhibition of its remarkable properties, CNT is popularly used as a major Interconnect material in the present day VLSI circuits. CNT are broadly classified as single-walled (SWCNT) or multi-walled (MWCNT). For single-walled (SWCNT) the devices dimensions are less than 1 nm and MWCNT are prepared by connecting various tubes of CNT in which the device dimension greater than 100 nm are attainable [5,6]. The 3-D structure of CNTFET is shown in Fig.1.

Fig.1. 3D Structure of CNTFET

In this Manuscript we have measured various performance improvement parameters by using Cu and CNTFET interconnect technology, while applying process variation over device dimension of CNTFET technology is considered. The remaining paper is structured as follows. CNTFET structure is study in section II. In Section III RLC interconnects is studied. Section IV describes the PVT variation by using Cu and CNTFET based interconnects. Section V deals with the results and discussion, in this section Average power, Delay, PDP and EDP and PVT variation in L_{Tube} , W_{Tube} , H_{Tube} , T_{Tube} etc. is calculated by using Cu and CNTFET interconnects. Lastly, we have presented conclusion in Section VI.

II. CNTFET

Carbon nanotube (CNT) is formed with the help of Hexagonal arrangement of carbon atoms to form benzene ring. The arrangement of benzene to form a graphene sheet and by rolling this graphene sheet CNT is formed. If the diameter is lesser than 1nm it is called single-walled (SWCNT), If multiple tubes or bundles of tubes are arranged with single source and drain terminal is called multi-walled (MWCNT). The outstanding electrical, Mechanical & structural properties of CNTFET technology make one of the most reliable VLSI Interconnect material in current scenario.

The parameters of CNT are understood with the crystal structure of CNTs as shown in the Fig. 2. The carbon atom is packed into honeycomb lattice structure, where C represents the circumference vector, which indicates the rolling direction of graphene sheet. The c vector is represented as $c=ma_1+na_2$ where a_1 and a_2 is the lattice vector of the grapheme sheet and chirality vector is indicated with m & n. The rolling direction of graphene sheet it is indicated with Chirality vector. We can classify the CNT on the basis of charity vector (m,n) are are armchair and Zig Zag structure as shown in the Fig.3. If the difference between m and n is 3X that is $m-n=3X$ where X is integer, if m and n are equa i.e. $m= n$ l chirlity vector is called armchair and & m and n are ($m=0$ or $n=0$) it is called zigzag approach; metallic properties are always shown in armchair approach and in Zig-Zag approach shows either metallic or semiconductor approach. With the help of chirlity vector we can measure the diameter of CNT which can be represented by equation

$$D_{CNT} = a \sqrt{\frac{m^2+n^2+mn}{\pi}} \quad (1)$$

And width of the CNTFET gate (W_{gate}) is calculated by equation (2)

$$W_{gate} \approx \text{Max}(W_{min}, N \times \text{Pitch}) \quad (2)$$

Where *Pitch* is the distance between Centres of two neighbouring SWCNT under same gate, W_{min} is minimum gate width and N is the no. of nanotube as shown in Fig.3.

Fig.2: Top View of CNTFET

Fig.3: Chirality Vector of Graphin Sheet

The layout of CNTFET is approximately same as traditional MOSFET of layout except that the channel between source and drain region are replaced by carbon nanotube. The source and drain region are heavily doped region in CNTFET transistor for faster operation of device. The intrinsic CNT are formed the channel by enclosing with planer metal gate by high- k dielectric like zirconium oxide (ZrO_2) and hafnium oxide (HfO_2) that's the gate oxide [12]. Then substrate is fully covered by insulating thick SiO_2 layer. A Multiple CNTFET channel is formed by inserting large No of nanotube aligned parallel with width of gate. The distance between centres of adjacent nanotube is called the pitch. In simulation work source and drain of CNT are doped with 0.8% doping level, HfO_2 used as gate dielectric thickness with 3nm and bulk dielectric SiO_2 thickness with $10\mu\text{m}$ [10-12]. CNT has a property that its energy gap (E_g) is inversely proportional to its diameter which allows to alter its band-gap by varying the diameter of CNTs. The threshold voltage (V_{TH}) of the CNT-FET can be approximated as half of the CNT band-gap [13, 14] as

$$V_{TH} = \frac{E_g}{2q} = \frac{1}{2\sqrt{3}} \frac{aV_\pi}{qD_{CNT}} \quad (3)$$

Where $V_\pi = 3.033 \text{ eV}$ the carbon-carbon bond energy and q is the electronic charge and by substituting these constant values, the equations can be simplified into

$$E_g = \frac{0.872}{D_{CNT}} \quad \text{and} \quad V_{TH} = \frac{0.436}{D_{CNT}} \quad (4)$$

From equation 4 energy gap (E_g) is measured with the help of diameter D_{CNT} of the tube and D_{CNT} of the tube depends upon the relative vector (m, n). Now we roll the graphene sheet if

there is change in the diameter of the tube the conductivity of the tube changes, the diameter of the tube is varies from 5 nm to 20 nm. All electrical mechanical and thermal properties of CNTFET technology depends upon diameter and chirality vector so conductivity of single walled CNT and multi-wall CNT depends upon the D_{CNT} , if we increase the diameter there is a reduction in the threshold voltage V_{th} of CNT, which results in increase of I_{ON} current because electrostatic screening effect sub-band of the channel appears closer and more number of sub-band shift towards Fermi energy level. If the pitch and diameter of CNTFET is optimized which results in increase the current of the tubes with higher aspect ratio and superconductivity of CNT with higher C-C bond [12, 15].

The main properties of CNTFET are:-

Due to arrangement of carbon atom in CNT technology it exhibits unique properties like electrical mechanical and thermal etc.

Electrical Characteristics: - It exhibits higher electrical conductivity due to chirality vector arrangement both in metallic or semiconductor properties.

Strength and Elasticity:- Carbon atom form a sheet of graphene which is chemically having strong bonding with neighboring atoms. The elastic model of CNT is higher when press the tip of CNT tube it bands and return to its original place when force is realized.

Thermal Conductivity:- CNTFET has higher conductivity due to bonding of carbon-carbon atom which provides higher strength and stiffness against strains. Due to higher thermal conductivity it is having higher potential in nano-scale molecular electronic and sensing devices. CNT is most promising material for choice today because of its properties of material like light weight, flexibility super electrical properties and its mechanical strength.

Table.I. List of chirality used in the circuits, their diameter and threshold voltage

Chirality	Diameter	V_{TH} (V)	E_g (eV)
(4,0)	0.313	1.392	0.626
(7,0)	0.548	0.795	1.096
(10,0)	0.783	0.556	1.566
(13,0)	1.018	0.428	2.036
(16,0)	1.251	0.348	2.502
(19,0)	1.486	0.293	2.972
(22,0)	1.720	0.253	3.440
(25,0)	1.955	0.223	3.910

III. Interconnects

The term interconnects is the combination of linear and non-linear elements like RLC as shown in Fig.4. For critical design process interconnects modelling is necessary aspects, there are many papers which have been published by using Cu interconnects as shown in Fig.5, here we are going to replace it with CNTFET based interconnects which has a huge potential in term of performance parameters [14,16].

Fig.4. RLC Interconnects

Fig.5. SWCNT 3D Structure

From Fig.6 the 3D view of copper interconnects have length, width and thickness t , for the measurement of two centre of Cu interconnect from central line to ground shield is d_{sg} and d_{gg} CNT. The RLC Interconnects is inserted between the buffer elements so the circuit can be lumped by RL network and value of C is measured as shown in Fig.7 [17].

Fig.6. 3D Structure of Cu Interconnects

Fig.7. Optimized RLC interconnect using buffer

Table.II Process Parameters of CNTFET Technology [13]

Parameters	Descriptions	Values
L_{ch}	Channel Length of CNT	32nm
L_{ss}	Length of source side doping in extension region	32nm
L_{dd}	Length of drain side doping in extension region	32nm
L_I	Interconnect Length	800-2000 (μm)
Pitch	Distance between CNT Tubes	15nm
T_{ox}	Thickness of gate dielectric	4nm
$(n_1 \ \& \ n_2)$	Chirality Vector	(4,0) to (25,0)
E_{fo}	Fermi level	0.6 eV
K_{ox}	Dielectric constant	16nm

Fig.8. DC Characteristics of MOS and CNTFET interconnects

Fig.9. Resistance of Cu and CNTFET Interconnects

IV. Process Variability of FinFET Devices

In this proposed research work we have simulated the geometric variation in Tube's Length (L_{Tube}), Width of the Tube (W_{Tube}), Height of the Tube (H_{Tube}), Thickness of the Tube (T_{Tube}), Source/Drain Doping (N) and evaluated variation of fin for calculation of mean and standard deviation of I_{ON} and I_{OFF} current by using CNTFET at 32nm technology [4].

PTM-MG model is developed by BSIM-CMG, for scaling multigated devices. Monte Carlo simulation is done for checking the variability of the device for ten thousand samples for each parameter. From the simulation results I_{ON} and I_{OFF} currents were calculated for 3σ deviation of 10% from the standard values for different parameters like L_{Tube} , W_{Tube} , H_{Tube} , T_{Tube} , Small deviations on WFF have high impact on electrical behaviour of CNTFET devices. After calculating the mean (μ) and standard deviation (σ), we normalize the standard deviation by dividing with mean (σ/μ) for checking the variability of the different device parameters [5, 18].

V. Results and Discussion

In Table III, dynamic power is measured by using Cu and CNTFET interconnects over various logic gates in term of performance parameters like Average power, delay, PDP and EDP. In Table IV, Static power is measured over various logic gates with all input vector combination of Cu and CNTFET interconnects with the variation of temperature from 25°C to 110°C in order to check the failure rate at higher degree.

Table. III. Dynamic Power Measuring by using Cu and CNTFET Interconnects

Logic Gates	Temp.	CMOS CU-Interconnects				CNTFET-CNT Interconnects			
		Average Power (μ W)	Delay (pS)	PDP (aJ)	EDP	Average Power	Delay	PDP	EDP
NOT	25°C	0.126	1.009	0.127	0.128	0.0281	1.419	0.039	0.055
	110°C	0.710	0.867	0.615	0.533	0.1882	1.332	0.250	0.333
NOR	25°C	0.130	2.497	0.324	0.809	0.1005	10.77	1.082	11.65
	110°C	0.627	2.361	1.480	3.494	0.2516	9.143	2.300	21.02
AND	25°C	0.345	4.923	1.698	8.359	0.2053	14.18	2.911	21.27
	110°C	1.785	8.678	15.47	134.2	0.5930	13.73	8.141	111.7
NAND	25°C	0.143	5.715	0.817	4.669	0.1017	11.82	1.202	14.20
	110°C	1.045	5.636	5.889	33.19	0.3587	11.72	4.203	49.25
EXOR	25°C	0.270	8.315	2.245	18.66	0.1650	18.91	3.120	58.99
	110°C	1.298	7.856	10.19	80.05	0.4490	17.58	7.893	138.75
EXNOR	25°C	0.261	7.584	1.978	15.00	0.1614	17.24	2.782	47.96
	110°C	1.294	7.316	9.466	69.25	0.4498	16.49	7.417	122.1

Table. IV. Static Power Measuring by using Cu and CNTFET Interconnects

Logic Gates	Temp.	CMOS CU-Interconnects				CNTFET-CNT Interconnects			
		00	01	10	11	00	01	10	11
NOT	25°C	6.043	0.788			1.259	0.150		
	110°C	75.33	31.62			19.48	8.537		
NOR	25°C	12.08	0.786	0.727	0.0511	2.516	0.149	0.118	0.0089
	110°C	150.04	29.10	29.39	3.256	38.84	8.217	7.001	0.8132
AND	25°C	9.860	15.45	15.35	7.632	0.594	1.743	1.707	1.560
	110°C	313.3	384.4	384.8	143.2	29.25	46.30	45.91	36.98
NAND	25°C	0.458	6.025	5.924	1.576	0.110	1.258	1.223	0.300
	110°C	8.450	73.26	73.64	62.61	2.485	19.26	18.87	16.97
EXOR	25°C	1.512	11.90	11.86	1.512	0.267	2.478	2.478	0.267
	110°C	58.75	146.3	146.1	58.75	15.16	38.02	38.02	15.16
EXNOR	25°C	12.04	1.571	1.454	11.84	2.513	0.299	0.236	2.442
	110°C	145.95	58.89	58.60	146.8	38.39	16.34	13.99	37.65

Table.V shows the value of I_{ON} and I_{OFF} current for Cu and CNTFET interconnects over NFET and PFET transistor with the variation of tube from 1 to 32. As No of tube increases there is a variation in I_{ON} and I_{OFF} current. When Cu-NFET interconnect is compared with CNT-NFET interconnect, saves I_{ON} current upto 41.77% and I_{OFF} current upto 4.4% for single CNTFET tube. For CNT-PFET saves I_{ON} current upto 41.35% and I_{OFF} current 2.1% when compared with Cu-PFT, there is a drastic change in I_{ON} current and very small change in I_{OFF} current due to the threshold voltage variation.

Table.V. Results of I_{ON} and I_{OFF} for No. of Tubes by using CU and CNT- Interconnects

Modes	I_{ds}	No. of Tubes=1	No. of Tubes =4	No. of Tubes =8	No. of Tubes =16	No. of Tubes =32
Cu NFET	I_{ON} (μA)	88.41	353.6	707.3	1414	2829
	I_{OFF} (nA)	6.555	26.22	52.44	104.8	209.7
Cu PFET	I_{ON} (μA)	78.29	313.1	626.3	1252	2505
	I_{OFF} (nA)	6.338	25.35	50.17	101.4	202.8
CNT- NFET	I_{ON} (μA)	51.48	205.9	411.8	823.6	1647
	I_{OFF} (nA)	6.262	25.04	50.09	100.1	200.3
CNT- PFET	I_{ON} (μA)	45.91	183.6	326.2	734.5	1469
	I_{OFF} (pA)	6.200	24.88	49.75	99.51	199.0

Table.VI. Results of Nominal I_{ON} and I_{OFF} for Multiple Fin and I_{ON} and I_{OFF} considering geometric Variability in Gate Length (L) of the Tube

Modes	I_{ds}	Nominal	No. of Tubes=1		No. of Tubes =4		No. of Tubes =8		No. of Tubes =16	
			Mean	SD	Mean	SD	Mean	SD	Mean	SD
Cu NFET	I_{ON} (μA)	88.41	88.39	0.525	353.5	2.103	707.1	4.207	1414	8.414
	I_{OFF} (nA)	6.555	7.157	2.923	28.62	11.69	57.25	23.38	114.5	46.77
Cu PFET	I_{ON} (μA)	78.29	78.27	0.474	313.1	1.897	626.1	3.796	1252	7.589
	I_{OFF} (nA)	6.338	7.039	3.203	28.15	12.81	56.31	25.62	112.6	51.25
CNT- NFET	I_{ON} (μA)	51.48	51.47	0.043	205.9	0.177	411.8	0.355	823.5	0.710
	I_{OFF} (nA)	6.262	6.829	2.777	27.31	11.10	54.62	22.21	109.2	44.43
CNT- PFET	I_{ON} (μA)	45.91	45.90	0.008	183.6	0.035	367.2	0.070	734.5	0.140
	I_{OFF} (pA)	6.200	6.840	2.942	27.36	11.77	54.72	23.54	109.4	47.08

Table. VII. Results of Nominal I_{ON} and I_{OFF} for Multiple Fin and I_{ON} and I_{OFF} considering geometric Variability in Width (W_{Fin}) of the Tube

Modes	I_{ds}	Nominal	No. of Tubes=1		No. of Tubes =4		No. of Tubes =8		No. of Tubes =16	
			Mean	SD	Mean	SD	Mean	SD	Mean	SD
Cu NFET	I_{ON} (μA)	91.05	91.04	0.720	364.2	2.881	728.4	5.762	1456	11.52
	I_{OFF} (nA)	5.949	6.268	2.075	25.07	8.300	51.14	16.60	100.2	33.20
Cu PFET	I_{ON} (μA)	80.30	80.30	0.676	321.2	2.706	642.4	5.412	1284	10.82
	I_{OFF} (nA)	5.693	6.050	2.172	24.20	8.689	48.40	17.37	96.80	34.75
CNT- NFET	I_{ON} (μA)	51.27	51.27	0.551	205.0	2.204	410.1	4.408	820.3	8.816
	I_{OFF} (nA)	5.813	6.247	2.427	24.98	9.709	49.97	19.42	99.94	38.83
CNT- PFET	I_{ON} (μA)	45.70	45.71	0.536	182.8	2.146	365.6	4.293	731.3	8.586
	I_{OFF} (pA)	5.924	6.406	2.606	25.62	10.42	51.24	20.85	102.4	41.70

Table. VIII. Results of Nominal I_{ON} and I_{OFF} for Multiple Fin and I_{ON} and I_{OFF} considering geometric Variability in Threshold Voltage (V_{th}) of the Tube

Modes	I_{ds}	Nominal	No. of Tubes=1		No. of Tubes =4		No. of Tubes =8		No. of Tubes =16	
			Mean	SD	Mean	SD	Mean	SD	Mean	SD

Cu NFET	I_{ON} (μA)	94.14	94.14	0.788	376.5	3.155	753.1	6.311	1506	12.62
	I_{OFF} (nA)	5.204	5.500	1.881	22.00	7.527	44.00	15.05	88.00	30.11
Cu PFET	I_{ON} (μA)	86.49	86.49	0.835	345.9	3.342	691.9	6.685	1383	13.37
	I_{OFF} (nA)	5.014	5.344	1.976	21.37	7.904	42.75	15.81	85.51	31.61
CNT- NFET	I_{ON} (μA)	49.78	49.78	0.581	199.1	2.324	398.3	4.649	796.6	9.298
	I_{OFF} (nA)	4.919	5.288	2.067	21.15	8.271	42.30	16.54	84.60	33.08
CNT- PFET	I_{ON} (μA)	45.65	45.65	0.615	182.6	2.461	365.2	4.922	730.5	9.845
	I_{OFF} (pA)	4.970	5.375	2.197	21.50	8.788	42.99	17.57	85.99	36.15

Table. XI. Results of Nominal I_{ON} and I_{OFF} for Multiple Fin and I_{ON} and I_{OFF} considering geometric Variability in Thickness (t_{ox}) of Tube

Modes	I_{ds}	Nominal	No. of Tubes=1		No. of Tubes =4		No. of Tubes =8		No. of Tubes =16	
			Mean	SD	Mean	SD	Mean	SD	Mean	SD
Cu NFET	I_{ON} (μA)	89.97	89.97	0.770	359.9	3.083	719.8	6.166	1439	12.33
	I_{OFF} (nA)	4.704	4.982	1.737	19.92	6.951	39.85	13.90	79.71	27.80
Cu PFET	I_{ON} (μA)	82.66	82.66	0.789	330.6	3.157	661.3	6.314	1322	12.62
	I_{OFF} (nA)	4.584	4.889	1.817	19.56	7.268	39.11	14.53	78.23	28.07
CNT- NFET	I_{ON} (μA)	43.78	43.79	0.540	175.1	2.160	350.3	4.320	700.6	8.640
	I_{OFF} (nA)	4.475	4.778	1.744	19.11	7.096	38.22	14.19	76.44	28.38
CNT- PFET	I_{ON} (μA)	39.27	39.27	0.570	157.1	2.280	314.2	4.560	628.4	9.121
	I_{OFF} (pA)	4.448	4.795	1.921	19.18	7.687	38.35	15.37	76.71	30.75

Table.X. Results of Nominal I_{ON} and I_{OFF} for Multiple Fin and I_{ON} and I_{OFF} considering geometric Variability in Source & Drain Doping concentration of CNFTFET

Modes	I_{ds}	Nominal	No. of Tubes=1		No. of Tubes =4		No. of Tubes =8		No. of Tubes =16	
			Mean	SD	Mean	SD	Mean	SD	Mean	SD
Cu NFET	I_{ON} (μA)	81.94	81.99	0.716	327.9	2.867	655.9	5.735	1311	11.47
	I_{OFF} (nA)	3.973	4.195	1.439	16.78	5.756	33.56	11.51	67.13	23.02
Cu PFET	I_{ON} (μA)	72.20	72.20	0.708	288.8	2.833	577.6	5.666	1155	11.33
	I_{OFF} (nA)	3.824	4.072	1.497	16.28	5.987	32.57	11.97	65.15	23.95
CNT- NFET	I_{ON} (μA)	35.16	35.16	0.526	140.6	2.105	281.3	4.210	562.6	8.421
	I_{OFF} (nA)	3.782	4.035	1.493	16.13	5.973	32.27	11.27	64.55	23.89
CNT- PFET	I_{ON} (μA)	31.47	31.47	0.529	125.9	2.117	251.8	4.233	503.6	8.467
	I_{OFF} (pA)	3.762	4.029	1.539	16.11	6.155	32.23	12.31	64.46	24.62

Simulation for 1,4,8,16 Tubes CNT interconnects shows that 10% variation in WFF from its mean value gives I_{OFF} current deviation nearly 110% for tub1 and 158% for Tube 4,8,16 which is the highest average standard deviation of I_{OFF} . With number of Tubes variation along with deviation in parameters that 10% deviation from mean value of Length shows 42%, Width shows 38% , Height shows 7% ,WFF shows 115%, T_{Tube} shows 36%, N shows

32% average standard deviation in I_{OFF} respectively. Hence it can be said that Tubes as well as parameters variation shows more I_{OFF} deviation than I_{ON} .

Fig.10. Leakage Power in Bench Mark Circuits using Cu and CNT-Interconnects

Fig.10. shows leakage power consumption over standard bench mark circuits by using Cu and CNTFET interconnects for validation and verification of results. Here Cu interconnects consume more power than CNTFET interconnects in C17 (ISCAS 85) saves upto 47.56%, B01 (ITC 99) saves upto 41.3%, B02 (ITC 99) saves upto 49.4% and B06 (ITC 99) 52.32%.

VI. Conclusion

An unprecedented approach in Cu and CNTFET interconnects for delay, power dissipation and PDP optimization which results drastically reduction in energy consumption. This article proposes PVT variation on different parameters for high speed and low-power interconnects applications. These P-CNTFETs have high V_{th} and reduces leakage current during idle state. Result analysis points out that compared to conventional Cu interconnect, the CNT interconnects paired with CNTFET interconnect designs are more energy efficient. CNT-Interconnect saves dynamic power by 89.96%, reduces propagation delay by 77.5% and leakage power dissipation is reduced by 89%. With the reduction of feature size of the device, lower supply voltage and complex vector set, and also there are several issues with scaling to maintain same electric field with new methodologies of design and new EDA tools that would be capable to deal with the latest fabrication process and variability challenges.

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