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Research Article

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Posted Date: September 3rd, 2021

DOI: <https://doi.org/10.21203/rs.3.rs-859825/v1>

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Performance analysis of dual material junction accumulation mode tri gate junctionless SOI FET: Modeling and Simulation

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Abstract

The paper illustrates the performance of Tri-Gate (TG) Dual Material (DM) SOI (Silicon on Insulator) Junctionless (JL) FET operating in Junction Accumulation Mode (JAM). An analytical model is developed to evaluate its performance. The device is also simulated using Silvaco device simulator. Both the analytical and simulation results are compared and found to match closely. Quasi 3-D modeling approach is adopted here to determine the surface potential of the above device. In this technique, the entire 3-D device is segregated into two 2-D devices with certain physical constraints. These 2-D devices are then analyzed separately to obtain the surface potentials, which are added together using suitable multiplication factors to get the surface potential of the 3-D device. This surface potential is, in turn, used to model the threshold voltage, sub-threshold drain current ($I_{d,sub}$) and the drain induced barrier lowering (DIBL). The proposed device configuration reduces the I_{OFF} significantly and offers excellent immunity to SCEs. The response of the proposed device is studied for the variations of certain device parameters, such as, thickness of High- K dielectric layer in stack gate, channel doping, and the work-functions as well as lengths of the gate metals. Such study will lead to turn the proposed device immune to short channel effects through proper choice of various parameters.

Keywords: DM JL JAM SOI TG JLFET, symmetric DMG-JLFET, asymmetric SOI-JLFET, SCEs

1 Introduction

Junctionless field-effect transistor (JLFET) has become the promising device in present days due to its simpler fabrication process. The absence of conventional p-n junctions makes further downscaling of device dimensions feasible. Other features of JL FET include, high $I_{ON} : I_{OFF}$ ratio [1], minimum thermal budgeting, almost ideal subthreshold swing and better roll-off [1]-[2]. In spite of having these advantages, JL FET suffers from mobility degradation due to heavily doped channels, and reduction in ON-current (I_{ON}) because of high parasitic resistances [3]-[4]. To resolve the issue of ON-current reduction, Junction Accumulation Mode (JAM) FET has been introduced [5]-[6]. The scheme of maintaining heavy doping in the source/drain region, while lowering the channel doping, enhances both the I_{ON} , and $I_{ON} : I_{OFF}$ ratio compared to those in JLFET [7]-[8]. At the ON-state, high electric field at the channel/drain interface gives rise to the hot-electron effects (HCEs) and gate induced drain leakage (GIDL). Gate engineering using dual material has been established as an effective approach to get rid of the reliability issues caused by HCEs and short channel effects (SCEs) in various FET architectures [9]-[13]. Reduction of gate oxide thickness leads to the gate direct tunneling [14]. Such gate leakage current that occurs due to tunneling can be suppressed by replacing the conventional gate oxide (SiO_2) with dielectric material of high- K value [15]. However, formation of the high- K material layer over Si-film creates a rough Si-Insulator interface, which causes the surface scattering

and thereby, mobility degradation of carriers [16]. Formation of dual oxide layer (high- K oxide on top of a thin SiO_2 layer), commonly referred to as Gate stacking [17], offers an effective solution to the problem of mobility degradation [18].

Among various gate structures, Tri-gate (TG) provides excellent gate control in sub-100 nm regime and thus attracts lots of research attention. Reduced surface scattering, subthreshold swing (SS) and drain induced barrier lowering (DIBL) make the tri-gate (TG) JLFETs more suitable for analog and digital applications [9], [19]-[22]. Improvement in gate-channel electrostatics gives rise to immunity to SCEs, and consequently, pushes down the device scaling limits [23]. Thus, TG-JLFET architecture that possesses the features of both JLFETs and multi gate FETs deserves special attention to prove its suitability in the short-channel regime. With the increasing demand for high packing density, feature size of the device gets reduced. As a result, the SCEs and parasitic capacitances become stronger [24]. Such parasitic capacitances can be controlled by the Silicon-on-Insulator (SOI) technology [25].

Various analytical modeling have been presented in numerous literatures. Katti *et. al.* in [26] modeled a fully depleted SOI MOSFET considering small geometry by solving the 3D Poisson's equation. 3D model of tri-gate JL nano-wire MOSFET with quantum effects was proposed by Holtij *et. al.* [27]. Auth *et. al.* [28] proposed a quasi-3D model that involves mathematics of reduced complexity without compromising the accuracy of the model. In this model,

3D device was split into two 2D devices to solve the potential function. This technique, applied in tri-gate MOSFET with lightly doped channel, yielded accurate results [29]. Various research works were carried out based on the above quasi-3D model [30]-[31], which will also be adopted in this communication.

To the best of our knowledge, analytical modeling of DM JL JAM SOI TG JLFET with gate stacking is reported here for the first time. In this paper, the proposed device will be analyzed on the basis of variant device parameters such as, thickness of High- K dielectric layer, channel doping, work-functions and lengths of the gate metals. The proposed JL FET will be modeled based on the quasi-3D modeling technique, in which the 3D potential function will be obtained by the weighted sum approximated approach of surface potentials. Analytical modeling of threshold voltage, subthreshold current and DIBL will also be derived from the approximated surface potential. The proposed device will be simulated by TCAD from Silvaco ATLAS device simulator, in order to validate the model. The performance of the device will be analyzed based on the surface potential, threshold voltage, drain current and DIBL.

The literature is organized in a couple of sections, starting from the introduction, which is followed by the device structure and model description. In the next section, analytical modeling is elaborated. Thereafter, the model validation and simulation setup are briefed, which is followed by the result and discussion section. Finally, the study is

concluded by enlightening the major findings of this work.

2 Device Structure and Model Description

The 3-D view of a DM JL JAM SOI TG JLFET is presented in Fig. 1(a). The top view of the device shows a symmetric double-gate structure [as depicted in Fig. 1(b)] and the side cross-sectional view [presented in Fig. 1(c)], which appears as an asymmetric SOI device. The Si-film is wrapped from three sides with stacked oxide layers (HfO_2 on top of SiO_2) of thickness t_{HfO_2} and t_{SiO_2} respectively, while the effective oxide thickness (EOT) of t_{ox} is maintained. Two metals with different work functions (ϕ_{M1} and ϕ_{M2}) are used to form the gate. Different donor densities are considered here for the channel and source/drain (S/D) regions. S/D are doped with higher doping (N_{SD}) whereas, the channel is doped with slightly lower dopant density (N_C) of the same type. The channel length, width and thickness (height) are assumed to be oriented along x , y , and z -directions respectively.

Proposed device is analytically modeled, as reported in [28]-[29] with certain geometrical restrictions imposed on the device architecture. They are: i) thickness of the buried oxide layer (t_{box}) should be greater than or equal to the channel length (L) to reduce interaction between two side gates [29]; ii) channel length should be at least equal to twice of the width/thickness of the device or more, if not less i.e., $L \geq 2W$

Fig. 1 DM JL JAM SOI TG JLFET with gate stack: (a) 3-D schematic view, (b) Top cross-sectional view, (c) Side cross-sectional view, (d) Enlarged channel from side cross-section.

and $L \geq 2t_{si}$ [30]-[32]. In the perimeter-weighted sum approach, channel potential $[\psi(x, y, z)]$ at any point can be expressed as a function of $\psi(x, y)$ and $\psi(x, z)$. Here, $\psi(x, y)$ and $\psi(x, z)$ are the potential function of symmetrical double-gate structure and asymmetric SOI device, respectively. These potential functions are obtained from the analytical model by solving 2D Poisson's Equation.

2.1 Surface Potential Model:

The surface potential of the DM JL JAM SOI TG JLFET is derived by dividing it into symmetrical double-gate and asymmetrical SOI structures as shown in Fig. 1 (a), (b). The channel in both the structures is splitted into two sections, based on its overhead metal gate work function. These structures are modeled as follows,

2.1.1 For symmetric DMG-JLFETs:

Let, $\psi_1(x, y)$ and $\psi_2(x, y)$ be the potential profile for region-1 (with gate work function ϕ_{M1}) and region-2 (with gate work function ϕ_{M2}) respectively. The 2D Poisson's equation for both the regions are given by,

$$\frac{\partial^2 \psi_1(x, y)}{\partial x^2} + \frac{\partial^2 \psi_1(x, y)}{\partial y^2} = -\frac{q \cdot N_C}{\epsilon_{si}}; \quad 0 \leq x \leq L_1 \quad (1a)$$

$$\frac{\partial^2 \psi_2(x, y)}{\partial x^2} + \frac{\partial^2 \psi_2(x, y)}{\partial y^2} = -\frac{q \cdot N_C}{\epsilon_{si}}; \quad L_1 \leq x \leq L \quad (1b)$$

Where, q , ϵ_{si} and N_C represent the electron charge, permittivity of Si-substrate and channel doping concentration respectively. The potentials in the channel are assumed to

maintain the parabolic profile [31] and can be represented as,

$$\psi_1(x, y) = B_{11}(x) + B_{12}(x) \cdot y + B_{13}(x) \cdot y^2 \quad (2a)$$

$$\psi_2(x, y) = B_{21}(x) + B_{22}(x) \cdot y + B_{23}(x) \cdot y^2 \quad (2b)$$

Where, the x dependent coefficients, i.e., $B_{11}(x)$, $B_{12}(x)$, $B_{13}(x)$, $B_{21}(x)$, $B_{22}(x)$ and $B_{23}(x)$ can be obtained using the boundary conditions [?] as follows,

A) The surface potential at $y=0$ for region-1 and 2 are given by:

$$\psi_1(x, 0) = \psi_{d1}(x) = B_{11}(x) \quad (3a)$$

$$\psi_2(x, 0) = \psi_{d2}(x) = B_{21}(x) \quad (3b)$$

B) The electric field at the top of the channel ($y=0$) for both the regions are given by:

$$\begin{aligned} \frac{\partial \psi_1(x, y)}{\partial y} &= \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_{d1}(x) - (V_{gs} - V_{fb.1})}{t_{ox}} \\ &= B_{12}(x) \end{aligned} \quad (4a)$$

$$\begin{aligned} \frac{\partial \psi_2(x, y)}{\partial y} &= \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_{d2}(x) - (V_{gs} - V_{fb.2})}{t_{ox}} \\ &= B_{22}(x) \end{aligned} \quad (4b)$$

C) The electric field at the bottom of the channel ($y=W$) is given by:

$$\frac{\partial \psi_1(x, y)}{\partial y} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{(V_{gs} - V_{fb.1}) - \psi_{d1}(x, W)}{t_{ox}} \quad (5a)$$

$$\frac{\partial \psi_2(x, y)}{\partial y} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{(V_{gs} - V_{fb.2}) - \psi_{d2}(x, W)}{t_{ox}} \quad (5b)$$

D) The surface potential at the source end ($x=0$) is given by,

$$\psi_{d1}(0) = \psi_1(0, 0) = V_{bi.1} = V_T \cdot \ln \left(\frac{N_{SD}}{n_i} \right) \quad (6)$$

Where V_T is the volt equivalent temperature ($=kT/q$).

E) The surface potential at the boundary of two regions ($x = L_1$) is given by

$$\psi_{d1}(L_1) = \psi_1(L_1, 0) = V_m \quad (7)$$

Where V_m is the surface potential developed at the boundary of two regions. F) The surface potential at the drain end ($x=L$) is given by

$$\psi_{d2}(L) = \psi_2(L, 0) = V_{ds} + V_{bi.2} = V_{ds} + V_T \cdot \ln \left(\frac{N_{SD}}{n_i} \right) \quad (8)$$

Considering these boundary conditions the generalized channel potential functions are obtained as,

$$\begin{aligned} \psi_1(x, y) &= \psi_{d1}(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_{d1}(x) - (V_{gs} - V_{fb.1})}{t_{ox}} y \\ &\quad - \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_{d1}(x) - (V_{gs} - V_{fb.1})}{t_{ox} \cdot W} y^2 \end{aligned} \quad (9a)$$

$$\begin{aligned} \psi_2(x, y) &= \psi_{d2}(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_{d2}(x) - (V_{gs} - V_{fb.2})}{t_{ox}} y \\ &\quad - \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_{d2}(x) - (V_{gs} - V_{fb.2})}{t_{ox} \cdot W} y^2 \end{aligned} \quad (9b)$$

And at $y=0$ the solution of the differential equations (1a), (1b) yields,

$$\psi_{d1}(x) = K_1 \cdot e^{(x/\lambda_1)} + K_2 \cdot e^{(-x/\lambda_1)} - P_1 \quad (10a)$$

$$\psi_{d2}(x) = K_3 \cdot e^{(x/\lambda_1)} + K_4 \cdot e^{(-x/\lambda_1)} - P_2 \quad (10b)$$

The expressions of λ_1 , K_1 , K_2 , K_3 , K_4 , P_1 and P_2 are given in Appendix.

2.1.2 For asymmetric SOI-JLFET:

Following the previous analytical model of determining the surface potential, the asymmetric SOI-JLFET is also modeled in this section. $\psi_1(x, z)$, $\psi_2(x, z)$ be the 2-D potential function of region-1 and 2, which can be obtained by solving the 2D Poisson's Equation as follows,

$$\frac{\partial^2 \psi_1(x, z)}{\partial x^2} + \frac{\partial^2 \psi_1(x, z)}{\partial z^2} = -\frac{q \cdot N_C}{\epsilon_{si}}; \quad 0 \leq x \leq L_1 \quad (11a)$$

$$\frac{\partial^2 \psi_2(x, z)}{\partial x^2} + \frac{\partial^2 \psi_2(x, z)}{\partial z^2} = -\frac{q \cdot N_C}{\epsilon_{si}}; \quad L_1 \leq x \leq L \quad (11b)$$

Considering the parabolic potential distribution along the channel region, the potential functions ($\psi_1(x, z)$, $\psi_2(x, z)$) may take the following form,

$$\psi_1(x, z) = C_{11}(x) + C_{12}(x) \cdot z + C_{13}(x) \cdot z^2 \quad (12a)$$

$$\psi_2(x, z) = C_{21}(x) + C_{22}(x) \cdot z + C_{23}(x) \cdot z^2 \quad (12b)$$

The co-efficients $C_{11}(x)$, $C_{12}(x)$, $C_{13}(x)$, $C_{21}(x)$, $C_{22}(x)$ and $C_{23}(x)$ can be obtained using the boundary conditions ((3) to (8)) for this asymmetric structure. The potential profiles at $z=0$ may hold the following form,

$$\psi_{s1}(x) = K_5 \cdot e^{(x/\lambda_2)} + K_6 \cdot e^{(-x/\lambda_2)} - D_1 \quad (13a)$$

$$\psi_{s2}(x) = K_7 \cdot e^{(x/\lambda_2)} + K_8 \cdot e^{(-x/\lambda_2)} - D_2 \quad (13b)$$

The expressions of related coefficients are illustrated in Appendix. The generalized potential function at any point in the channel region of the 3D DM JL JAM SOI TG JLFET can be obtained by multiplying

$\psi_i(x, y)$ and $\psi_i(x, z)$ ($i = 1, 2, d1, s1$) with appropriate factors, as follows,

$$\psi_1(x, 0, 0) = \alpha_1 \psi_{d1}(x) + \alpha_2 \psi_{s1}(x) \quad (14a)$$

$$\psi_2(x, 0, 0) = \alpha_1 \psi_{d2}(x) + \alpha_2 \psi_{s2}(x) \quad (14b)$$

$$\psi_1(x, y, z) = \alpha_1 \psi_1(x, y) + \alpha_2 \psi_1(x, z) \quad (14c)$$

$$\psi_2(x, y, z) = \alpha_1 \psi_2(x, y) + \alpha_2 \psi_2(x, z) \quad (14d)$$

2.1.3 Expression of V_m :

The voltage at the interface of two regions (region-1 and region-2) (V_m) is determined in this section. Interface voltage ($V_{m(DMG)}$) of symmetric DMG-JLFETs can be obtained by making electric field in Region-1 and electric field in Region-2 equal at $x = L_1$ (electric field continuity).

$$\left. \frac{\partial \psi_{d1}(x)}{\partial x} \right|_{x=L_1} = \left. \frac{\partial \psi_{d2}(x)}{\partial x} \right|_{x=L_1} \quad (15)$$

The expression of $V_{m(DMG)}$ is

$$V_{m(DMG)} = \frac{K_{11} \{e^{(L_1/\lambda_1)} + e^{(-L_1/\lambda_1)}\} + 2K_{12}e^{(L_1/\lambda_1)} + K_9}{K_{10} \{e^{(L_1/\lambda_1)} + e^{(-L_1/\lambda_1)}\} + 2K_{13}e^{(L_1/\lambda_1)} + 1} \quad (16)$$

Interface voltage ($V_{m(SOI)}$) needs to be measured for the asymmetric SOI-JLFET structure also following the similar approach mentioned above. $V_{m(SOI)}$ is obtained as,

$$V_{m(SOI)} = \frac{K_{16} \{e^{(L_1/\lambda_2)} + e^{(-L_1/\lambda_2)}\} + 2K_{17} \cdot e^{(L_1/\lambda_2)} + K_{14}}{K_{15} \{e^{(L_1/\lambda_2)} + e^{(-L_1/\lambda_2)}\} + 2K_{18} \cdot e^{(L_1/\lambda_2)} + 1} \quad (17)$$

2.2 Threshold voltage (V_{th})

Model:

The threshold voltage is measured as the value of gate voltage (V_{gs}) at which minimum surface potential reaches to the twice

of its bulk Fermi potential [33]. Mathematically,

$$\psi_{d/si}(x = x_{min}) = \phi_f \quad (18)$$

In DMG-JLFET, for region-1, $x_{min} = (\lambda_1/2) \ln \left(\frac{K_2}{K_1} \right)$ and for region-2, $x_{min} = (\lambda_1/2) \ln \left(\frac{K_4}{K_3} \right)$. Putting these expressions of x_{min} in (10a) and (10b) yield,

$$\psi_{d1}(x = x_{min}) = 2\sqrt{K_1 K_2} - P_1 \quad (19a)$$

$$\psi_{d2}(x = x_{min}) = 2\sqrt{K_3 K_4} - P_2 \quad (19b)$$

P_1 , P_2 , $V_{m(DMG)}$, K_1 , K_2 , K_3 , K_4 can be expressed as,

$$\begin{aligned} P_1 &= K_{19} - V_{gs}; & P_2 &= K_{20} - V_{gs}; \\ V_{m(DMG)} &= K_{26} - V_{gs} K_{27} \\ K_1 &= K_{29} - V_{gs} K_{30}; & K_2 &= K_{31} - V_{gs} K_{32} \\ K_3 &= K_{33} - V_{gs} K_{34}; & K_4 &= K_{35} - V_{gs} K_{36} \end{aligned} \quad (20)$$

Putting these expressions in (19a) and (19b) yields,

$$K_{37} V_{gs}^2 - K_{38} V_{gs} + K_{39} = 0 \quad (21a)$$

$$K_{40} V_{gs}^2 - K_{41} V_{gs} + K_{42} = 0 \quad (21b)$$

The solution of which gives the threshold voltages (V_{th1} , V_{th2}) as follows,

$$V_{thd1} = \frac{-K_{38} \pm \sqrt{K_{38}^2 - 4K_{37}K_{39}}}{2K_{37}} \quad (22a)$$

$$V_{thd2} = \frac{-K_{41} \pm \sqrt{K_{41}^2 - 4K_{40}K_{42}}}{2K_{40}} \quad (22b)$$

Therefore, the threshold voltage ($V_{th,DMG}$) of DMG-JLFET is the maximum of the two threshold voltages which may invert the entire surface underneath both the gates, i.e., $V_{th,DMG} = (V_{thd1}, V_{thd2})|_{max}$.

Similarly, the threshold voltage for the two

regions and the entire asymmetric SOI-JLFET structure can be obtained and denoted as $V_{th_{s1}}$, $V_{th_{s2}}$, and $V_{th,SOI} = (V_{th_{s1}}, V_{th_{s2}})|_{max}$, respectively.

Thus, the threshold voltage of the DM JL JAM SOI TG JLFET is

$$V_{th} = \alpha_1 V_{th,DMG} + \alpha_2 V_{th,SOI} \quad (23)$$

2.3 Sub-threshold drain current ($I_{d,sub}$) Model:

Modeling of sub-threshold drain current is obtained from the current density along x -direction [34], [35]. The expression is derived taking into account of the drift and the diffusion components of the carriers, as follows,

$$\begin{aligned} I_{d,sub} &= \frac{kTW\mu_n n_i (1 - e^{(-V_{ds})/V_T})}{\int_0^{L_1} \frac{dx}{\int_0^{t_{si}} e^{\psi_1(x)/V_T} dy} + \int_{L_1}^L \frac{dx}{\int_0^{t_{si}} e^{\psi_2(x)/V_T} dy}} \end{aligned} \quad (24)$$

Here, $\psi_1(x)$, $\psi_2(x)$ are obtained from (14a, 14b).

2.4 DIBL:

The DIBL is measured as the deterioration of V_{th} [13]. At a specific V_{ds} , DIBL can be obtained by the following expression,

$$DIBL = - \frac{V_{th}(V_{ds} = 50mV) - V_{th}(V_{ds})}{0.05 - V_{ds}} \quad (25)$$

3 Analytical and Simulation Results

3.1 Device Parameters and Simulation

The DM JL JAM SOI TG JLFET is studied for the parameters are given in Table 1. All the simulations are carried out in Silvaco ATLAS device simulator using the standard density models. Major models con-

Fig. 2 Model is calibrated with the experimental data [38] at $V_{ds} = 0.8$ V.

sidered during the simulation process are Drift-Diffusion model, Shockley-Read-Hall (SRH) recombination model and Lombardi Mobility Model [36]. Robust Meshing strategy is adopted for accuracy. The empirical terms introduced in the model are taken from [35], [37]. The body (substrate) and the source terminals are shorted and connected to ground. The model data of transfer characteristics is calibrated with the experimental data [38] in Fig. 2. The data obtained from simulation and analytical modeling are plotted and analyzed to examine the performance of the device.

Fig. 3 Surface Potential variation along the channel at $V_{gs} = 0.5$ V and $V_{ds} = 0.5$ V, for a) $t_{HfO2} = 1.5$ nm, 2.5 nm and 3.5 nm b) $N_c = 10^{16} \text{ cm}^{-3}$ and 10^{18} cm^{-3} , c) $L_1 : L_2 = 1:1, 1:2$ and $2:1$ d) $\phi_{M1}, \phi_{M2} = (5.2 \text{ eV}, 4.7 \text{ eV})$ and $(5.3 \text{ eV}, 4.8 \text{ eV})$.

Table 1 Device dimensions and biasing voltages used for Simulations

Parameters	Values
High- K oxide (HfO_2) layer thickness (t_{HfO_2})	1.5 nm, 2.5 nm, 3.5 nm
Work-functions of dual metal gate (ϕ_{M1} , ϕ_{M2})	(5.2 eV, 5.3 eV), (4.7 eV, 4.8 eV)
Ratio of dual metal gate length ($L_1 : L_2$)	1:1, 1:2, 2:1
Channel doping (N_C)	10^{16} cm^{-3} , 10^{18} cm^{-3}
Channel length (L)	20 nm - 60 nm
Source/Drain doping (N_{SD})	10^{20} cm^{-3}
Thickness of the buried oxide layer (t_{box})	60 nm
Thickness and width of Si-film (t_{Si} , W)	10 nm, 10 nm
Gate voltage (V_{gs}), Drain Voltage (V_{ds})	0 - 1 V, 0.8 V

4 Results and Discussions

In this section, the data obtained from simulation and analytical modeling are plotted and analyzed to examine the performance of the device.

Fig. 3 (a)-(d) shows the surface potential variation along the channel length for different parameters. In Fig. 3(a), the above variation is presented for different high- K oxide thickness. With increase of t_{HfO_2} , the EOT increases and associated gate capacitance reduces. As a result the surface potential shifts upward reducing the immunity of the device from SCEs. Fig. 3(b) shows the similar variation for two different channel dopings, which are carefully chosen such that the device still works in junction accumulation mode (JAM). As channel doping increases, higher electron concentration in the channel enables the surface potential to move up. This implies that the device with higher channel doping, while working in JAM, is less shielded against SCEs. Fig. 3(c) presents the surface potential variation for different ratios of the lengths of gate metals with high and low work function ($L_1 :$

L_2). It can be seen that, as the length (L_1) of the gate metal of higher work function is reduced with the associated increase in the other gate metal length (L_2), the overall surface potential profile shifts upward, and the surface potential minimum shifts towards the source end. Since the upliftment is significant compared to the left shift of the surface potential minima, the device with this configuration of gate metal work-function is more influenced by drain voltage fluctuation. As the peak electric field shifts more towards the source side and that there is more uniform electric field in the channel. Fig. 3(d) presents the potential variation for different work functions of gate metals. Increase in the dual gate metal work functions raises the work function difference between the gate and the substrate, and thus, pushes the surface potential profile downwards. It results in enhancement of the device immunity against SCEs.

Variation of the threshold voltage with the channel length for different values of t_{HfO_2} , N_C , $L_1 : L_2$ and work functions are depicted in Fig. 4 (a) - (d). The smaller t_{HfO_2} raises the gate oxide capacitance that causes increase of the threshold voltage [in Fig. 4(a)]. Fig. 4 (b) shows the dependence of threshold voltage on the channel doping. It is observed from the figure that higher the channel doping, lower is the threshold voltage due to the increased channel conductivity. Thus, the leakage currents also increase. Fig. 4 (c) shows the threshold voltages for different values of $L_1 : L_2$ ratio. It is quite clear from the plot that lowering the length (L_1) of the gate metal of higher work function reduces the threshold voltage. The

Fig. 4 Plot of threshold voltage with the channel length variations at $V_{ds} = 0.8$ V, for a) $t_{HfO_2} = 1.5$ nm, 2.5 nm and 3.5 nm b) $N_C = 10^{16} \text{ cm}^{-3}$ and 10^{18} cm^{-3} , c) $L_1 : L_2 = 1:1$, $1:2$ and $2:1$ d) ϕ_{M1} , $\phi_{M2} = (5.2 \text{ eV}, 4.7 \text{ eV})$ and $(5.3 \text{ eV}, 4.8 \text{ eV})$.

variation in threshold voltage (V_{th}) for different gate work functions is depicted in Fig. 4 (d). V_{th} rises up with the increase in gate work function. The lower the V_{th} value, the device turns ON earlier. Therefore, with this work-function engineering, the same device can be operated as a low/high- V_{th} transistor, which is an important aspect of low power circuit design.

Fig. 5 (a) - (d) presents the transfer characteristics of the proposed device structure for the above device parameters. The drain current is plotted here in log scale as we are mainly interested in the sub-threshold current (I_{OFF}). The gate voltage is varied from 0 to 1 V, while the drain voltage is kept fixed at 0.8 V. It is evident from Fig. 5 (a) that the OFF-current increases with the increase in high- K oxide thickness. This occurs due to the fact that the threshold voltage reduces with the increment of t_{HfO_2} as evident from Fig. 4 (a). Thus, the device with a thinner high- K oxide (HfO_2) layer improves its immunity to SCEs. It can also be achieved with the reduced channel dopant concentration, as evident from Fig. 5 (b). Increase in channel doping enhances both the ON and OFF-current, thereby pushing the device more into the critical zone. Extending length of the gate metal of higher work-function reduces the I_{OFF} , causing improvement in device performance in the short channel regime [in Fig. 5 (c)]. Fig. 5 (d) indicates that the device with gate metals of higher work functions yields better sub-threshold behavior through reduction in the OFF-current.

The plot of DIBL versus channel length for different t_{HfO_2} , N_C , $L_1 : L_2$ and gate metal work functions are shown in Fig. 6 (a) - (d).

Fig. 5 Variation of sub-threshold drain current with the gate voltage at $V_{ds} = 0.8$ V, for a) $t_{HfO2} = 1.5$ nm, 2.5 nm and 3.5 nm b) $N_C = 10^{16} \text{ cm}^{-3}$ and 10^{18} cm^{-3} , c) $L_1 : L_2 = 1:1$, 1:2 and 2:1 d) $\phi_{M1}, \phi_{M2} = (5.2 \text{ eV}, 4.7 \text{ eV})$ and $(5.3 \text{ eV}, 4.8 \text{ eV})$.

Fig. 6 Variation of DIBL with channel length at $V_{ds} = 0.8$ V, for a) $t_{HfO2} = 1.5$ nm, 2.5 nm and 3.5 nm b) $N_C = 10^{16} \text{ cm}^{-3}$ and 10^{18} cm^{-3} , c) $L_1 : L_2 = 1:1$, 1:2 and 2:1 d) $\phi_{M1}, \phi_{M2} = (5.2 \text{ eV}, 4.7 \text{ eV})$ and $(5.3 \text{ eV}, 4.8 \text{ eV})$.

It is evident from Fig. 6 (a) that the device with short channel ($L < 25$ nm), the DIBL increases rapidly as channel length reduces, and more so for larger values of t_{HfO_2} . However, with the increase in channel length ($L > 25$ nm) DIBL reduces significantly for all t_{HfO_2} , as it should be. Fig. 6 (b) clearly shows that lower channel doping forces the DIBL to reduce remarkably. Hence, lower channel doping compared to the source/drain doping makes the device more immune to short channel effects. Fig. 6 (c) depicts that 2:1 gate length partition yields the lowest DIBL compared to other two partitions. The lowest DIBL is also obtained, as evident from Fig. 6 (d), for the reduced gate metal work functions.

In all of the above figures, the analytical and simulation results show close match.

5 Conclusion

In this work, the performance of a trigate dual material JAM SOI JLFET with gate stack has been studied based on analytical modeling, and numerical simulations performed in Silvaco TCAD. Derivation of surface potential, threshold voltage, drain current and DIBL are based on semi-analytical modeling (perimeter weighted sum approach). The performance of the proposed device has been investigated by varying several device parameters, such as high-K oxide layer thickness in gate stack, channel doping and gate metal work functions. Significant improvements in combating the SCEs are evident from graphical presentation of the simulation and analytical results.

Reduction in the channel doping, and

increase in the gate-metal work functions influence the device performance similarly, making the device robust against SCEs. The channel doping lowering from 10^{18} cm^{-3} to 10^{16} cm^{-3} has been found to result in 4% increase in V_{th} , 80% decrease in I_{OFF} and 16% reduction in DIBL. Again, increase in work-functions of both the gate metals by 0.1 eV induces 73% increment in V_{th} , while respectively 45% and 80% reduction in I_{OFF} and DIBL. With reduction in the high-K oxide layer thickness, the surface potential gets lowered, which in turn, increases the threshold voltage and decreases the OFF-current. To be more specific, reduction of t_{HfO_2} by 2 nm causes at most 6.4% rise in V_{th} and 70% fall in I_{OFF} ; but the DIBL suffers an increase by 7%. Therefore, our present study suggests that through proper choice of various device parameters (channel doping, high-K oxide thickness in gate stack) along with the appropriate materials (gate metals) may make the proposed device structure immune to SCEs and thereby, quite efficient while operating in short-channel regime for low power applications.

6 Appendix A

$$\begin{aligned}
 \lambda_1 &= \sqrt{\frac{t_{ox} \cdot W \cdot \epsilon_{si}}{2 \cdot \epsilon_{ox}}} \\
 P_1 &= -\left\{ \frac{q \cdot N_C \cdot \lambda_1^2}{\epsilon_{si}} + (V_{gs} - V_{fb.1}) \right\} \\
 K_1 &= \frac{V_m \cdot e^{(L_1/\lambda_1)} - V_{bi.1} + P_1 \{e^{(L_1/\lambda_1)} - 1\}}{e^{(2L_1/\lambda_1)} - 1} \\
 K_2 &= V_{bi.1} - K_1 + P_1 \\
 P_2 &= -\left\{ \frac{q \cdot N_C \cdot \lambda_1^2}{\epsilon_{si}} + (V_{gs} - V_{fb.2}) \right\}
 \end{aligned} \tag{26}$$

$$\begin{aligned}
 K_3 &= \frac{(V_{ds} + V_{bi.2}) \cdot e^{(L/\lambda_1)} - V_m \cdot e^{(L_1/\lambda_1)}}{e^{(2L/\lambda_1)} - e^{(2L_1/\lambda_1)}} \\
 &+ P_2 K_{25} \\
 K_4 &= e^{(L_1/\lambda_1)} \left\{ V_m - K_3 e^{(L_1/\lambda_1)} + P_2 \right\} \\
 \lambda_2 &= \frac{1}{\sqrt{b+c}}; \quad a = 2 \cdot t_{si} + \frac{\varepsilon_{ox} \cdot t_{si}^2}{\varepsilon_{si} \cdot t_{box}} \\
 b &= \frac{2 \cdot \varepsilon_{ox}}{a \cdot \varepsilon_{si} \cdot t_{box}}; \quad c = \frac{2 \cdot \varepsilon_{ox}}{\varepsilon_{si} \cdot t_{ox} \cdot a} \cdot \left(1 + \frac{t_{si} \cdot \varepsilon_{ox}}{t_{box} \cdot \varepsilon_{si}} \right) \\
 D_1 &= -\frac{q \cdot N_C}{\varepsilon_{si}} \cdot \lambda_2^2 - b(V_{sub} - V_{fb.b1}) \cdot \lambda_2^2 \\
 &- c(V_{gs} - V_{fb.1}) \cdot \lambda_2^2 \\
 K_5 &= \frac{V_m \cdot e^{(L_1/\lambda_2)} - V_{bi.1} + D_1(e^{(L_1/\lambda_2)} - 1)}{e^{(2L_1/\lambda_2)} - 1} \\
 K_6 &= V_{bi.1} - K_5 + D_1 \\
 D_2 &= -\frac{q \cdot N_d}{\varepsilon_{si}} \cdot \lambda_2^2 - b(V_{sub} - V_{fb.b2}) \cdot \lambda_2^2 \\
 &- c(V_{gs} - V_{fb.2}) \cdot \lambda_2^2 \\
 K_7 &= \frac{(V_{ds} + V_{bi.2}) \cdot e^{(L/\lambda_2)} - V_m \cdot e^{(L_1/\lambda_2)}}{e^{(2L/\lambda_2)} - e^{(2L_1/\lambda_2)}} \\
 &+ D_2 K_{25} \\
 K_8 &= (V_m + D_2) \cdot e^{(L_1/\lambda_2)} - K_7 \cdot e^{(2L_1/\lambda_2)} \\
 K_9 &= (V_{bi.1} + P_1) \cdot e^{(-L_1/\lambda_1)} \\
 K_{10} &= \frac{e^{(L_1/\lambda_1)}}{e^{(2L_1/\lambda_1)} - 1} \\
 K_{11} &= \frac{P_1 \cdot \{e^{(L_1/\lambda_1)} - 1\} - V_{bi.1}}{e^{(2L_1/\lambda_1)} - 1} \\
 K_{12} &= \frac{(V_{ds} + V_{bi.2}) \cdot e^{(L/\lambda_1)}}{e^{(2L/\lambda_1)} - e^{(2L_1/\lambda_1)}} + P_2 K_{25} \\
 K_{13} &= \frac{e^{(L_1/\lambda_1)}}{e^{(2L/\lambda_1)} - e^{(2L_1/\lambda_1)}}
 \end{aligned}
 \tag{27}$$

$$\begin{aligned}
 \alpha_1 &= \frac{2 \cdot t_{si}}{W + 2 \cdot t_{si}}; \quad \alpha_2 = 1 - \alpha_1 \\
 K_{14} &= (V_{bi.1} + D_1) \cdot e^{(-L_1/\lambda_2)} - D_2 \\
 K_{15} &= \frac{e^{(L_1/\lambda_2)}}{e^{(2L_1/\lambda_2)} - 1} \\
 K_{16} &= \frac{D_1 \cdot (e^{(L_1/\lambda_2)} - 1) - V_{bi.1}}{e^{(2L_1/\lambda_2)} - 1} \\
 K_{17} &= \frac{(V_{ds} + V_{bi.2}) \cdot e^{(L/\lambda_2)}}{e^{(2L/\lambda_2)} - e^{(2L_1/\lambda_2)}} + D_2 K_{25} \\
 K_{18} &= \frac{e^{(L_1/\lambda_2)}}{e^{(2L/\lambda_2)} - e^{(2L_1/\lambda_2)}} \\
 K_{19} &= -\frac{q \cdot N_C \cdot \lambda_1^2}{\varepsilon_{si}} + V_{fb.1} \\
 K_{20} &= -\frac{q \cdot N_C \cdot \lambda_1^2}{\varepsilon_{si}} + V_{fb.2} \\
 K_{21} &= \frac{K_{19} \cdot (e^{(L_1/\lambda_1)} - 1) - V_{bi.1}}{e^{(2L_1/\lambda_1)} - 1} \\
 K_{22} &= \frac{e^{(L_1/\lambda_1)} - 1}{e^{(2L_1/\lambda_1)} - 1} \\
 K_{23} &= (V_{bi.1} + K_{19}) e^{(-L_1/\lambda_1)} \\
 K_{24} &= \frac{(V_{ds} + V_{bi.2}) e^{(L/\lambda_1)}}{e^{(2L/\lambda_1)} - e^{(2L_1/\lambda_1)}} + K_{20} K_{25} \\
 K_{25} &= \frac{e^{(L/\lambda_1)} - e^{(L_1/\lambda_1)}}{e^{(2L/\lambda_1)} - e^{(2L_1/\lambda_1)}} \\
 K_{26} &= \frac{K_{21} \{e^{(L_1/\lambda_1)} - e^{(-L_1/\lambda_1)}\} + 2K_{24} e^{(L_1/\lambda_1)} + K_{23}}{K_{28}} \\
 K_{27} &= \frac{(K_{22} - 2K_{25}) e^{(L_1/\lambda_1)} - (K_{22} + 1) e^{(-L_1/\lambda_1)}}{K_{28}} \\
 K_{28} &= (K_{10} + 2K_{13}) e^{(L_1/\lambda_1)} + K_{10} e^{(-L_1/\lambda_1)} + 1
 \end{aligned}
 \tag{28}$$

$$\begin{aligned}
 K_{29} &= \frac{K_{26} - V_{bi.1} + K_{19}\{e^{(L_1/\lambda_1)} - 1\}}{e^{(2L_1/\lambda_1)} - 1} \\
 K_{30} &= \frac{K_{27} + e^{(L_1/\lambda_1)} - 1}{e^{(2L_1/\lambda_1)} - 1} \\
 K_{31} &= V_{bi.1} - K_{29} + K_{19}; \quad K_{32} = 1 - K_{30} \\
 K_{33} &= \frac{(V_{ds} + V_{bi.2} + K_{20})e^{(L/\lambda_1)}}{e^{(2L/\lambda_1)} - e^{(2L_1/\lambda_1)}} \\
 &\quad - \frac{(K_{20} + K_{26})e^{(L_1/\lambda_1)}}{e^{(2L/\lambda_1)} - e^{(2L_1/\lambda_1)}} \\
 K_{34} &= \frac{e^{(L/\lambda_1)} - (K_{27} + 1)e^{(L_1/\lambda_1)}}{e^{(2L/\lambda_1)} - e^{(2L_1/\lambda_1)}} \\
 K_{35} &= (K_{26} + K_{20})e^{(L_1/\lambda_1)} - K_{33}e^{(2L_1/\lambda_1)} \\
 K_{36} &= (K_{27} + 1)e^{(L_1/\lambda_1)} - K_{34}e^{(2L_1/\lambda_1)} \\
 K_{37} &= 1 - 4K_{30}K_{32} \\
 K_{38} &= 2K_{19} + 2\phi_f - 4K_{30}K_{31} - 4K_{29}K_{32} \\
 K_{39} &= K_{19}^2 + \phi_f(\phi_f + 2K_{19}) - 4K_{29}K_{31} \\
 K_{40} &= 1 - 4K_{34}K_{36} \\
 K_{41} &= 2K_{20} + 2\phi_f - 4K_{34}K_{35} - 4K_{33}K_{36} \\
 K_{42} &= K_{20}^2 + \phi_f(\phi_f + 2K_{20}) - 4K_{33}K_{35} \\
 &\quad (29)
 \end{aligned}$$

7 Authors Declarations

7.1 Ethics Approval

For this type of study formal consent is not required.

7.2 Consent to participate

Not applicable for this type of study.

7.3 Availability of data and materials

Authors are not willing to disclose the data and materials related to this research, as this work is a part of thesis.

7.4 Competing interests

The authors declare that they have no conflict of interest.

7.5 Funding

No funding is available for this work.

7.6 Authors' contributions

Mrinmoy Goswami: Software, Data curation, Writing-Original draft preparation, Writing.
Ankush Chattopadhyay: Conceptualization, Methodology, Reviewing and editing.
Chayanika Bose: Supervision, correction of manuscript.

7.7 Compliance with Ethical Standards

7.7.1 Disclosure of potential conflicts of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

7.7.2 Research involving Human Participants and/or Animals

Not applicable for this type of study.

7.7.3 Informed consent

Not applicable for this type of study.

7.8 Acknowledgements

We would like to thank the Department of ETCE, Jadavpur University for their constant support for providing the access of the laboratory.

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