Design and Parametric Analysis of GaN on Silicon High Electron Mobility Transistor for RF Performance Enhancement

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Research Article

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Posted Date: September 3rd, 2021

DOI: https://doi.org/10.21203/rs.3.rs-865726/v1

Design and Parametric Analysis of GaN on Silicon High Electron Mobility Transistor for RF Performance Enhancement

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Abstract—**The need of performance enhancement at the RF and millimeter wave is highly desirable to eliminate the heating effects and power dissipation. Silicon substarte found to be a suitable candidate which reduces about 70% channel temperature than sapphire. To achieve high performance, a GaN on the Silicon substrate high electron mobility transistor is designed and its various performance paramters are analyzed by varying the design specifications. Moreover, the problem of blocking voltage improvement is resolved by epitaxial design approach. Since, threshold voltage, doping-level, work-function of gate material and channel length are considered as some of the important parameters while device modeling. Therefore, the impact of these parameters is examined and analyzed to enehace the performance and reliability of the device for RF applications. The performance parameters like trans-conductance, drain current curves are plotted at different state of device physical and electrical parameters. Results exhibits maximum value of transconductance g_m=13 milli-mho, minimum gate capacitance C_g=0.5pf, wheras V_{th} is varied between -0.25 volts to 0.25 volts.**

Keywords— **GaN on Silicon, high electron mobility transistor, gate work-function, doping effects, 2 dimensional electron gas.**

I. INTRODUCTION

With the continue down scaling of the transistor leads to switching speed and its efficiency losses in terms of short channel effects and hence renders large power dissipation. Form the past two decades, all the device are reliable on the silicon material for power device, however the silicon has some limits on handling high power devices [1-2]. In some domains, the power electronic devices are reaching to its fundamental limits, where the design and manufacturing unit facing the challenge in terms of operating voltage, temperature and frequency [3-5]. As alternatives of sapphire substarte, researchers move to Silicon substrate for wide bandgap materials such as GaN or SiC. The related semiconductor like GaN/AlGaN/InGaN on Silicon substrate have been continuously recorded as a promising device for the next generation of high frequency, high electric field with wide temperature range [6-8]. In particular, hetero-structure base on wide band gap materials like AlGaN/GaN are preferred in the channel interface to achieve the high mobilty of the carriers. This happens due to its distinctive characteristics due to wide band gap, which yields high breakdown field with high drain current [9-11]. The high electron mobility transistor device commonly used for RF applications likewise in radar, cellular telecommunication, radio astronomy and the satellite broadcasting. These applications employ the low noise with high frequency and high critical electric field [12-14]. The high electron mobility transistor exhibits the three times higher power density than MOSFET which over all reduces the chip area in terms of their output performance. One of the special characteristics of the high electron mobility transistor is the formation of the two-dimensional electron gas molecule where the carrier mobility is extremely high [15-16]. The important feature of AlGaN/GaN based high electron mobility transistor structure is basically the formation of electrons confinement at the interface to from two dimensional electron gas (2DEG). The conventional AlGaN/GaN hetero-structure suffers from high R_{ON} which owns the 2DEG density in gate-source and gate-drain region, however low R_{ON} can be achieved by polarization-induced high density and 2DEG mobility at the interface. Many other optimal approaches used for lowering the R_{ON}, like 2-DEG depletion can be attained by using a thin AlGaN barrier layer with low Aluminum concentration [17]. The 2DEG cannot be easily- depleted at zero bias in schottky gate contact [18-19] but due to the band-gap, the critical field strength is inversely proportion to the drift region thickness and hence, the ON-state resistance is lower [20].

In this paper, the response of the Gallium nitride (GaN) on Silicon sunbstrate high electron mobility transistor is desined and being analyzed for the high voltage, high switching power for regulation of RF application at high temperature. The operation is associated with efficiently power switching in which the OFF-state voltage is highly blocked with minimum leakage current and ON state resistance. In order to operate at high voltage, these devices can be limited by the chain factor like subthreshold voltage and device scaling. However, the blocking voltage improvement is a complex problem which can be resolved by, epitaxial design, device structure and its scaling with favorable fabrication technology.

II. DEVICE STRUCTURE AND SIMULATION FRAMEWORK

In high electron mobility transistor, the presence of a conduction band offset at the interface of two different bandgap materials produces two-dimensional electron gas (2DEG). The potential well is formed on the material side of the lower bandgap. Over the GaN side of the device, 2DEG is generated when higher bandgap material (AlGaN) develops on lower bandgap material (GaN). Due to ease of growth in the of GaN over silicon substrate with low cost and large size will make its choice better over the SiC and other material. Additionally, in heterostructure, GaN employed with polarization field in which two different layers of different bandgap are come together for

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single growth. However, this will create a difference in electric field and surface potential at heterojunction. Figure 1 show the schematic structure of AlGaN/GaN in which AlGaN is common in between source and drain electrodes. The doped high electron mobility transistor structure with AlGaN doped layer will help in improving the polarization across the layer. This enhances the transport characteristics by imprisonment of electron within the channel.

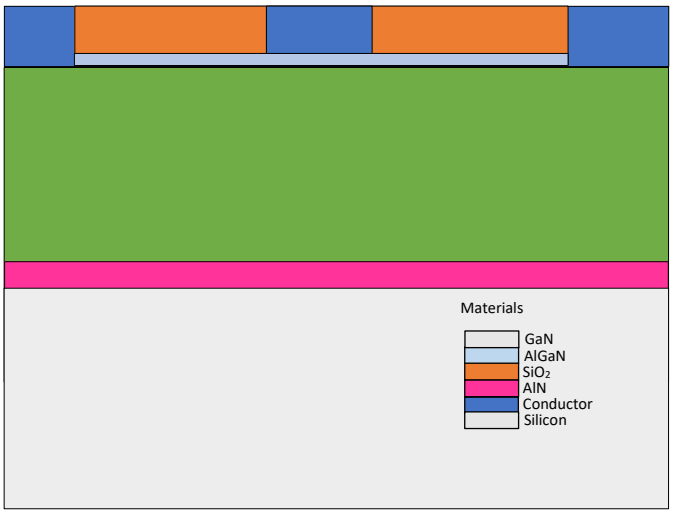


Fig. 1. Schematic diagram of GaN on Silicon substarte high electron mobility transistor (high electron mobility transistor) TCAD tool structure

If the induced charge is positive, electrons will tend to compensate the induced charge resulting in the formation of the channel. The channel electrons in the high electron mobility transistor are referred to as a Two-Dimensional Electron Gas because they are trapped in a quantum well in a very restricted spatial region at the hetero-interface (2DEG) [22]. The equivalent device design parameters of high electron mobility transistor used during simulation work are shown in Table I.

Table I: Device specification of the proposed device AlGaN/GaN based high electron mobility transistor.

Parameter Used	Length	Width
Device	6 µm	3 µm
Channel	3 µm	0.03 µm
AlN 2DEG	6 µm	0.05 µm
Electrode Gate	1 µm	0.05 µm
Electrode Drain	1 µm	0.035 µm
Electrode Source	1 µm	0.035 µm
Silicon Substrate	400 µm	0.095 µm

The simulation of the device is excuted using Silvaco-ATLAS tool [21]. Drift-deffusion model which is based on the Boltzmann's transport theory along with two advance transport models namely hydrodynamic transport model and energy balance transport model are considered while simulation to sustain the carrier temperature instead of the local electric field. Moreover, polarization model of GaN, fermi-dirac model, SRH model, low and high electric field models, and Selberherr's impact ionization model are included during the simualtiing the device structure. A detailed analysis of the proposed device of AlGaN/GaN high electron mobility transistor is given with the structure dimensions. More attention towards thermal conduction and Schottky-gate reverse bias tunneling are carried out. The affecting parameters like doping concentration, channel length, gate work-function, trans-conductance and capacitance characteristics are observed by varying V_{GS}.

A. Polarization Effect

AlGaN/GaN have special characteristics which holds the two-dimensional electron gas without doping process. This happens due to piezoelectric properties and spontaneous polarization which is found in crystal structure of III-nitrides and can be represent by Figure 2. The high tendency of atom to attract an electron bonding which is of tetrahedrally structure between III-nitrides elements, results in spontaneous polarization [23-24]. In the crystal structure, the epitaxial GaN layer was grown at normal to (0001) position. Due to lack of inversion symmetry, it will result in spontaneous polarization in <0001> direction.

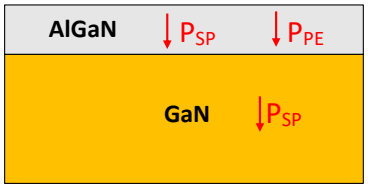


Fig. 2. Schematic diagram representing the spontaneous effect with piezoelectric polarization of AlGaN/GaN high electron mobility transfer (high electron mobility transistor) TCAD tool structure.

In comparison to GaN, the AlGaN is very thin in AlGaN/GaN in high electron mobility transistor structure, this is done due to lattice mismatch which need to be equal and constant. The piezoelectric polarization of the interface field can be expressed as:

$$P_{PE} = 2\varepsilon_a\left(e_{31} - \frac{e_{33}c_{13}}{c_{33}}\right) \qquad (1)$$

The above equation is directly proportional to lattice constant(ε_a) and piezoelectric coefficient of AlGaN/GaN in high electron mobility transistor structure. The average polarization effect caused by AlGaN/GaN, where GaN consist negative polarization field and AlGaN consist of positive spontaneous and piezoelectric polarization effect (P_{SP}) [25-26]. Since the spontaneous polarization (P_{PE}) is greater in comparison to the GaN, at the AlGaN/GaN interface charges.

$$\sigma = \left(P_{SP,AlGaN} + P_{PE,AlGaN}\right) - P_{SP,GaN} \qquad (2)$$

Both the equation (1) & (2), will conclude as a fixed permanent creation of a 2DEG polarization.

B. Parasitic Effects

The parasitic effects are also known as trapping effects, as the trap charges (electron and holes) are lie between the channel and the gate contact. The effect induces due to generation of available energy levels in energy bandgap of semiconductor, which are generally related to the lattice mismatched of different materials connected to each other [27]. In the ON condition of the device, it limits the active charges with respect

to time and stress, which futher causes an effect to the static and dynamic performance of the device. In order to eliminates these trap charges, we need to apply operative electric field. This collision of trap and non-trap charge will make device performance degrading [28] .The two main parasitics effects are kink and current collapse effect. The kink effect are more effective at low drain voltage at degrade the ON drain current performace. However, this can be overcome by the increasing the voltage V_{ds} (drain-source voltage), resulting the pinch off voltage to be shifted towards more negative voltages and which implusively raise the drain current. The disturbed DC current will effect on ON resistance (R_{on}) and transconductance (g_m). The upper trap charges of bandgap are acceptor and lower trap charges are donor. The position of the trap charges will play a vital role in the device performance. They are filled with the narrow AlGaN layer, in order to kept the trap charges level below the Fermi level. Due to narrow barrier, the charges will trap and pused hardly by the strong polarization effect of AlGaN. The emmison rate relation will the V_D can be exterated by using three given three equations (3), (4)and (5). Initally consider the emission rate to be calculated by Arrhenius equation at random temperature [29].

$$e = AT^2 exp\left(-\frac{E_F}{kT}\right) \quad (3)$$

Where T, k and E_F are temperature, Boltzmann constant and Fermi energy level. The barrier (β) decreases due to high electric field with respect to square root of applied electric field given by equation (4).

$$\Delta\eta\phi_{PF} = \left(\frac{q^3}{\pi}\right)^{1/2} \sqrt{F} = \beta\sqrt{F} \quad (4)$$

Here, q is a electron charges and ε represent the dielectric constant. The ionization energy of the field can be represented by:

$$E_i(F) = E_i(0) - \beta\sqrt{F} \quad (5)$$

The ΔE_C is energy band gap difference between AlGaN and GaN, where at interface of AlGaN and GaN, $E_i(F)$ is difference conduction band and fermi level. The current collapse near drain region occur near the surface of AlGaN layer resulting the channel depletion.

Fig. 3 is given below to understand energy band diagram of the high electron mobility transistor, there is given three different regions of Metal, AlGaN and GaN. Quantum tunneling valley happens in conduction band, basically the reason behind that being the tunneling of electrons present in two-dimensional electron gas layer.

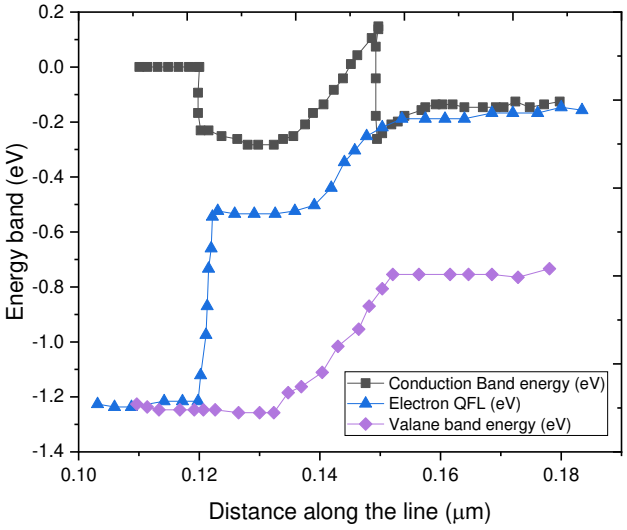


Fig.3. ON state Energy Band diagram of the AlGaN/GaN based high electron mobility transistor

According to energy band diagram observations there is almost same energy required in both the cases to move one electron from valance band to conduction band. So finally proposed device structure and ON state band diagram of the high electron mobility transistor has been drawn in above part and analysis has been done behind them.The conduction path was created by joining layer of AlGaN/GaN in high electron mobility transistor structure causes positive net charges, which pull the conduction band towards downwards. The positive change density is now attracted by electrons and trap at potential well at triangular shaped. Moreover, the polarization shifted net negative charges which now dragged the conduction band upwards. The confined electron will create 2-DEG at the GaN channel junction. The expression for 2DEG at the GaN channel can be described as:

$$n_s = \left(\frac{\sigma_{int}}{q}\right) - \left(\frac{\varepsilon_0\varepsilon_r}{q^2 t_{AlGaN}}\right)(q\varphi_b + E_F + \Delta E_C) \quad (6)$$

Where, q is the electron change, σ is the AlGaN/GaN sheet charges at the interface, E_F is the fermi energy level, φ_b is the gate contact Schottky barrier height which can change the threshold voltage of the device. ΔE_C represent the energy bandgap between AlGaN and GaN, where dielectric constant effects the breakdown field strength. Due to different value energy band gap of AlGaN and GaN, lattice mismatches occur which can be compensate by its thickness. Table II represent different properties of high electron mobility transistor structure which are arose by hetero structures, which generates a potential well for electron as a channel for easy movement of electron and forms 2DEG.

Table II: Different properties of high electron mobility transistor material

Material Properties	Si	GaAs	GaN	AlN	InN	SiC
Energy bandgap (eV)	1.12	1.42	3.4	6.2	0.9	3.26
Dielectric Constant (ε_r)	11.8	13.1	8.9	8.5	15.3	-
Breakdown Field (Mv/cm)	0.3	0.4	3.0	11	low	3
Velocity (cm/s)	1×10^7	2×10^7	2×10^7	-	2×10^8	-
Electron Mobility (cm^2/Vs)	1350	8500	440	300	250	720
Lattice constant (Å)	5.43	5.65	3.19	3.1	3.53	3.0
Thermal conductivity (W/cm k)	1.5	0.5	1.3	-	-	4.9

III. RESULTS AND DISCUSSION

In order to describe the parameter variation effects on the characteristics of an AlGaN–GaN high electron mobility transistor, the most important characteristics are discussed below, and with the help of these characteristics we analyze the fundamental concepts behind them.

A. *Impacts on I_d-V_{GS} Characteristics*

Fig.4 shows the DC I-V characteristics of an AlGaN/GaN high electron mobility transistor on Al_2O_3 substrate at various doping levels. The drain current is plotted with the gate gate voltages at the drain source voltage of 2V. It is seen that at low level doping i.e. from 10^{10} /cm^3 to 10^{12} /cm^3 the drain current remain constant and it start increasing when doping level rises from 10^{13}/cm^3. At the doping level of 10^{15}/cm^3 maximum drain current I_d= 22mA is achieved.

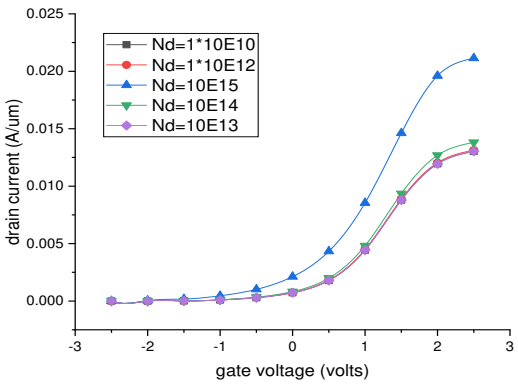


Figure 4 Id-Vgs characteristics for various doping concentration

The impact of gate work fuction (wf) on the drain current is plotted on the Fig.5. This graph is plotted keeping the constant doping level of 10^{15}/cm^3 and at the Vds=2V. It can be noticed that on increasing the gate work function from 4 eV to 4.5 eV initially the drain current increses by 2 orders but on futher increasing the work function the drain current starts decreasing. So, the maximum drain current is observed at gate work function of 4.5 eV.

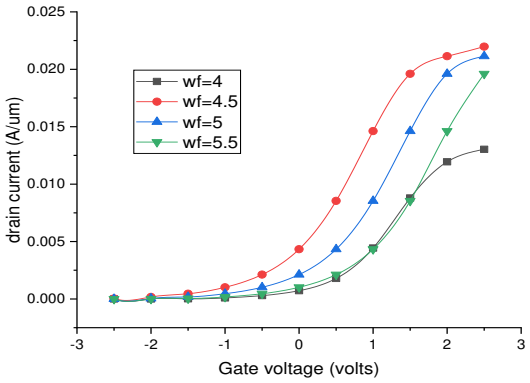


Figure 5 Id-Vgs characteristics for various gate work functions

According to the above characteristics, the threshold voltage is directly proportional to the doping of the device. Threshold voltage expression is given below.

$$V_{TH} = V_{FB} + 2\varphi_F + \gamma\sqrt{\varphi_F} \tag{7}$$

$$\gamma = \frac{\sqrt{2q\varepsilon N}}{C_{ox}} \tag{8}$$

Now third observation has been taken that is impacts of work-function on I-V characteristics. Threshold voltage is again directly proportional to work-function of metal so the characteristics show slightly high threshold voltage compared to previous results.

$$V_{th} = Ideal\ threshold\ volt. + V_{FB} \tag{9}$$

Where, V_{FB} is the flat band voltage.

$$V_{FB} = \phi_{ms} - \frac{Q_{fc}}{C_{ox}} \tag{10}$$

The variation of the drain current with different channel length are plotted in Fig. 6 and Fig. 7 at high bulk doping and low bulk dping respectively. The simulation is carried out at the gate wok function of 4. eV and Vds= 2V. It is noticed that at the high doping level the drain current decreases on increasing the channel length while at the low doping level the variation is less as compare to the high doping level. Threshold voltage is very small compared to the previous one because the charge in the oxide increases, that is mentioned in above equations (9) & (10). It is also observed that the drain current at the low level doping is 78% lower than the drain current at high doping level.

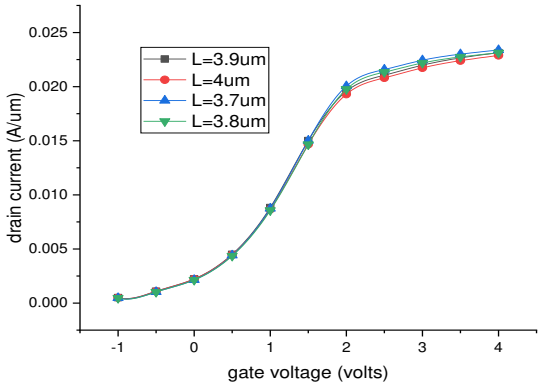


Figure 6 Id-Vgs characteristics for various channel length at high doping concentration

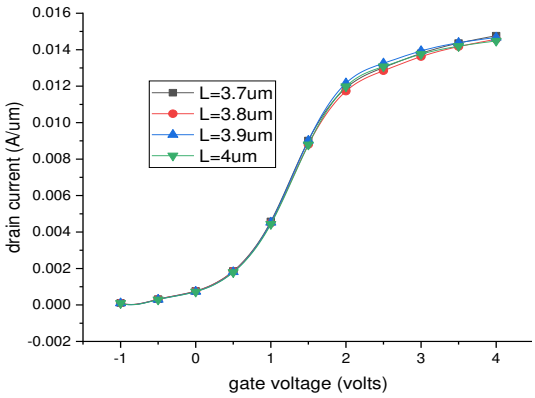


Figure 7 Id-Vgs characteristics for various channel length at low doping concentration

B. Impacts on g_m-V_{GS} Characteristics

The trans-conductance is defined as change in drain current with respect to gate to source voltage at constant V_{ds}.

$$gm = \frac{\partial I_D}{\partial V_{GS}} \tag{11}$$

Fig.8 shows the characteristics of g_m vs. V_{gs} at the different doping concentarion of the bulk. Transconductance shows maximum at value V_{gs}=1.5V and at the doping level of $1x10^{16}/cm^3$. Initially the the transconductnce increses with increase in the doping but eventually it start decreasing when the doing level reaches to $1x10^{18}/cm^3$.

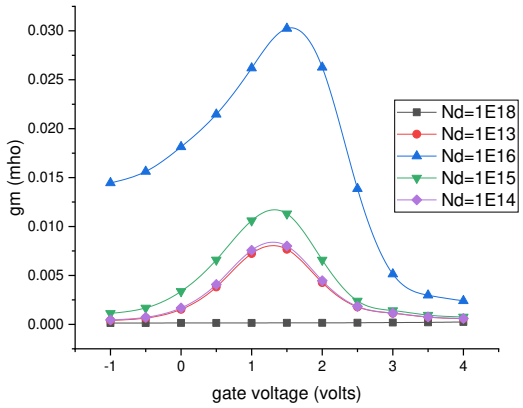


Figure 8 g_m vs Gate voltage characteristics at different doping level

For RF applications g_m should be maximum because the cutoff frequency of the device should be large and g_m is directly proportional to f_T. Now the trans-conductance depends upon various parameters so the mathematical equation of the trans-conductance is given below-

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th}) \tag{12}$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{13}$$

Comparison between two g_m characteristics clearly shows the effect of doping concentration on the trans-conductance and it is observed that trans-conductance is inversely proportional to the doping concentration. We have observed that impact ionization increases with the decrease in the doping concentration and vice versa.

The effect of metal gate work function on the transconductance is plotted in Fig. 9. Which shows g_m is maximum at V_{gs} = 1V for the work function of 4.5eV. the maximum value of the g_m is obtained as 11 m mho. Equation (12) already mentions that g_m is linear and inversely dependent on threshold voltage so it is ultimately inversely dependent on gate work-function.

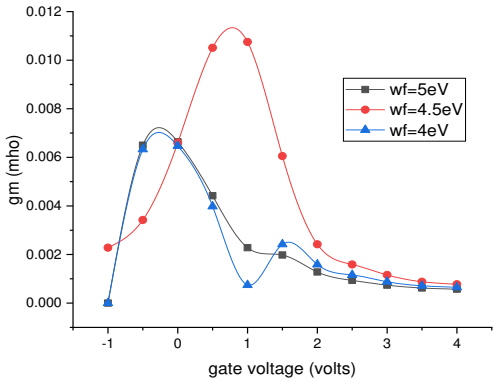


Figure 9. gm vs Gate voltage at different gate material work-function

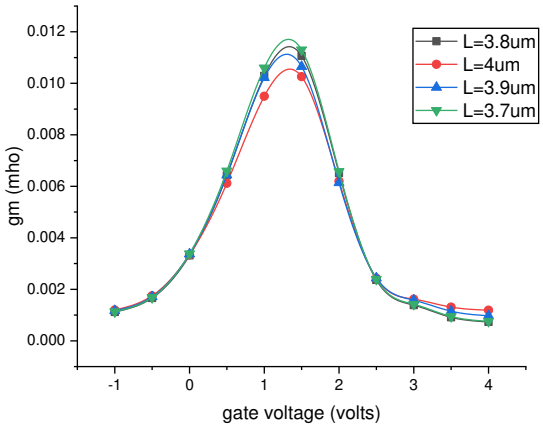
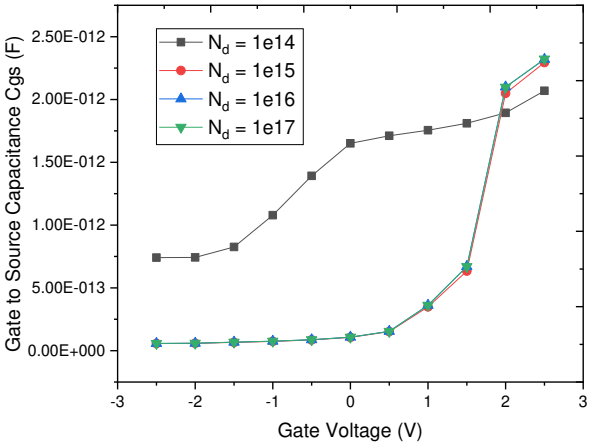


Figure 10. g_m-V_{gs} characteristics for various channel length

The variation of the transconductance with the channel length is plotted in Fig. 10. It is seen that on increasing the channel length the transconductance decreases because the drain current reduces with the increase in the channel length. If the channel length increases the drain current decreases because the number of electrons or electron density decreases so if the drain current gives approximate linear characteristic then the trans-conductance will be constant or saturate according to equation (11).

C. Impacts on Gate Capacitance

For RF applications, the gate capacitances; gate to source capacitance Cgs and gate to drain capacitance Cgd plays a major role while determining the device performance. gate voltage versus gate capacitance Cgs and Cgd characteristics are shown in Figure 11(a) and Fig. 11 (b) respectively at different doping variations. It is seen that initially there is little variation on the Cgs and Cgd with the doping but on further increasing the doping level in th bulk both source and drain capacitance increases since the number of chrge carrier increases. At the higher gate voltage its value varies in the range of 1.5 pF to 2 pF.



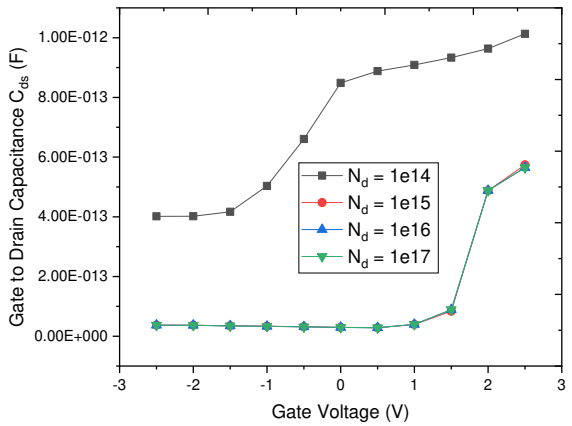
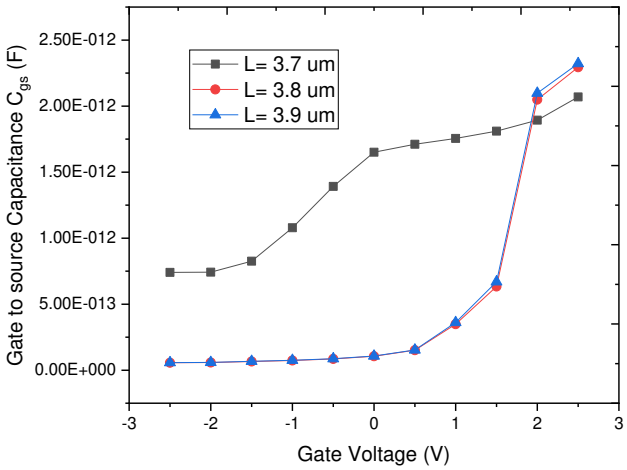


Figure 11 (a)C_{gs}-V_{gs}, and (b) Cgd-Vgs Characteristics for various doping levels

Fig. 12 shows the variation of gate capacitance with the applied gate bias for different channel lengths. Fig. 12(a) is drawn for gate to source capacitance while Fig. 12 (b) is drawn for gate to drain capacitance. It is noticed that on increasing the channel length both capacitances Cgs and Cgd increase with the gate voltage. The obtaine values of the gate capacitance lies in the range of 0.2 pF to 0.8 pF.



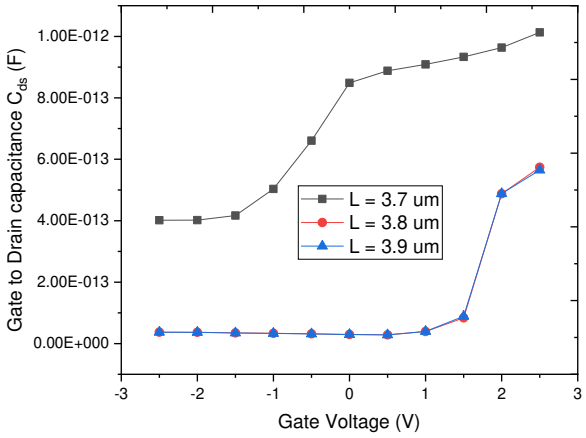
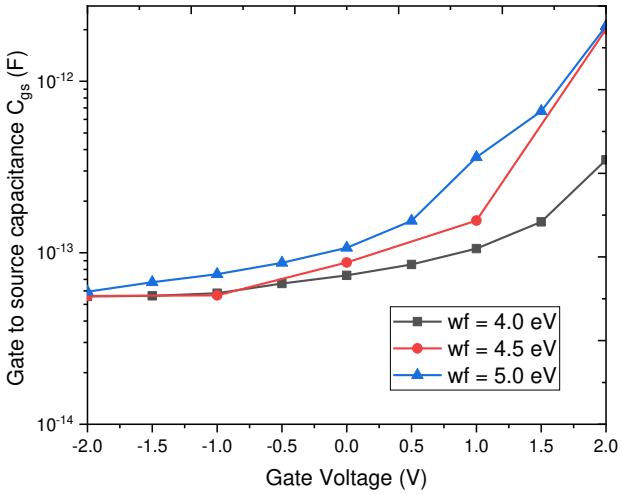


Fig. 12 Variation of (a) gate to source capciatnce Cgs and (b) gate to drain capacitance Cgd for different channel length

The impct of work function on the variation of the gate to source capciatnce Cgs and gate to drain capacitance Cgd is plotted in the Fig 13 (a) and Fig. 13 (b) respectively. It is observed that the both capaciatnces increase when the metal work function rises and their values lie in the range of 0.2 pF to 1 pF.



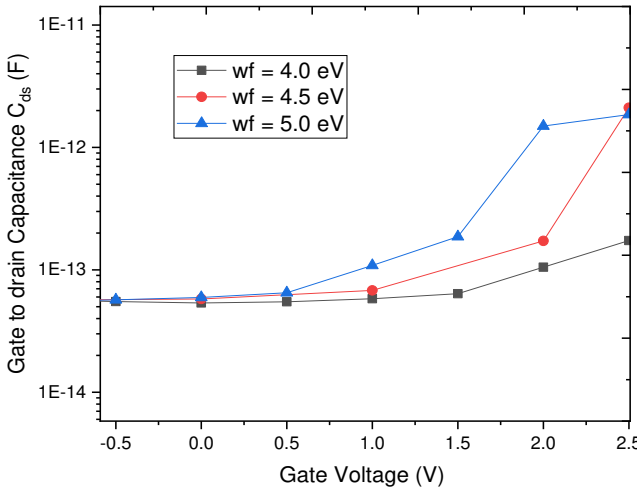


Fig. 13 Variation of (a) gate to source capciatnce Cgs and (b) gate to drain capacitance Cgd for different metal gate work function

The cut-off frequency expression is given as-

$$f_T = \frac{g_m}{2\pi C_g} \tag{14}$$

The gain falls at high frequency and low frequency so there is a frequency range where the gain of the device is maximum. According to equation (14) the cut-off frequency depends on two parameters so g_m is directly proportional and overall gate capacitance is inversely proportional to cut-off frequency.

Therefore, C_g should be less and g_m should be high to acquire high cut-off frequency range. If we observe the characteristic, then doping plays a major role in capacitance so in one hand, the doping of device should be less but for good conduction and for high gain the doping is required.

IV. Conclusion

This paper presents design and comparative performance analysis of the high electron mobility transistor on silicon substrate for RF applications. The variation in the performance parameters drain current, transconductance, and total gate capacinatce is analyzed by varying the various design parameters like doping level, channel length and work-function of gate material. In the proposed device a good performance with maximum g_m = 13 milli-mho, minimum gate capacitance C_g=0.5pf is achieved. V_{th} is varied between -0.25V to 0.25V at various status of device parameters. One characteristic is basic device parameter and other two RF characteristics are investigated.

Data Availability: Not applicable.

Author contributions:
All authors have equally participated in the preparing of the manuscript during implementation of ideas, findings results, and writing of the manuscript.

Declarations

Funding statement: The author(s) received no financial support for the research, authorship, and/or publication of this article.

Availability of data and material: Not applicable

Compliance with ethical standards: all procedures performed in studies involving human participants were in accordance with the ethical standards.

Consent to participate: Not applicable

Consent for Publication: The Author transfers his copyrights to the publisher.

Conflict of Interest: The authors declare that there are no conflicts of interest.

Acknowledgement: Not Applicable

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