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Neeraj Jain (✉ neerajengi24@gmail.com)

Manipal University <https://orcid.org/0000-0002-4544-1120>

Kunal Singh

National Institute of Technology

Shashi Kant Sharma

Indian Institute of Information Technology Ranchi

Renu Kumawat

Manipal University

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Analog/RF Performance Analysis of a-ITZO Thin Film Transistor

Neeraj Jain^{1,2}, Kunal Singh³, Shashi Kant Sharma⁴, and Renu Kumawat¹

¹ Department of Electronics and Communication Engineering, Manipal University, Jaipur, Rajasthan - 303007, India

² Department of Electronics and Communication Engineering, Swami Keshvanand Institute of Technology, Management and Gramothan, Jaipur, Rajasthan - 302017, India

³ Department of Electronics and Communication Engineering, National Institute of Technology, Jamshedpur, Jharkhand - 831014, India

⁴ Department of Electronics and Communication Engineering, Indian Institute of Information Technology Ranchi, Jharkhand - 831014, India

E-mail: neerajengi24@gmail.com

Abstract

This work reports RF and analog performance analysis of an amorphous Indium Tin Zinc Oxide thin film transistor. The various parameters affecting the performance of a-ITZO TFT like drain current, drain conductance, output resistance, transconductance, transconductance generation factor, early voltage, intrinsic gain, capacitances, cut off frequency, maximum frequency of oscillation, transconductance frequency product, gain frequency product, gain bandwidth product and gain transconductance frequency product have been closely examined. The device is further analyzed to investigate the impact of variation in physical parameters viz. dielectric material, dielectric thickness (D_t) and temperature (T) on the RF/Analog performance. Use of high- k dielectric material in the simulated structure has resulted in low subthreshold slope (SS) of 0.62 V/decade, On voltage (V_{on}) of (-0.29) V, I_{on}/I_{off} ratio of $\sim 10^9$, intrinsic gain (A_V) of 104.5 dB and gain frequency product (GFP) of 1.86 GHz. The best results for dielectric thickness variation are offered for dielectric thickness of 150 nm with SS of 0.22 V/decade, V_{on} of (-0.26 V), I_{on}/I_{off} of $\sim 10^{10}$, (A_V) of 175.69 dB and GFP of 2.39 GHz. For device reliability and stability study, temperature analysis has also been done. To demonstrate the circuit level implementation of the simulated structure, a resistive load inverter circuit is simulated and analyzed for different variations (high- k , D_t and T). The results obtained are promising to meet the current display industry requirement. It has also been concluded that TFT with high- k material or thinner dielectric at T=300 K provides best performance.

Keywords Analog, RF, Thin Film Transistor, TCAD.

1 Introduction – In recent years, thin film transistors have drawn a significant attention of researchers as it has become the backbone of thin film electronics industry. A CAGR of 17.34% is expected to register for TFT market during 2021-2026 [1]. TFT is used as a pixel switching element in LED or flat panel displays [2]. The major outlook of display industry is to produce large area and high-resolution displays. Therefore, there is an immediate need to improve the performance of TFTs. TFT is a special type of transistor which has a supporting substrate over which a layer of dielectric, semiconductor and contacts are deposited [3]. The material used as channel layer are A-Si, Poly Si, Semiconducting Metal Oxides (SMO's) etc. Use of A-Si and Poly-Si for large and high-resolution display is now becoming unacceptable because of its low mobility, high processing temperature and inferior electrical properties [4]. Considering these limitations,

semiconductor oxide materials like ZnO [5], SnO₂ [6], GaZnO [7], IGZO [8] etc. are seen as a replacement to A-Si and Poly-Si. Among all semiconductor oxide materials, ZnO has drawn a significant attention of researchers because of its large band gap, low cost, good transparency, appreciable mobility, abundance in nature and high excitation energy [9]. However, Chung *et al.* [10] reported that ZnO has many grain boundaries which limit its use in large and high-resolution displays. This obstacle was resolved by doping ZnO with metals like In [11], Al [12], Tin [13], Mg [14] etc. to make amorphous oxide semiconductors (AOS) with no grain boundaries. As reported by Lee *et al.* [15], IGZO as AOS in channel layer of TFT provides high electric mobility as well as high optical transmittance. Nomura *et al.* [16] reported first IGZO TFT at room temperature and suggested that IGZO can be used as a potential material for future

electronic devices. Yabuta *et al.* [17] grown IGZO as channel material for TFT with mobility (μ_{fe}) of the order of ~ 10 and I_{on}/I_{off} ratio of the order of $\sim 10^8$. However, this high mobility and stability is still not sufficient for next generation displays which require μ_{fe} of the order of ~ 20 . Arai *et al.* [18] proposed a-ITZO as an alternative of IGZO with high μ_{fe} (~ 25) and good stability. Grover *et al.* [19] reported that ZITO is a potential TFT channel material as it offers high mobility of $5\text{-}19\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, turn on voltage in range of -4 to -17 V and I_{on}/I_{off} of $> 10^6$. Based upon the past literature, it can be concluded that a-ITZO has all potential properties that makes it a potential material for TFTs.

To investigate the applicability of a-ITZO as channel layer in TFTs, a simulation study using ATLAS tool [20] from Silvaco TCAD have been reported in this work. To demonstrate the use of a-ITZO TFT in Analog/RF application, different RF/Analog parameters have been studied. To the best of our knowledge, this kind of investigations have not been reported in literature for TFTs. Furthermore, it has also been seen that high density analog and RF application are facing challenges in the attainment of higher device performance like low power and high frequency of operation. Different methods like scaling the geometric dimensions, material changes and temperature variability [21-25] can effectively make the TFTs to work at low voltages with decreased subthreshold swing. To achieve current device requirements, scaling the dimension of TFT is seen as a potential method by many researchers. Scaling also scales the dielectric thickness. Kumar *et al.* [26] reported that downscaling has improved electrical parameters like I_{on}/I_{off} , μ_{fe} , SS but at the cost of increasing tunneling gate leakage current. To cop up with this, Vyas *et al.* [27] suggested that high- k dielectric material like Al_2O_3 , HfO_2 etc. can improve the electrical performance of TFTs. High- k material is physically thick without being electrically thicker, leading to the same effect of scaling SiO_2 without increasing the leakage current. Many TFT applications like active-matrix liquid-crystal display (AMLCD), active-matrix organic light-emitting diode (AMOLED), bio medical devices etc. also require temperature analysis as it tells the working temperature range of the device. Considering all the above aspects, a 2D simulation of a-ITZO TFT along with its RF and analog analysis is thoroughly done by varying different physical parameters. It is seen that a-ITZO material based TFT is a promising option for future RF and analog devices.

The organization of the work is as follows: Section 2 deals with the TFT simulation approach including dimensions, materials and their properties. Section 3 deals with the simulation result, analysis and discussion about impact of different dielectric material, dielectric materials thickness (D_t) and temperature (T) on DC, Analog and RF parameters. The application of a-ITZO TFT as resistive load inverter is discussed in section 4.

2 TFT SIMULATION APPROACH

Fig. 1 shows Bottom Gate Top Contact (BGTC) TFT. Device material parameter used for simulation are tabulated in Table I [20, 28, 29, 30]. The TCAD simulation have been done using ATLAS simulator on 2D grid. Newton method is employed to do the calculations. For carrier transport, drift diffusion and energy balance models have been considered. Fermi Dirac model are used for carrier distribution. The TFT uses disordered semiconductors which has defect states that can trap the charges so, the models that define defect density are also included. To verify the simulation results, the simulation parameters are calibrated with the results available for TFT [31] and obtained in Fig. 2. It can be deduced that TCAD simulation results are in excellent agreement with the results obtained by taouririt *et al* [31]. Further, Analog/ RF analysis of a-ITZO TFT by introducing different physical variations have been discussed.

3 RF/ Analog Analysis of a-ITZO TFT

This section deals with the calculation and analysis of Analog/RF performance parameters for a-ITZO TFT using the expressions mentioned in Table II. The primary Figure of Merits (FOM's) i.e. drain current (I_{DS}), g_d , R_O , g_m , TGF, V_{EA} , A_V , gate to source (C_{GS}) and gate to drain (C_{GD}) capacitances, f_T , F_{max} , TFP, GFP, GBP and GTFP and the impact of physical parameter i.e. dielectric material, dielectric thickness (D_t) and temperature (T) of a-ITZO TFT on Analog/RF performance is analyzed in the below subsections.

3.1 Impact of High K Dielectric Material on the DC, Analog and RF Parameters:

In last few decades, SiO_2 was mainly used as dielectric material and the devices based on it have shown good electrical performance. As the technology is changing, there is a need of miniaturized devices to fulfill the requirement of future thin film electronic market.

As the device dimensions are scaled, dielectric layer thickness is also scaled, which has a positive

impact on device performance. The dielectric thickness (D_t)

Fig. 1 Structure of the 2D cross sectional a-ITZO TFT

Table I: Material and Density of State (DOS) parameter of a-ITZO

Domain	Parameter	Value (Unit)
a-ITZO Parameters	Band Gap	3.02 eV
	Dielectric Constant	10
	Affinity	4.65 eV
	Electron mobility	$0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$
	Hole mobility	$30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$
	Effective density of states in the conduction band, N_C	$1.59 \times 10^{19} \text{ cm}^{-3}$
	Effective density of states in the valence band, N_V	$1.21 \times 10^{19} \text{ cm}^{-3}$
	Carrier concentration (N)	$4.62 \times 10^{15} \text{ cm}^{-3}$
	Thickness (Tch)	20 nm
Dielectric Parameters	Band Gap, SiO_2	9 eV
	Permittivity, SiO_2	3.9
	Band Gap, Si_3N_4	5 eV
	Permittivity, Si_3N_4	7.5
	Band Gap, Al_2O_3	8.7 eV
	Permittivity, Al_2O_3	9.5
	Band Gap, HfO_2	5.7 eV
	Permittivity, HfO_2	35
a-ITZO, Density of Defects Parameters	Thickness (Dt)	variable (nm) (150,200,250,300)
	Peak density of acceptor-like states, N_{TA}	$1.22 \times 10^{18} \text{ cm}^{-3} \text{ eV}^{-1}$
	Peak density of donor-like states, N_{TD}	$1.30 \times 10^{20} \text{ cm}^{-3} \text{ eV}^{-1}$
	Characteristic decay energy (acceptor-like states), W_{TA}	0.016 eV
	Characteristic decay energy (donor-like states), W_{TD}	0.20 eV
	Peak density (shallow donor Gaussian), N_{GD}	$1.73 \times 10^{16} \text{ cm}^{-3} \text{ eV}^{-1}$
	Decay energy (shallow donor Gaussian), W_{GD}	0.082 eV
	Energy peak (shallow donor Gaussian) E_{GD}	2.9 eV
Source/ Drain/ Gate Parameters	Gate (Molybdenum) Length (L_g)/Width (W) /Tcont	$35 \mu\text{m} / 10 \mu\text{m} / 0.1 \text{ nm}$
	Molybdenum Source and Drain (L_s & L_d /W/Tcont)	$15 \mu\text{m} / 10 \mu\text{m} / 0.1 \text{ nm}$
	Work Function of Molybdenum (Φ_s)	4.53 eV

Fig. 2 Comparison of the transfer characteristics of TFT results reported in [31] and a-ITZO TFT (TCAD simulation) for Drain-to-Source Voltage $V_{DS}=5V$.

Table II: Symbols and expressions [32,33]

Symbol	Quantity	Unit	Expression
g_d	Drain Conductance	S	$g_d = \frac{dI_{DS}}{dV_{DS}} \mid V_{GS} = \text{Const.}$
R_O	Output Resistance	Ω	$R_O = \frac{1}{g_d}$
V_{EA}	Early Voltage	V	$V_{EA} = \frac{I_{DS}}{g_d}$
A_V	Intrinsic Gain	dB	$A_V = \frac{g_m}{g_d}$
g_m	Transconductance	S	$g_m = \frac{dI_{DS}}{dV_{GS}} \mid V_{DS} = \text{Const.}$
TGF	Transconductance Generation Factor	V^{-1}	$TGF = \frac{I_{DS}}{g_m}$
f_T	Cut-off Frequency	Hz	$f_T = \frac{g_m}{2\pi[(C_{GS}+C_{GD})]}$
GBP	Gain Bandwidth Product	Hz	$GBP = \frac{g_m}{20\pi C_{GD}}$
F_{max}	Maximum frequency of operation	Hz	$F_{max} = \sqrt{\frac{f_T}{8\pi R_G C_{GD}}}$, Where, $(R_G = \frac{1}{g_{gg}})$
TFP	Transconductance Frequency Product	Hz	$TFP = (\frac{g_m}{I_{DS}}) * f_T$
GFP	Gain Frequency Product	Hz	$GFP = (\frac{g_m}{g_d}) * f_T$
GTFP	Gain Transconductance Frequency Product	Hz	$GTFP = (\frac{g_m}{g_d}) * TFP$

scaling also increases (Eq.1) capacitance per unit area (C_{ox}) that directly increases the drain current of the device [23].

$$C_{ox} = \frac{\epsilon_0 \cdot k_{ox} \cdot L \cdot W}{T_{ox}} \quad (1)$$

Where L, W, T_{ox} are the length, width and thickness of dielectric, k_{ox} is the dielectric constant and ϵ_0 is the absolute permittivity.

To solve the thickness scaling problem, high- k dielectric material instead of low- k dielectric have been used. High- k dielectric material is recognized by Effective Oxide Thickness (EOT) which means that it is electrically thick without being physically thick which results in increased capacitances and reduced leakage current [31]. In this section, the impact of high- k material (SiO_2 , Si_3N_4 , Al_2O_3 and HfO_2) on DC, analog and RF performance of a-ITZO TFT have been studied where dielectric thickness (D_t) was considered as 200 nm during the simulation.

The plot of different analog/RF parameters with variation in dielectric material is shown in Fig. 3. Fig Table III Extracted parameters: V_t , V_{on} , SS , I_{on} , I_{off} depending on dielectric material variation

Dielectric	V_t (V)	V_{on} (V)	Sub-Threshold Swing (V/decade)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}
SiO ₂	1.75	-0.70	1.0775	9.387×10^{-5}	2.36×10^{-12}	3.97×10^7
Si ₃ N ₄	1.97	-0.50	0.8492	1.790×10^{-4}	1.75×10^{-12}	1.01×10^8
Al ₂ O ₃	2.03	-0.46	0.7945	2.262×10^{-4}	4.07×10^{-13}	5.55×10^8
HfO ₂	2.19	-0.29	0.6216	8.232×10^{-4}	4.11×10^{-13}	1.99×10^9

Fig. 3 (a) I_{DS} (Linear and Log) (b) g_d & Output I_{DS} (c) R_O (Inset), V_{EA} and A_V (d) g_m & TGF for different dielectric materials.

and TGF for different high- k materials. Drain current (I_{DS}) in linear and log scale w.r.t. V_{GS} is shown in Fig. 3 (a). The peak value of I_{DS} increases from 95 μ A to 825 μ A when the dielectric material changed from HfO₂ to SiO₂. The electrical parameters are extracted from this curve and tabulated in Table III. It is seen

3 (a-d) shows the variation of I_{DS} , g_d , R_O , V_{EA} , A_V , g_m

from Table III that I_{on} and I_{on}/I_{off} are mostly affected with this change. Also, there is an increased shift in threshold voltage (V_{th}) because of the reduction of surface material potential along the channel [34]. Fig.3(b) demonstrates the output characteristics and drain conduction (g_d) for a-ITZO

TFT for different dielectric material at $V_{GS} = 5$ V. The right axis (Fig. 3(b)) depicts the output characteristics and it is seen that when $V_{DS} > 5$ V, the drain current

starts to saturate for all the dielectric materials, however it has higher

(a)

(b)

(c)

(d)

Fig. 4 (a) C_{GS} & C_{GD} (b) f_T & GBP (Inset) (c) F_{max} & GTFP (inset) (d) TFP & GFP for different dielectric materials.

value for HfO₂ based TFT. The reason for this change is increased capacitance per unit area because of decreased effective thickness (Eq.1). The Drain conductance (g_d) is derived from output characteristics and is plotted on left axis of Fig. 3(b). The same rise is seen in g_d as that of I_{DS} for HfO₂ based TFT. The inverse of g_d is known as output resistance (R_o). The inset of Fig. 3(c) shows the variation of R_o with V_{DS} for various dielectric materials. It is found that TFT with HfO₂ dielectric has low R_o of 2.95 M Ω as compared to SiO₂ based TFT having R_o of 16.86 M Ω . As a result of this, HfO₂ based TFT shows superior I_{DS} values than SiO₂ based dielectric TFT (Fig. 3(a)).

The analog performance is further analyzed by the graph of early voltage (V_{EA}) and intrinsic gain (A_V) plotted in Fig. 3 (c). The variation in V_{EA} is 29% when dielectric material is changed from SiO₂ to HfO₂ for a-ITZO TFT. This higher value of V_{EA} has a good sign as it tells that the simulated TFT has better control on channel length modulation and DIBL. The left axis of Fig. 3 (c) shows the variation of intrinsic gain (A_V) with V_{DS} . It is defined as the ratio of transconductance (g_m) by drain conductance (g_d). An increase of nearly 55% in A_V is observed for HfO₂ based a-ITZO TFT as compared to SiO₂ material based TFT.

A combined plot of TGF and g_m is drawn as a function of V_{GS} in Fig. 3(d). The left axis of the figure

shows that greater value of transconductance ($\sim 10^{-5}$ S) is attained for a-ITZO TFT with HfO_2 as dielectric. The increment in g_m with high- k material is because of increase in drain to source current of device. Effective use of current to achieve desired value of transconductance is determined by TGF. TGF is a major performance parameter for analog applications which indicates TFT's capability to amplify a signal for a certain I_{DS} . The value of TGF also increases with high- k dielectric material. This trend follows as that of maximum g_m/I_{DS} is for a-ITZO TFT with HfO_2 dielectric followed by Al_2O_3 , Si_3N_4 and SiO_2 for $V_{GS} < 2$ V. It is also observed that with increasing V_{GS} , TGF value starts to decrease for all configurations. This analysis is very beneficial for circuit designers working on analog applications.

Fig.4(a-d) represent the calculation of RF parameters i.e. C_{GS} and C_{GD} , GBP, f_T , F_{max} , GTFP, TFP and GFP with respect to different dielectric materials. The RF analysis for the a-ITZO TFT is done from AC analysis by including frequency of 1 MHz after post processing of DC solution. The C_{GS} and C_{GD} values for different dielectric material TFT is plotted in Fig. 4 (a). It is seen that capacitance values have incremental nature with high k material because of the increased fringing field density in the device [33]. The value of C_{GS} and C_{GD} are almost same for SiO_2 , Si_3N_4 and Al_2O_3 . The variation in C_{GS} and C_{GD} values for a-ITZO TFT for HfO_2 dielectric is from 253fF (at $V_{GS} = 0$ V) to 274fF (at $V_{GS} = 20$ V) and 176fF (at $V_{GS} = 0$ V) to 266 fF (at $V_{GS} = 20$ V) respectively.

Unity gain cut-off Frequency (f_T) is another FOM for high-speed digital application. The variation of f_T against V_{GS} in plotted in Fig. 4(b). It is a potential characteristic for devices in defining the acceptable bandwidth range so that they can be used for RF application. As depicted from the Fig. 4(b), there is a slight variation in f_T with changing dielectric material from low to high- k . This trend is seen because the rate of improvement in g_m is higher than that of capacitances. Inset of Fig. 4(b) shows the variation of GBP with V_{GS} . Close analysis of the curve shows both (f_T & GBP) have same nature with V_{GS} . At $V_{GS} = 4$ V, the peak value of f_T and GBP for ITZO TFT with HfO_2 dielectric is 13.42 Mhz and 3.34 MHz respectively.

The plot of maximum frequency of oscillation (F_{max}) with V_{GS} is shown in Fig. 4 (c). F_{max} determines the transit frequency at which maximum power gain is available. F_{max} value shows decreasing trend with V_{GS} . The a-ITZO TFT with HfO_2 dielectric achieve

nearly 0.17 times increase in F_{max} than a-ITZO TFT with SiO_2 dielectric. GTFP allows the circuit designers to identify the best region of operation by trading off gain, transconductance and speed. As seen from the inset of Fig. 4 (c), GTFP value increases by nearly 55% when using HfO_2 as dielectric with a-ITZO TFT than by using SiO_2 .

Fig. 4 (d) represent the variation of TFP and GFP w.r.t V_{GS} for different dielectric materials. TFP defines the tradeoff between power and bandwidth. As seen from the curve that high TFP value is achieved for a-ITZO TFT with high K dielectric at $V_{GS} < 4$ V and after that it is decreased as V_{GS} is increased. GFP as seen from right axis of Fig. 4 (d) shows linear rise with the V_{GS} . The GFP for a-ITZO TFT with HfO_2 dielectric has 0.5 times more GFP value than its SiO_2 counterpart.

3.2 Impact of Dielectric Thickness (D_t) on the DC, Analog and RF Parameters

As deduced from the last analysis, DC, analog/RF parameters are affected by dielectric material. Changing the low- k material to high- k implies low power, low leakage and high-performance electronic devices. In this section, impact of D_t scaling is seen on different Analog/RF parameters. Thickness of the dielectric material is inversely proportional to capacitance. As the thickness of dielectric material reduces, it increases the capacitance which in turn induces more number of charge carriers at the same output voltage and increases the drain current. g_m will also improve by variation of gate capacitance, which results in reduction of extrinsic delays in digital circuits. Fig. 5 and 6 shows the calculation of different Analog/RF parameters of a-ITZO TFT with HfO_2 as dielectric material. The device is simulated and compared for different dielectric thickness (D_t) = 150 nm, 250 nm, 300 nm, 350 nm.

Fig. 5 (a) represent the calculation of I_{DS} in linear and log scale w.r.t V_{GS} at $V_{DS} = 5$ V. The peak value of I_{DS} is 1.1 mA, 824 μA , 661 μA , 552 μA for D_t of 150 nm, 200 nm, 250 nm and 300 nm respectively. The different parameters like V_t , V_{on} , SS, I_{on} , I_{off} were extracted from the linear and log transfer curves and tabulated in Table IV. The I_{off} state current for all the dielectric thickness is found in the range of 10^{-13} to 10^{-14} . This value is above the requirement of ITRS for low power application.

The right axis of Fig. 5 (b) shows output current (I_{DS}) w.r.t V_{DS} at constant $V_{GS} = 5$ V for different dielectric thickness (D_t). It is evident from the curve

that decrease in thickness improves the electrical characteristic and also the performance of the device because of increased dielectric capacitance per unit area [C_i]. It is also due to the decrease in the energy band gap of dielectric material [35]. Here, it is seen that all a-ITZO TFT shows excellent saturated characteristic at approx. $V_{DS} = 6$ V and the thinnest TFT exhibit highest saturation current. The g_d for Table IV: Extracted parameters: V_t , V_{on} , SS, I_{on} , I_{off} depending on dielectric thickness variation

Dielectric Thickness (nm)	V_t (V)	V_{on} (V)	Sub-Threshold Swing (V/decade)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}
150	2.21	-0.26	0.22	1.09×10^{-3}	2.74×10^{-14}	3.98×10^{10}
200	2.19	-0.29	0.62	8.24×10^{-4}	1.72×10^{-13}	4.77×10^9
250	2.17	-0.32	0.64	6.61×10^{-4}	1.75×10^{-13}	3.75×10^9
300	2.15	-0.35	0.66	5.52×10^{-4}	4.03×10^{-13}	1.37×10^9

(a)

(b)

(c)

(d)

Fig. 5 (a) I_{DS} (Linear and Log) (b) g_d & Output I_{DS} (c) R_O (Inset), V_{EA} and A_V (d) g_m & TGF for different values of D_t

Early voltage (V_{EA}) and Intrinsic Gain (A_V) are another FOM and their calculation with V_{DS} is represented in the Fig. 5 (c). E_{VA} is higher for thinnest TFT i.e. nearly 80% higher than that of $D_t = 300$ nm. The value of A_V is 89.3 dB, 109.2 dB, 137.1 dB and 176.2 dB for dielectric thickness of 300 nm, 250 nm, 200 nm and 150 nm respectively. Both V_{EA} and A_V has higher values for thinner TFT and found its use in fast memory and RF amplification

application. g_m as seen from the left axis of Fig. 5(d) shows inverse trend with dielectric thickness. Higher value of g_m is desired to design high performance circuits. It is seen that apex value of g_m increases approximately 2 times when D_t reduced from 300 nm to 150 nm. Right axis of Fig. 5(d) shows inverse trend with dielectric thickness. Higher value of g_m is desired to design high performance

Fig. 6 (a) C_{GS} & C_{GD} (b) f_T & GBP (Inset) (c) F_{max} & GTFP (inset) (d) TFP & GFP for different values of D_t

performance circuits. It is seen that apex value of g_m increases approximately 2 times when D_t reduced from 300 nm to 150 nm. Right axis of Fig. 5(d) reveals that considerable improvement in TGF is seen for a-ITZO TFT with a decrease in dielectric thickness. The lower value of subthreshold swing (0.22 V/decade) exhibit higher value of TGF (6.89 V^{-1}) for $D_t = 150$ nm.

Fig. 6(a-d) represent the calculation of C_{GS} & C_{GD} (b) f_T & GBP (Inset) (c) F_{max} & GTFP (inset) (d) TFP & GFP with respect to dielectric thickness (D_t). Fig. 6 (a) shows the variation of small signal

capacitance C_{GS} & C_{GD} w.r.t V_{GS} . The variation in C_{GS} & C_{GD} values for a-ITZO TFT with dielectric thickness $D_t = 150$ nm is from 220 fF ($V_{GS} = 0$ V) to 365 fF ($V_{GS} = 20$ V) and 214 fF (at $V_{GS} = 0$ V) to 354 fF (at $V_{GS} = 20$ V) respectively. From circuit designer point of view these low values of capacitance are required.

These intrinsic capacitances (C_{GS} , C_{GD}) are used to find cut-off frequency (f_T) which is shown in Fig. 6 (b). From figure it is seen that a-ITZO TFT with dielectric thickness ($D_t = 150$ nm) yield a peak value of 14.3 MHz at $V_{GS} = 4.5$ V. GBP with V_{GS} is shown in the

inset of Fig. 6 (b). The nature of GBP and f_T is similar when $C_{GS} = C_{GD}$ is approximated. a-ITZO TFT using thinner dielectric attains higher GBP. Although the variation is not so much.

The frequency at which power gain is unity is known as maximum frequency of oscillation (F_{max}). As evident from the Fig. 6 (c), the value of F_{max} decreases as we increase the V_{GS} . The maximum value of F_{max} at $V_{GS} = 3.5$ V for dielectric thickness (D_t) value of 150 nm, 200 nm, 250 nm and 300 nm is 20.4 KHz, 19.5 KHz, 18.9 KHz and 18.4 KHz

respectively. GTFP is defined as the product of intrinsic gain and TFP as shown in the inset of Fig. 6 (c). The highest value of GTFP as obtained for $D_t = 150$ nm is nearly two times that of GTFP at $D_t = 300$ nm. Fig. 6 (d) shows the calculation of TFP and GFP w.r.t V_{GS} for different values of D_t . As seen from the left axis of Fig. 6 (d) that there is a slight variation in TFP with change in dielectric thickness. The value of GFP as seen from the right axis of Fig. 6 (d) are 1.22 GHz, 1.49 GHz, 1.86

Table V: Extracted parameters: V_t , V_{on} , SS, I_{on} , I_{off} depending on temperature variation

Temperature (K)	V_t (V)	V_{on} (V)	Sub-Threshold Swing (V/decade)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}
300	2.19	-0.29	0.621	8.24×10^{-4}	1.72×10^{-13}	4.77×10^9
350	2.18	-0.32	0.662	6.54×10^{-4}	5.30×10^{-14}	1.23×10^{10}
400	2.17	-0.35	0.703	5.35×10^{-4}	2.03×10^{-13}	2.63×10^9
450	2.16	-0.38	0.744	4.48×10^{-4}	3.56×10^{-13}	1.26×10^9

(a)

(b)

(c)

(d)

Fig. 7 (a) I_{DS} (Linear and Log) (b) g_d & Output I_{DS} (c) R_O (Inset), V_{EA} and A_V (d) g_m & TGF for different values of T

GHz and 2.39 GHz for decreasing dielectric thickness from 300 nm to 150 nm in steps of 50 nm respectively.

3.3 Impact of Temperature on the DC, Analog and RF Parameters

In this section, impact of temperature (T) on various DC, analog and RF parameters is analyzed. In many

applications like AMOLED, medical display circuits, Amorphous Oxide Semiconductor (AOS) material plays an important role. The stability and reliability of particular circuit depend on their operating temperature like most of the medical circuits need to work in the range of 300-400K. For these applications, temperature stability of AOS TFT must be analyzed. Fig. 7 and 8 is obtained here to see the impact of tem-

(a)

(b)

(c)

(d)

Fig. 8 (a) C_{GS} & C_{GD} (b) f_T & GBP (Inset) (c) F_{max} & GTFP (inset) (d) TFP & GFP for different values of Dt

-perature changes on the different analog/RF parameters of a-ITZO TFT.

Fig.7(a) shows the variation of I_{DS} with V_{GS} at $V_{DS} = 5$ V. It is seen that drain current (I_{DS}) in linear scale experience an increase of nearly 85% when temperature changes from 450 K to 300 K. This trend is attributed to (a) electron and hole trapping at the interface between the material, (b) oxygen vacancies and (c) donor like defect creation in ITZO channel [36]. Out of these three, electron and hole trapping at interface will lead to degradation of drain current. Huo *et al.* [37] also showed the same trend in drain current and they verified their result by UPS experimental analysis which tells electron structure information. Higher UPS attributes that more electrons are trapped and less free electron availability leading to decreased electrical performance with increased temperature. The different parameters used to analyze the TFT performance are extracted from linear and log curves of transfer characteristics (Fig. 7 (a)) and tabulated in Table V. The best result is observed for $T = 300$ K with $V_{on} = -0.29$ V, $I_{on}/I_{off} = 4.77 \times 10^{+9}$. The V, it is seen that reduction in SS with decreasing temperature will lead to reduced N_t and so it is the reason of increased I_{DS} at decreased temperature. The left side of the Fig. 7 (b) shows the variation of drain conductance (g_D) w.r.t V_{DS} . It is also decreasing by nearly 2.2 % with the increasing temperature.

Fig. 7 (c) shows the variation of TGF and g_m with V_{GS} . Both TGF and g_m show decremented nature as we increase the temperature. The apex value of g_m at $V_{GS} = 4$ V are 4.64×10^{-5} S, 3.67×10^{-5} S, 3.00×10^{-5} S, 2.52×10^{-5} S for $T = 300$ K, 350 K, 400 K, 450 K

I_{off} value is in 10^{-13} - 10^{-14} range for all the temperature variation.

The right axis of Fig.7(b) shows the output characteristic of a-ITZO TFT. As seen, after $V_{DS} = 7$ V, the I_{DS} starts to saturate. The value of I_{DS} is 140 μ A, 111 μ A, 91.5 μ A, 77.1 μ A for 300 K, 350 K, 400 K, 450 K respectively. The conduction mechanism in AOS TFT is mainly hopping but here it changes to band conduction or percolation in the conduction and I_{DS} reduces as temperature increases [36]. So, trapping plays an important role for analyzing AOS TFT.

The electrical properties of device can be improved based on both the carrier concentration of active layer and interface trap density. The interface trap density (N_t) can be extracted by subthreshold slope (SS) and is given by Eq. 2 [38]:

$$N_t = \left(\frac{SS}{\ln 10} \frac{q}{kT} - 1 \right) \frac{C_{ox}}{q} \quad (2)$$

where q is electron charge, k is Boltzmann's constant, T is temperature and C_{ox} is given by Eq. 1. From table

respectively. TGF decreases nearly 35% when temperature is changed from 300 K to 450 K.

Inset of Fig. 7 (d) shows the variation of output resistance (R_O) with V_{DS} . R_O at $T = 450$ K is nearly 1.8 times that of $T = 300$ K. V_{EA} and A_V as seen from Fig. 7 (d) shows a very little or no impact with temperature variation. From close examination it can be concluded that analog performance is better for $T = 300$ K.

Fig. 8 (a-d) show the variation of different RF parameter with different temperature ranges. The C_{GS} & C_{GD} values as seen from the Fig. 8 (a) have shown

same nature for all the temperature variations. It is also seen that C_{GS} is greater than that of C_{GD} , which can be attributed to uneven distribution of charge on application of drain source bias [39]. The highest value of C_{GS} & C_{GD} is 280 fF and 266 fF respectively, which is very less and beneficial for circuit designing.

The variation of f_T with V_{GS} is seen from Fig. 8(b). Nearly 85% rise is seen in f_T when temperature is decreased from 450 K to 300 K in steps of 50 K. GBP as seen from the inset of Fig. 8 (b) has shown the same nature as that of f_T . GBP has attained peak value of 3.34 MHz at $V_{GS} = 4V$ for $T = 300$ K. Fig. 8 (c) represent the calculation of F_{max} with V_{GS} for different temperature ranges. The peak F_{max} for all temperature variation is nearly 19.47 KHz at $V_{GS} = 3.5$ V.

The measurement of GTFP with the V_{GS} when swept from 0 to 20 V at fixed V_{DS} of 5 V is seen from inset of Fig. 8 (c). The peak value of GTFP at $V_{GS} = 20$ V are 104.5 MHz, 82.7 MHz, 67.5 MHz and 56.3 MHz for $T = 300$ K, 350 K, 400 K and 450 K respectively. Fig. 8 (d) is obtained to see the variation of GFP and TFP with V_{GS} . GFP as seen from the curve is unchanged for all temperatures. The left axis of Fig. 8 (d) shows TFP at $T = 300$ K is nearly 2.3 times that of TFP at $T = 450$ K.

4 Application of ITZO TFT as Resistive Load Inverter

In this section, a resistive load inverter circuit to see the application of simulated TFT at device level is implemented. As seen in Fig. 9 (a), a-ITZO TFT is connected with a 1 M Ω load resistor (R_L) to examine clear On/Off levels in VTC curve. a-ITZO TFT can be considered as variable register depending on the V_{GS} values. After verifying successful resistive operation, the transistor parameter (dielectric value (high k), thickness and temperature) have been varied to observe the respective variations seen in Fig. 9 (b), (c) and (d). As deduced from the Fig. 9 (b, c and d), the V_{OUT} of VTC is consistent with the transfer characteristics as shown in Fig. 3(a), 5(a) and 7(a). It

is seen that there is an improvement in VTC by changing the dielectric material to high k (SiO_2 to HfO_2) or by decreasing the thickness of dielectric (300 nm to 150 nm). This change is attributed to increase in mobility and decrease in subthreshold swing value when dielectric material is changed to high k or thickness is decreased. With temperature the VTC curve shows a constant behavior. This investigation confirms the potentiality of simulated TFT structure for the designing of next generation logic circuits.

5 Conclusion

In this paper, RF and analog performance of an amorphous Indium Tin Zinc Oxide (a-ITZO) thin film transistor have been investigated. The impact of dielectric material, dielectric thickness (D_t) and temperature (T) on the DC, analog and RF parameters of a-ITZO TFT have been studied in detail. The investigations suggest that high k materials have potential impact on all analog and RF parameters. HfO_2 as dielectric provides best results in comparison to its low K dielectric siblings. Impact of D_t on all analog and RF parameters have also been reported. Reduction of D_t provides best results and this variation has same impact as that of using high k dielectric material. It is also been seen that scaling the device dimension leads to increased leakage current. Although, all the variation shows I_{off} value in range of 10^{-13} to 10^{-14} which in turn provides high I_{on}/I_{off} . In last, the stability and reliability of a-ITZO TFT by varying temperature is investigated and it is seen that at $T = 300$ K, the device provides best results. This is considered as one of the FOM's of the simulated structure as most of equipment/devices work on ambient temperature. It is concluded that using high k material which has a bandgap close to SiO_2 or thinner dielectric at $T = 300$ K gives the optimum results. Successful implementation of a-ITZO TFT as resistive load inverter indicates that the simulated TFT structure can provide further directions for researchers to design

Fig. 9 Voltage Transfer Characteristic (VTC) of resistive load inverter for different variations (a) Dielectric Material (b) Dielectric thickness (D_t) and (c) Temperature

complex analog and RF logic circuits.

6 Author Declarations

6.1 Ethics approval and consent to participate

Taken Informed consent from all authors included in the study

6.2 Consent for publication

Taken Informed consent from all authors included in the study

6.3 Availability of Data and Materials

For this submission, no linked research data sets are there.

6.4 Competing interests

The authors declare no competing interests.

6.5 Funding

The authors have not received any funding for this work.

6.6 Author's Contributions

The basic motivation to design and analyze a-ITZO TFT for Analog/RF application is of Neeraj Jain and Kunal Singh (Author 1 & 2). Shashi Kant Sharma and Renu Kumawat supervised the simulation work and conceptual discussions to develop and modify the manuscript.

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7 Compliance with Ethical Standards

7.1 Disclosure of potential conflicts of interest

The authors declare that they have no conflict of interest.

7.2 Research involving Human Participants and/or Animals

Not applicable.

7.3 Informed consent

Not applicable.

References

1. The "Thin Film Transistor Market - Growth, Trends, COVID-19 Impact, and Forecasts (2021 - 2026)", April 23, 2021
2. Ji, D., Jang, J., Park, J. H., Kim, D., Rim, Y. S., Hwang, D. K., & Noh, Y.-Y. (2020) Recent progress in the development of backplane thin film transistors for information displays. *J Inf. Disp.* <https://doi.org/10.1080/15980316.2020.1818641>
3. Lu, N., Jiang, W., Wu, Q., Geng, D., Li, L., & Liu, M. (2018) A Review for Compact Model of Thin-Film Transistors (TFTs). *Micromachines.* <https://doi.org/10.3390/mi9110599>
4. Braga, J. P., Lima, G. R. D., Gozzi, G., & Santos, L. F. (2018) Electrical Characterization of Thin-Film Transistors Based on Solution-Processed Metal Oxides. *Des. Simul. Construction F. Eff. Transistors.* <https://doi.org/10.5772/intechopen.78221>
5. Park, S.-H. K., Hwang, C.-S., Jeong, H. Y., Chu, H. Y., & Cho, K. I. (2008). Transparent ZnO-TFT Arrays Fabricated by Atomic Layer Deposition. *Electrochemical and Solid-State Letters.* <https://doi.org/10.1149/1.2801017>
6. Avis, C., Kim, Y., & Jang, J. (2019). Amorphous Tin Oxide Applied to Solution Processed Thin-Film Transistors. *Mater.* <https://doi.org/10.3390/ma12203341>
7. Liu, W.-S., Lin, Y.-H., Huang, C.-L., & Wang, C.-W. (2017). Device Performance Improvement of Transparent Thin-Film Transistors With a Ti-Doped GaZnO/InGaZnO/Ti-Doped GaZnO Sandwich Composite-Channel Structure. *IEEE Transactions on Electron Devices.* <https://doi.org/10.1109/ted.2017.2696956>
8. Dargar, S. K., & Srivastava, V. M. (2019). Design and analysis of IGZO thin film transistor for AMOLED pixel circuit using double-gate tri active layer channel. *Heliyon* <https://doi.org/10.1016/j.heliyon.2019.e01452>
9. Cho, J., Hwang, S., Ko, D.-H., & Chung, S. (2019). Transparent ZnO Thin-Film Deposition by Spray Pyrolysis for High-Performance Metal-Oxide Field-Effect Transistors. *Materials.* <https://doi.org/10.3390/ma12203423>
10. Chung, J. H., Lee, J. Y., Kim, H. S., Jang, N. W., & Kim, J. H. (2008). Effect of thickness of ZnO active layer on ZnO-TFT's characteristics Thin Solid Films. <https://doi.org/10.1016/j.tsf.2007.07.107>
11. Cheremisin, A. B., Kuznetsov, S. N., & Stefanovich, G. B. (2015). Effect of indium low doping in ZnO based TFTs on electrical parameters and bias stress stability. *AIP Advances.* <https://doi.org/10.1063/1.4935789>
12. Dong, J., Han, D., Li, H., Yu, W., Zhang, S., Zhang, X., & Wang, Y. (2018). Effect of Al doping on performance of ZnO thin film transistors *Appl. Surf. Sci.* <https://doi.org/10.1016/j.apsusc.2017.10.071>
13. Chen, Z., Han, D., Zhang, X. et al. (2019). Improving Performance of Tin-Doped-Zinc-Oxide Thin-Film Transistors by Optimizing Channel Structure. *Sci Rep.* <https://doi.org/10.1038/s41598-019-53766-2>
14. Kara, R., Mentar, L., & Azizi, A. (2020). Synthesis and characterization of Mg-doped ZnO thin-films electrochemically grown on FTO substrates for optoelectronic applications. *RSC Advances.* <https://doi.org/10.1039/d0ra06541b>
15. Lee, G. J., Kim, J., Kim, J.-H., Jeong, S. M., Jang, J. E., & Jeong, J. (2014). High performance, transparent a-IGZO TFTs on a flexible thin glass substrate. *Semiconductor Sci. Technol.* <https://doi.org/10.1088/0268-1242/29/3/035003>
16. Nomura, K., Ohta, H., Takagi, A. et al. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature.* <https://doi.org/10.1038/nature03090>
17. Yabuta, H., Sano, M., Abe, K., Aiba, T., Den, T., Kumomi, H., Hosono, H. (2006). High-mobility thin-film transistor with amorphous InGaZnO4 channel fabricated by room temperature rf-magnetron sputtering. *Appl. Phys. Letters.* <https://doi.org/10.1063/1.2353811>

18. Arai, T. (2012). Oxide-TFT technologies for next-generation AMOLED displays. *J. Soc. Info. Disp.* <https://doi.org/10.1889/jsid20.3.156>
19. Grover, M. S., Hersh, P. A., Chiang, H. Q., Kettenring, E. S., Wager, J. F., & Keszler, D. A. (2007). Thin-film transistors with transparent amorphous zinc indium tin oxide channel layer. *J. Phys. D: Appl. Phys.* <https://doi.org/doi:10.1088/0022-3727/40/5/004>
20. SILVACO-TCAD, ATLAS user's manual: device simulation software, SILVACO International, California, 2019.
21. Seo, J.-H., Ling, T., Gong, S., Zhou, W., Ma, A. L., Guo, L. J., & Ma, Z. (2016). Fast Flexible Transistors with a Nanotrench Structure. *Scientific Reports.* <https://doi.org/10.1038/srep24771>
22. Bahubalindruni, P. G., Kiazadeh, A., Sacchetti, A., Martins, J., Rovisco, A., Tavares, V. G., Barquinha, P. (2016). Influence of Channel Length Scaling on InGaZnO TFTs Characteristics: Unity Current-Gain Cutoff Frequency, Intrinsic Voltage-Gain, and On-Resistance. *J. Disp. Technol.* <https://doi.org/10.1109/jdt.2016.2550610>
23. Taouririt, T. E., Meftah, A., Sengouga, N., Adaika, M., Chala, S., & Meftah, A. (2019). Effects of high-k gate dielectrics on the electrical performance and reliability of an amorphous indium–tin–zinc–oxide thin film transistor (a-ITZO TFT): an analytical survey. *Nanoscale.* <https://doi.org/10.1039/c9nr03395e>
24. Martins, J., Bahubalindruni, P., Rovisco, A., Kiazadeh, A., Martins, R., Fortunato, E., & Barquinha, P. (2017). Bias Stress and Temperature Impact on InGaZnO TFTs and Circuits. *Materials.* <https://doi.org/10.3390/ma10060680>
25. Sheng, J., Han, J.-H., Choi, W.-H., Park, J., & Park, J.-S. (2017). Performance and Stability Enhancement of In–Sn–Zn–O TFTs Using SiO₂ Gate Dielectrics Grown by Low Temperature Atomic Layer Deposition. *ACS Appl. Mat. Interfaces.* 25.
- Sheng, J., Han, J.-H., Choi, W.-H., Park, J., & Park, J.-S. (2017). Performance and Stability Enhancement of In–Sn–Zn–O TFTs Using SiO₂ Gate Dielectrics Grown by Low Temperature Atomic Layer Deposition. *ACS Appl. Mat. Interfaces.* <https://doi.org/10.1021/acsami.7b15419>
26. Kumar Singh, V., & Mazhari, B. (2012). Impact of scaling of dielectric thickness on mobility in top-contact pentacene organic thin film transistors. *J. Appl. Phys.* <https://doi.org/10.1063/1.3681809>
27. Vyas, S., Dwivedi, A. D. D., & Dwivedi, R. D. (2018). Effect of gate dielectric on the performance of ZnO based thin film transistor. *Superlattices and Microstructures.* <https://doi.org/10.1016/j.spmi.2018.05.040>
28. Kim, J., Rim, Y. S., Chen, H., Cao, H. H., Nakatsuka, N., Hinton, H. L., Weiss, P. S. (2015). Fabrication of High-Performance Ultrathin In₂O₃ Film Field-Effect Transistors and Biosensors Using Chemical Lift-Off Lithography. *ACS Nano.* <https://doi.org/10.1021/acs.nano.5b01211>
29. Jang, J., Kim, D. G., Kim, D. M., Choi, S.-J., Lim, J.-H., Lee, J.-H., Kim, D. H. (2014). Investigation on the negative bias illumination stress-induced instability of amorphous indium-tin-zinc-oxide thin film transistors. *Appl. Phys. Letters.* <https://doi.org/10.1063/1.4898069>
30. Hoel, C. A., Mason, T. O., Gaillard, J.-F., & Poeppelemer, K. R. (2010). Transparent Conducting Oxides in the ZnO-In₂O₃-SnO₂ System. *Chem. Mat.* <https://doi.org/10.1021/cm1004592>
31. Taouririt, T. E., Meftah, A., & Sengouga, N. (2018). Effect of the interfacial (low-k SiO₂ vs high-k Al₂O₃) dielectrics on the electrical performance of a-ITZO TFT. *Appl. Nanosci.* <https://doi.org/10.1007/s13204-018-0866-x>
32. Verma, Y. K., Mishra, V., & Gupta, S. K. (2020). Analog/RF and Linearity Distortion Analysis of MgZnO/CdZnO Quadruple-Gate Field Effect Transistor (QG-FET). *Silicon.* <https://doi.org/10.1007/s12633-020-00406-4>
33. Pradhan, K. P., Mohapatra, S. K., Sahu, P. K., & Behera, D. K. (2014). Impact of high-k gate dielectric on analog and RF performance of nanoscale DG-MOSFET. *Microelectronics J.* <https://doi.org/10.1016/j.mejo.2013.11.016>
34. Adak, S., & Swain, S. K. (2019). Impact of high-K dielectric materials on performance analysis of underlap In_{0.17}Al_{0.83}N/GaN DG-MOSHEMTs. *Nano.* <https://doi.org/10.1142/s1793292019500607>
35. Mallik, A., & Chattopadhyay, A. (2012). The Impact of Fringing Field on the Device Performance of a p-Channel Tunnel Field-Effect Transistor With a High-k Gate Dielectric. *IEEE Transactions on Electron Devices.* <https://doi.org/10.1109/ted.2011.2173937>
36. Chen, Y.-J., & Tai, Y.-H. (2015). Hysteresis of Transistor Characteristics of Amorphous IGZO TFTs Studied by Controlling Measurement Speed. *ECS Solid State Letters.* <https://doi.org/10.1149/2.0041504ssl>
37. Huo, C., Dai, M., Hu, Y., Zhang, X., Wang, W., Zhang, H., Zhu, W. (2019). Temperature Dependence

Of AOS Thin Film Nano Transistors For Medical Applications. International J. Nanomed. <https://doi.org/10.2147/ijn.s208023>

38. Liang, Y., Kyungsoo, J., Velumani, S., Cam, P. T. N., & Junsin, Y. (2015). Effects of interface trap density on the electrical performance of amorphous InSnZnO thin-film transistor. J. Semiconductors. <https://doi.org/10.1088/1674-4926/36/2/024007>

39. Tang Z, Wie CR. (2009). Capacitance–voltage characteristics and device simulation of bias temperature stressed a-Si:H TFTs. Solid State Electron, <https://doi.org/10.1016/j.sse.2009.09.025>