Device Design, Simulation and Qualitative Analysis of GaAsP/ 6H-SiC/ GaN Metal Semiconductor Field effect transistor

B BALAJI (balaji@kluniversity.in)
KLEF: KL University
K.Srinivasa Rao
Koneru Lakshmaiah Education Foundation
M. Aditya
Koneru Lakshmaiah Education Foundation
K.Girija Sravani
Koneru Lakshmaiah Education Foundation

Research Article

Keywords: GaAsP, 6H-SiC, GaN, Drain Conductance, Transconductance, Silvaco TCAD

Posted Date: September 20th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-890973/v1

Abstract

In this paper we proposed a new structure of GaAsP/6H-SiC/GaN Power semiconductor field effect transistor with undoped region under gate. The device is made of semiconductor material i.e Gallium Nitride (GaN), Silicon Carbide and Gallium Arsenide Phospide and utilized Silvaco TCAD in 10nm technology for the simulation. The length and width of the undoped region is equal to length of channel and this undoped region under the gate will reduce the peak electric field which existed in the channel region. The saturated drain current of proposed structure is about 53 percent higher than the conventional transistor and subsequently an improvement in other drain current parameters and analog parameters. The performance comparison is mainly in terms of drain current characteristics and analog characteristics such as Gain, transconductance, drain conductance, threshold voltage. As a subsequent improvement of performance parameters, this structure is used at high power and high frequency applications

1. Introduction

As the technology developing day to day, semiconductors are playing a vital role for the human being [1]. The semiconductor connected with gate from the channel for flow of current from source to drain. If gate is not connected properly, then there will be a leakage current therefore gain of transistor will be decrease. The reduction of leakage current is based on proper connectivity of gate in different approaches [3]. If the gate is formed at the channel by a silicon dioxide (SiO_2) called Metal oxide semiconductor field effect transistor (MOSFET) and the gate is detached by the Schottky barrier call it as Metal semiconductor field effect transistor (MESFET)[7]. Power metal semiconductor field effect transistor has various operations in communications for high power and high frequency and low noise applications, medical engineering [9]. In submicron technology power metal semiconductor field effect transistors have low integration density and the same invention suitable for fabrication and modeling of device [8].

Gallium Nitride (GaN), Silicon Carbide(SiC) and Gallium Arsenide phosphide(GaAsP) has excellent potential to attract and improve the electrical properties and offer wider bandwidth operations and lower system size than silicon and gallium arsenide power MESFET[2].The channel is formed by inversion phenomenon in the MOSFET consequently reduces the mobility of the carrier and operating frequency of the transistor[10]. While in MESFET the channel is formed under the active region which increases mobility of the charge carriers in the transistor. Which has advantages of MESFET over MOSFET [4–6]

The content of this paper as follows: In the second section the device structure for three different materials are reported. In the third section the simulation results of various drain current characteristics and analog characteristics and various models and methods used in the devices are presented. The conclusion is reported in the final section

2. Structure Of Proposed Device

The proposed device structure of Power metal semiconductor field effect transistor (MESFET) and conventional device as shown in Fig. 1 and Fig. 2. The proposed device made of semiconductor material i.e Gallium Nitride (GaN), Silicon Carbide(SiC) and Gallium Arsenide phosphide (GaAsP) with undoped region under the gate compared to conventional structure[11].Both devices are simulated in Silvaco TCAD in 10nm

technology and the dimensions of these two transistors are equal, whereas length of undoped region is equal to length of channel (L_g=0.01μm) and thickness of undoped region thickness (T_u=0.04μm) with a work function of 4.87eV. Gate –source and gate-drain distance of both transistors are L_{gs}=0.001μm and L_{gd}=0.001μm commonly .The length of area without doping on the source side(L_s) and drain side(L_d) changes from zero to 0.002um[14–16].The channel uses doping concentration of 1 X 10^{17} cm^{-3} and source and drain doping concentration of 5 X 10^{18} cm^{-3}. In this paper we used important models like conmob, fldmob, evsatmod = 1, hcte.el, taurel.el = 1.e-12, taumob.el = 1.e-12, vsat = 1.e7, str–set, method newton maxtrap = 6[13] .Gate capacitance and electric field in the channel will be reduced by undoped region connected under the gate. The device structure is designed and simulations are carried out in ATLAS. Both devices are designed with GaAsP/6H-SiC/GaN materials and drain current simulations and analog simulations are carried out [12]. The effective use of parameters for simulation of structure is given in Table.1. Various models and methods are used for simulation of devices. The models and methods are given in Table.2 and Table.3

Table.1The parameters used for the simulation of structure.

Parameters	Symbol	Value
Device length	L_D	0.032μm
Gate length	L_g	0.01μm
Gate to source distance	L_{gs}	0.011μm
Gate to drain distance	L_{gd}	0.011 μm
Undoped region Length	L_s	0.01μm
Undoped region thickness	L_u	0.04μm
work function = 4.87Ev		

Table.2 Models used for simulation of the device

Model	Description
conmob	Specifies the concentration
	dependent mobility
fldmob	Calculation of the field
	dependent mobility
evsatmod = 1	implements the carrier temperature
	dependent mobility is invoked
hcte.el	to enable energy balance for electrons
taurel.el	specifies the relaxation time in the energy balance
taumob.el	specifies the relaxation time for electrons
	in the temperature dependent mobility

Table.3 Models used for simulation of the device

Method	Description
newton	used as solution method in
	subsequent solve statement
maxtrap	specifies the number of
	times the trap procedure
	repeated
autonr	specifies to increase the speed
	of newton solution
dvlimit	specifies the maximum
	magnitude of potential correction
nblockit	specifies the block iterations

3. Results And Discussion

The drain current is obtained as a function of drain voltage for three materials as shown in Fig.3 and given equation is essential to obtain the increased drain current

$I_{drain-sat} = z\, b(x)\, q\, n(x)\, v(x)$

Where z= channel width

b(x)=effective depth of the channel

q=electron charge

n(x)=electron density

v(x)=electron velocity

The saturated drain current (I_{ds}) is obtained as a function of gate voltage (V_{gs}) for different materials as shown in Fig4. As the device dimensions and length of channel is minimizing, significantly drain current increases [17]. The maximum drain current of proposed device is obtained at V_g=0.6V and V_g=2V .The drain current is increases based on increasing of drain voltage, which will give movement of the electrons in the channel

The Drain conductance versus drain voltage for three materials at V_{ds}=2V is shown in Fig 5. In which drain conductance of GaAsP is higher than 6H-SiC and GaN materials.

The undoped MESFET attains the highest packing density due to better current flow in the device [18-20]. Hence this structure provides more improvement in transcondutance. To achieve proper gain of device high transconductance is needed [21-23] and which is shown in Fig.6.

$$Transconductance\ (G_m) = \frac{\partial I_{ds}}{\partial V_{gs}}$$

The reduction of sub threshold slope increases the off-current and power dissipation in the device. These characteristics are essentials for low power portable devices. The amount of gate voltage needed for variation of drain current defined as sub threshold slope given by

$$Subthreshold\ slope\ (SS) = \frac{\partial V_{gs}}{\partial(\log\ (I_{ds}))}$$

The sub threshold curve plotted for different materials as shown in Fig.7.The suitable value of Sub threshold slope is recommended to reduce the effect of heating in the device with channel length.

Table 4: Comparision of performance parameters

Parameters	GaAsP	SiC	GaN
I_{on}(A)	5.05E-03	2.18E-03	2.15-03
I_{off}(A)	-1.61E-18	-1.40E-24	-3.69E-11
I_{on}/I_{off}	3.14E+15	1.55+21	1.71E-08
G_d(S)	2.51E-02	3.06E-03	5.06E-03
R_{on}(Ω)	3.98E+01	3.27E+02	1.98E+02
V_{th}(V)	0.49	1.13	0.59
G_m(S)	-1.74E-07	3.36E-15	-7.38E-10
Gain	6.92E-06	1.10E-12	1.46E-07

The performance parameters of the proposed device are tabulated in Table 4.

4. Conclusion:

In this paper we have designed and simulated a new structure of GaAsP/6H-SiC/GaN Power metal semiconductor field effect transistor with undoped region under gate using Silvaco ATLAS in 10nm technology .Gallium Nitride(GaN),Silicon Carbide(SiC) and Gallium arsenide Phospide has good potential to attract next generation semiconductors at high power and high frequency applications. The drain current characteristics and analog characteristics of a new undoped gate GaAsP/6H-SiC/GaN MESFET have been analyzed and it has increase oncurrent, Transconductance, drainconductance, gain and I_{on}/I_{off} ratio by factor of 33%. It can conclude that the proposed structure improves both characteristics. Consequently this device is suitable at high power applications.

Declarations

Acknowledgements The authors would like thank National institute of Technology Silchar for providing necessary computational tools

Author's Contributions Author 1 (Balaji B) studied the basic types of MESFET and simulation. Author 2 (K.Srinivasa Rao) analyzed the undoped MESFET and wrote paper. Author 3 (M.Aditya) carried out drain current characteristics. Author 4 (K.Girija Sravani) simulated analog parameters and wrote paper.

Availability of data The referred papers will be available on request.

Declarations:

Funding Not Applicable

Conflict of Interest Authors declare no conflict of Interest.

Ethics Approval The authors declare that they have no known competing financial interest or personal relationships that could have appeared to influence the work reported in this paper.

Consent to participate All authors voluntarily agree to participate in this paper.

Consent for Publication All authors give the permission to the Journal to publish this paper

References

[1] Akshay Kumar Ravirala, Leela Koteswari Bethapudi, Jeevani Kommareddy, Bhanu Sai Thommandru, Sateesh Jasti, Prakash Raju Gorantla, Ashok Puli, Girija Sravani Karumuri, Srinivasa Rao Karumuri, ―Design and performance analysis of uniform meander structured RF MEMS capacitive shunt switch along with perforations, Microsystem Technologies, Volume 24, Issue 2, pp 901–908, DOI: 10.1007/s00542-017-3403-z, Feb. 2018.

[2] P. Ashok Kumar, K. Girija Sravani, B. V. S. Sailaja, K. V. Vineetha, Koushik Guha, K. Srinivasa Rao, ―Performance analysis of series: shunt configuration based RF MEMS switch for satellite communication applications‖, Microsystem Technologies, Volume 24, Issue 12, pp 4909–4920, to be published, Dec. 2018, DOI: 10.1007/s00542-018-3907-1.

[3] K. Srinivasa Rao, P. Ashok Kumar, Koushik Guha, B. V. S. Sailaja, K. V. Vineetha, K. L. Baishnab, K. Girija Sravani, ―Design and simulation of fixed–fixed flexure type RF MEMS switch for reconfigurable antenna‖, Microsystem Technologies, to be published, https://doi.org/10.1007/s00542-018-3983-2.

[4] K. Girija Sravani, Koushik Guha, K Srinivasa Rao, Ameen Elsinawi, ―Design of a novel structure capacitive RF MEMS switch to improve performance parameters, IET Circuits, Devices & Systems. 2019 Jul 12;13(7):1093-101.

[5] Girija Sravani, K., Koushik Guha, and K. Srinivasa Rao. "A modified proposed capacitance model for step structure capacitive RF MEMS switch by incorporating fringing field effects." *International Journal of Electronics* (2020): 1-22.

[6] Karumuri Srinivasa Rao, Thalluri Lakshmi Narayana, Koushik Guha & Sravani, Girija. (2018). Fabrication and Characterization of Capacitive RF MEMS Perforated Switch. IEEE Access. PP. 1-1. DOI:10.1109/ACCESS.2018.2883353.

[7] Thalluri, Lakshmi Narayana & Guha, Koushik & Karumuri, Srinivasa Rao & Prasad, G. & Sravani, Girija & Sastry, K. & Kanakala, Appala & Babu, P.. (2020). Perforated serpentine membrane with AlN as dielectric material shunt capacitive RF MEMS switch fabrication and characterization. Microsystem Technologies. 10.1007/s00542-020-04755-3.

[8] Sravani, K. Girija, D. Prathyusha, K. Srinivasa Rao, P. Ashok Kumar, G. Sai Lakshmi, Ch Gopi Chand, P. Naveena, Lakshmi Narayana Thalluri, and Koushik Guha. "Design and Performance Analysis of Low Pull-In Voltage of Dimple Type Capacitive RF MEMS Shunt Switch for Ka- Band." *IEEE Access* 7 (2019): 44471-44488.

[9] Vijaya Prasad K., Kishore P.V.V., Srinivasa Rao O. (2019), Skeleton based viewinvariant human action recognition using convolutional neural networks', Interna-tional Journal of Recent Technology and Engineering, 8(2), PP.4860-4867

[10] Maity R., Maity N.P., Srinivasa Rao K., Guha K., Baishya S. (2018) , _A newcompact analytical model of nanoelectromechanical systems-based capacitive micromachined ultrasonic transducers for pulse echo imaging',Journal of Computa-tional Electronics, 17 (3),PP. 1334- 1342

[11] Aditya M, I Veeraraghava Rao, B. Balaji, John Philip B, Ajay Nagendra N, S Vamsee Krishna." A Novel Low-Power 5th order Analog to Digital Converter for Biomedical Applications." IJITEE, ISSN: 2278-3075, Volume-8 Issue-7,PP: 217-220,May, 2019

[12] B. Balaji, M. Aditya, G. Adithya, M. Sai Priyanka, V. V. S. S. K. Ayyappa Vijay, K. Chandu. "Implementation of Low-Power 1-Bit Hybrid Full adder with Reduced Area." IJITEE, ISSN: 2278-3075, Volume-8 Issue-7,PP:61-64, May, 2019.

[13] B.Balaji, N Ajaynagendra, Erigela Radhamma, A Krishna Murthy, M Lakshmana Kumar."Design of Efficient 16 Bit Crc with Optimized Power and Area in Vlsi Circuits."IJITEE, ISSN: 2278-3075, Volume-8 Issue-8, PP: 87-91 June, 2019

[14] Naraiah, R., Balaji, B., Radhamma, E., Udutha, R."Delay Approximation Model for Prime Speed Interconnects in Current Mode." IJITEE, ISSN: 2278-3075, Volume-8. Issue-9, PP: 3090-3093, July 2019

[15] P.Ashok Kumar, K. Srinivasa Rao,K. Girija Sravani,B.Balaji,M. Aditya,KoushikGuha,Ameen Elsinawi." An Intensive Approach to Optimize Capacitive type RF MEMS Shunt Switch." DOI: 10.1016/j.mejo.2021.105050 Microelectronics Journal ,2021 ,pp. 105050

[16] Sudhakar Alluri,K. Mounika,B.Balaji. , D.Mamatha," A Novel Implementation of 4 Bit Parity Generator in 7nm Technology" ISSN: 0094-243X, Volume-2358 Issue-1 July, 2021,PP: 030002- 1-10 , https://doi.org/10.1063/5.0059329

[17].Sudhakar Alluri,B.Balaji,Ch.cury" Low power, high speed VLSI circuits in 16nm technology" ISSN: 0094-243X, Volume-2358 Issue-1 July, 2021,PP: 030001- 1-16 , https://doi.org/10.1063/5.0060101

[18] Sravani, K.G., Guha, K., Aditya, M. et al. "Design, simulation and analysis of uniform and non-uniform serpentine step structure RF MEMS switch". Microsystem Technol (2021). https://doi.org/10.1007/s00542-021-05216-1

[19]Kumar, P.A., Rao, K.S., Balaji, B. et al. "Low Pull-in-Voltage RF-MEMS Shunt Switch for 5G Millimeter Wave Applications". Trans. Electr. Electron. Mater. (2021). https://doi.org/10.1007/s42341-021-00304-5

[20] Sudhakar Alluri,K. Mounika,B.Balaji. , D.Mamatha," Optimization of multiplexer architecture in VLSI circuits" ISSN: 0094-243X, Volume-2358 Issue-1 July, 2021,PP: 040004- 1-19 , https://doi.org/10.1063/5.0059332

[21] Aditya, M., Rao, K.S., Sravani, K.G. et al. Simulation and Drain Current Performance analysis of High-K Gate Dielectric FinFET. Silicon (2021). https://doi.org/10.1007/s12633-021-01176-3

[22] Aditya, M., Rao, K.S. Design and Performance Analysis of Advanced MOSFET Structures. Trans. Electr. Electron. Mater. (2021). https://doi.org/10.1007/s42341-021-00338-9

[23] Aditya, M., Srinivasa Rao, K., Sravani, K., Guha, K. (2021). 'Design, simulation and analysis of high-K gate dielectric FinField effect transistor', International Journal of Nano Dimension, 12(3), pp. 305-309. doi: 10.22034/ijnd.2021.681554

Figures

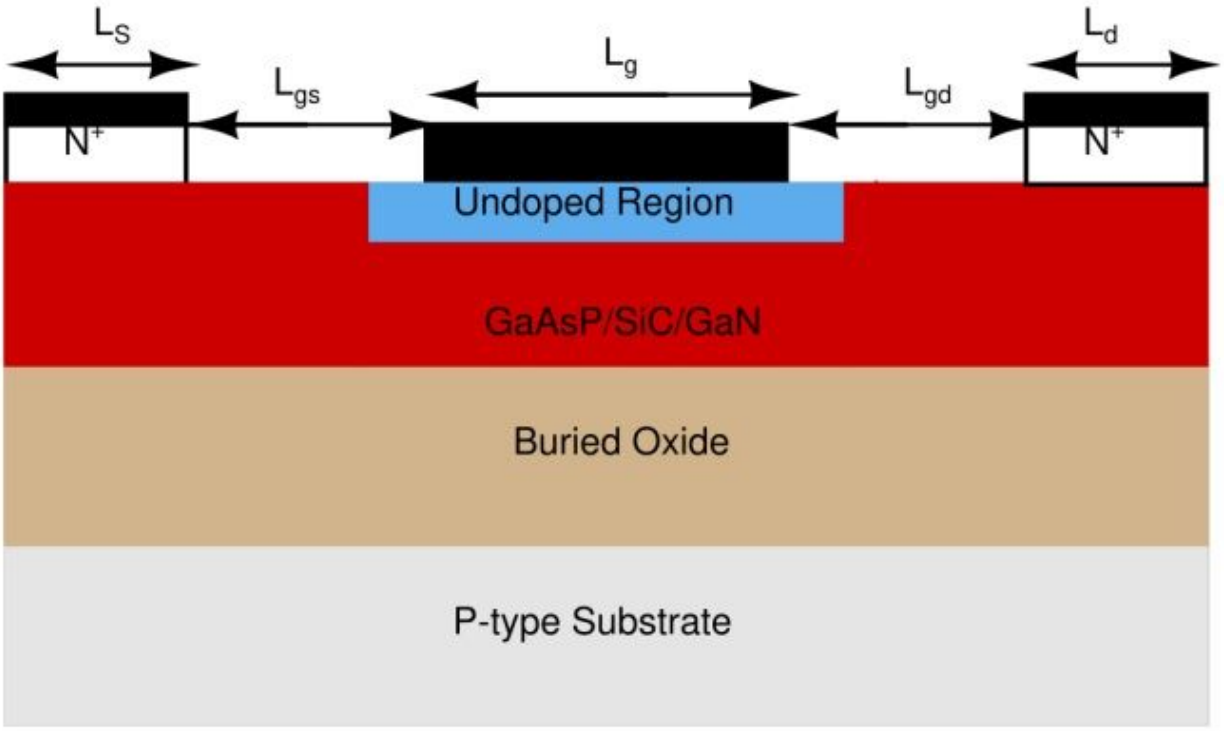

Figure 1

Structure of proposed U-MESFET

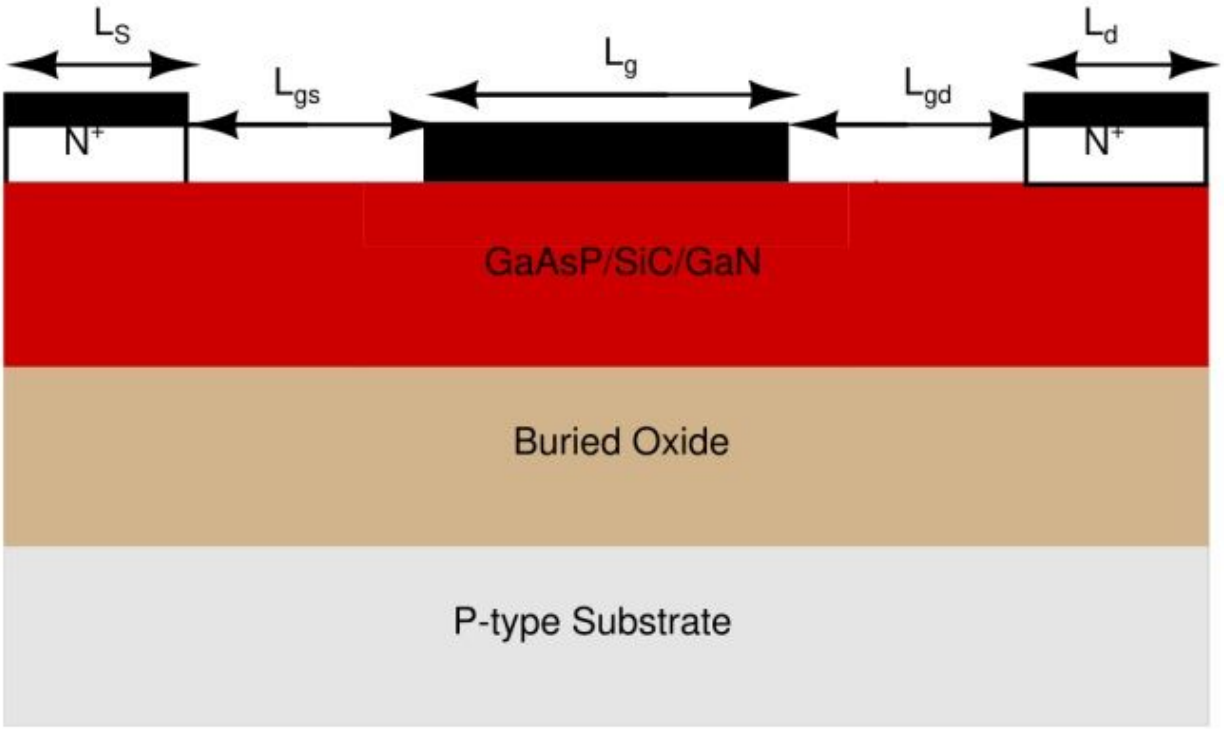

Figure 2

Structure of conventional MESFET

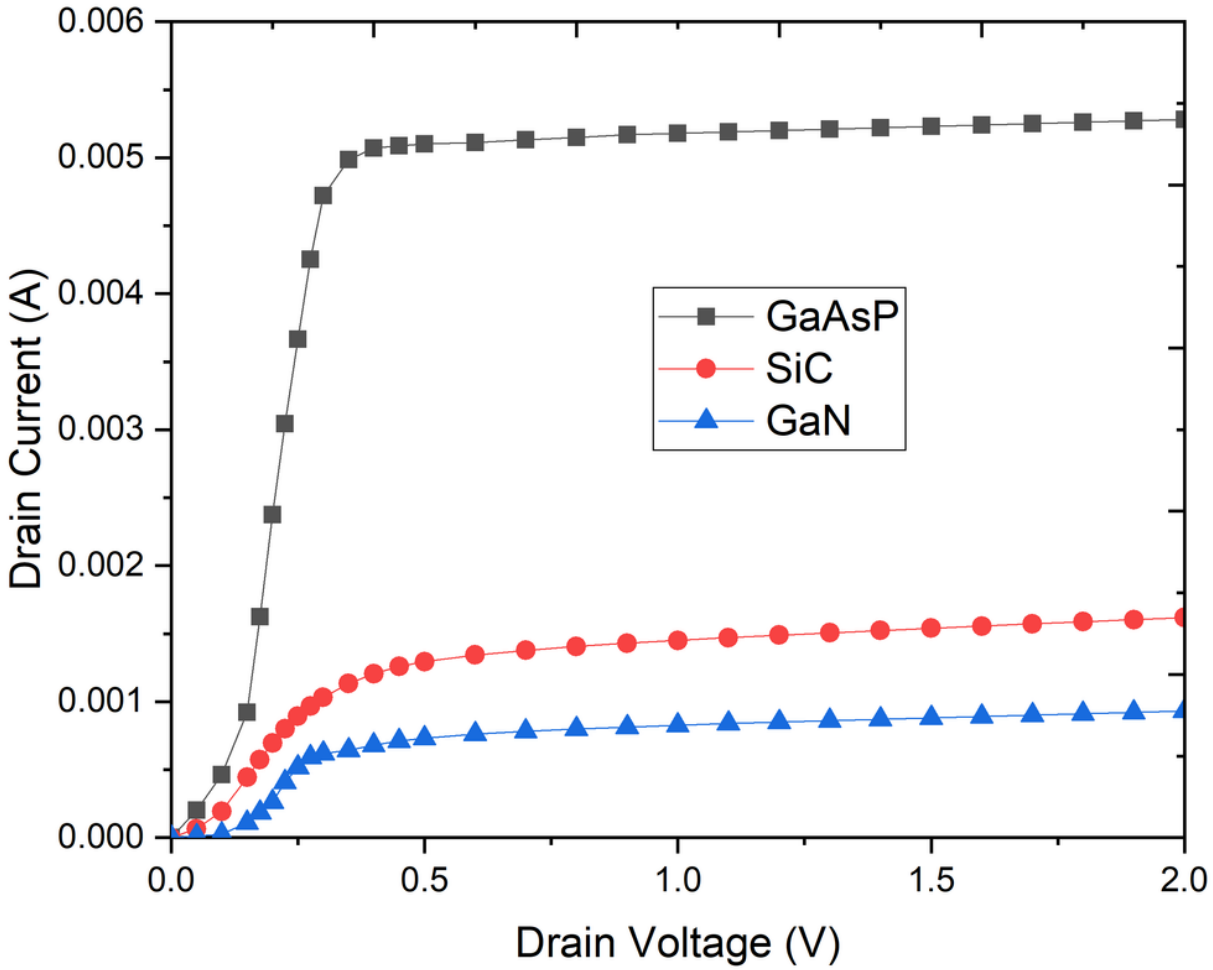

Figure 3

Ids VS Vds for GaAsP/SiC/GaN structure

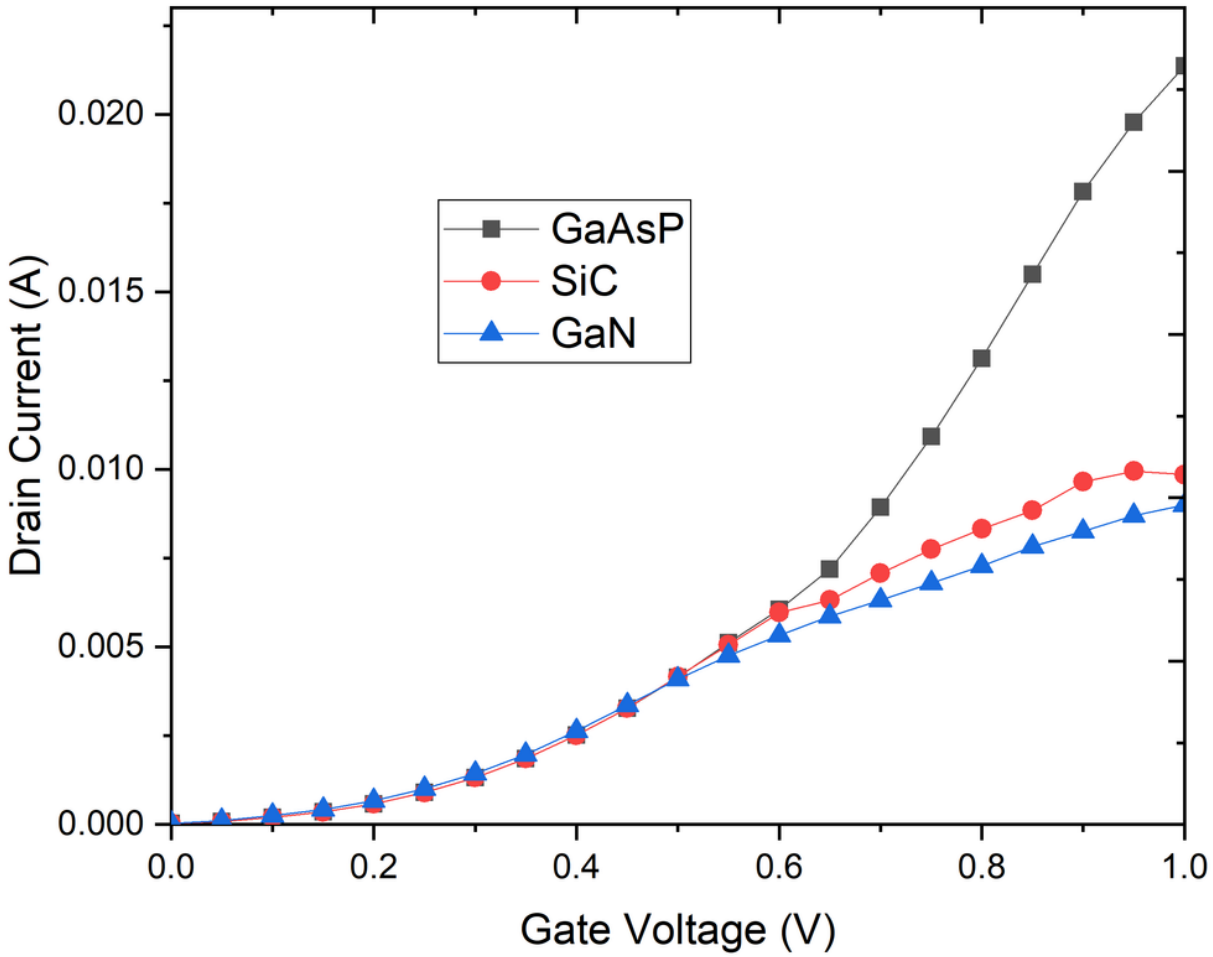

Figure 4

Ids VS Vgs for GaAsP/SiC/GaN structure

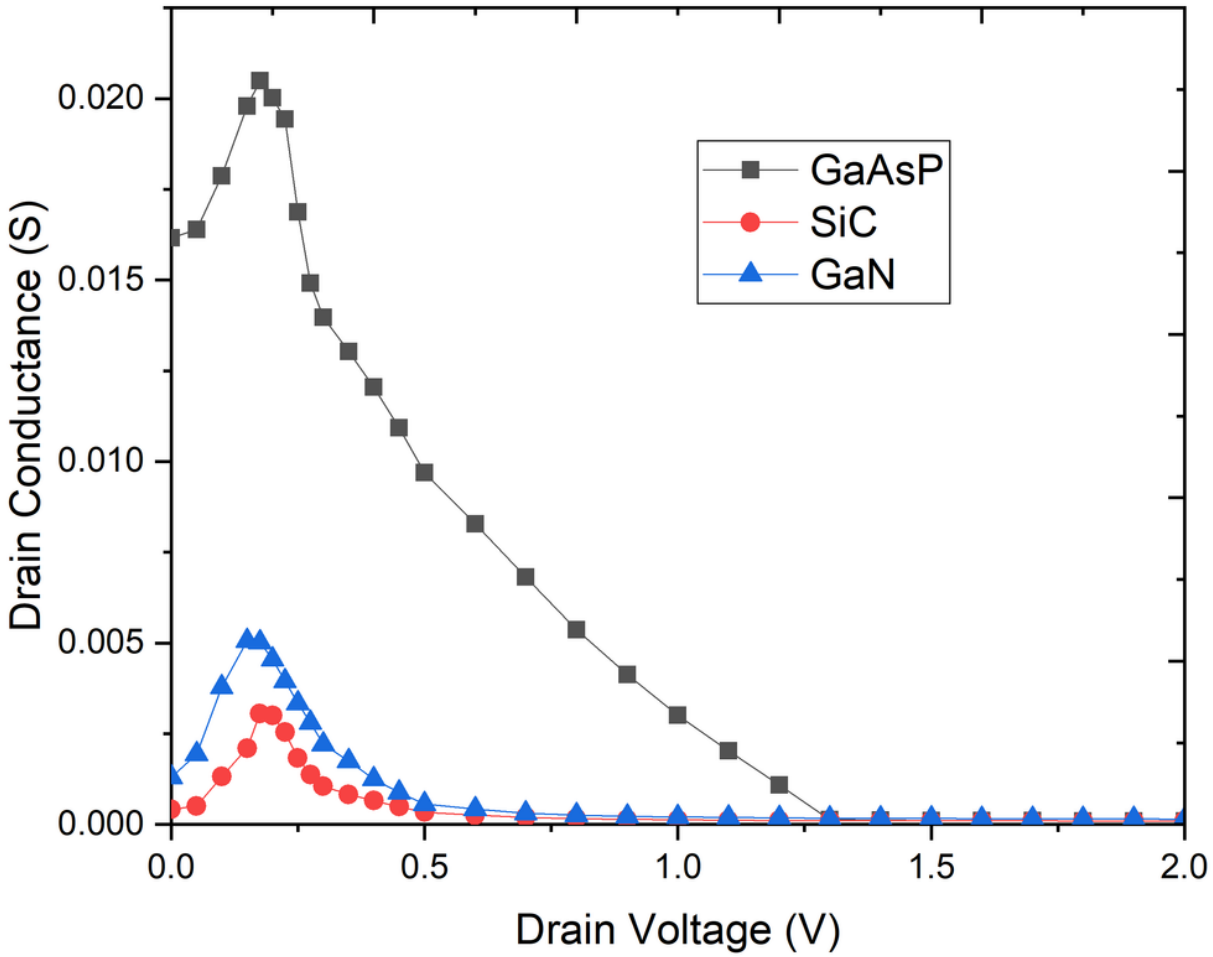

Figure 5

Gd VS Vds for GaAsP/SiC/GaN structure

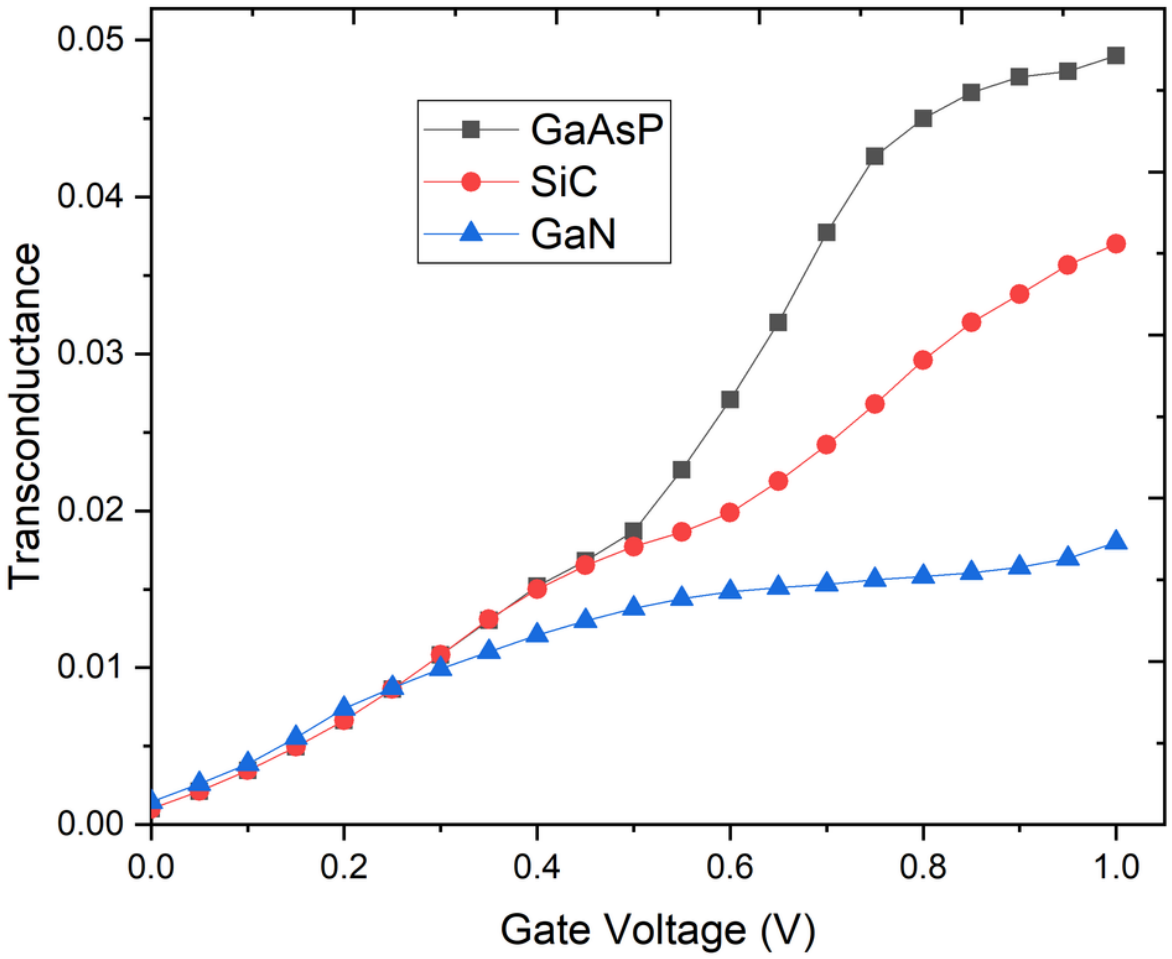

Figure 6

Gm VS Vgs for GaAsP/SiC/GaN structure

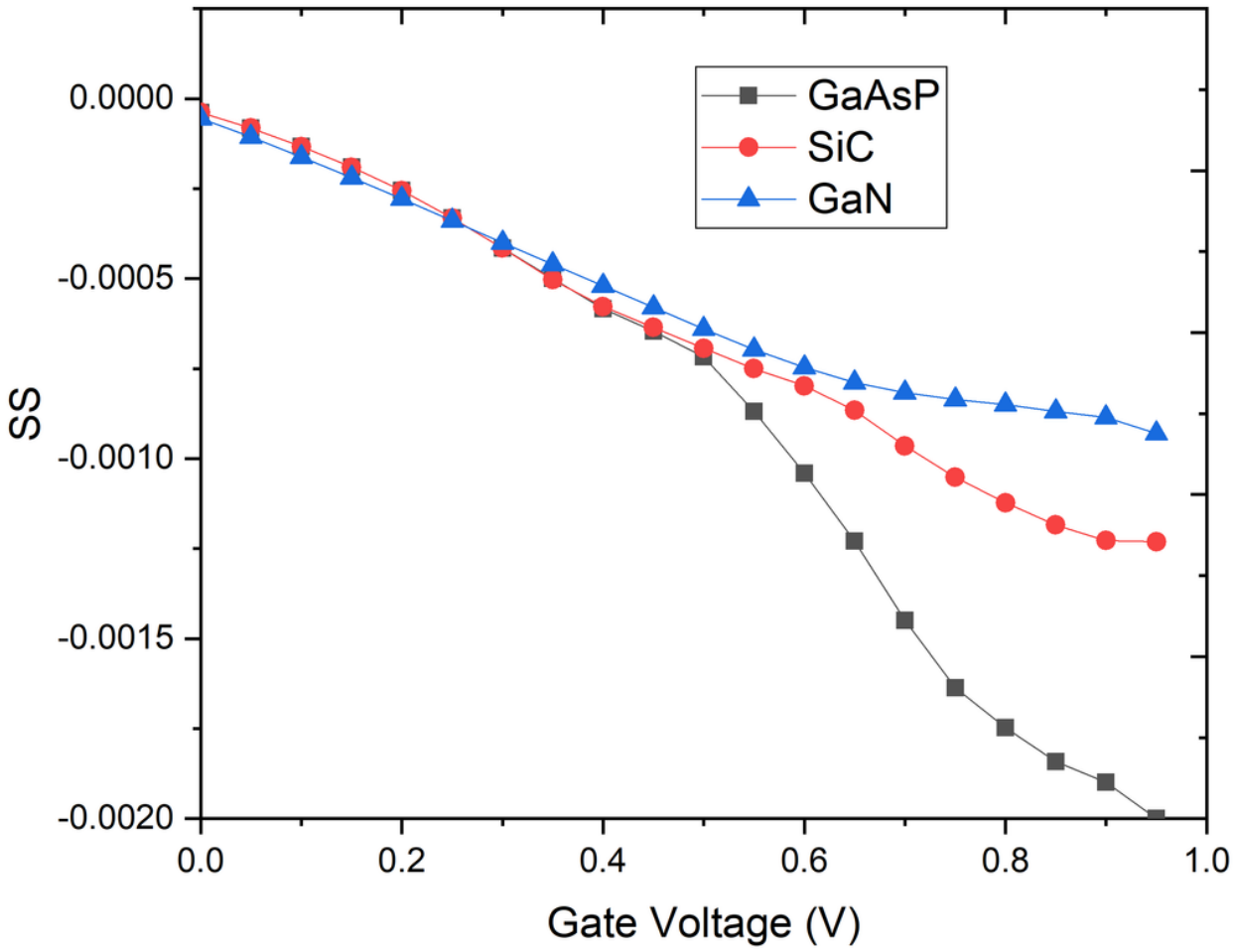

Figure 7

SS VS Vgs for GaAsP/SiC/GaN structure

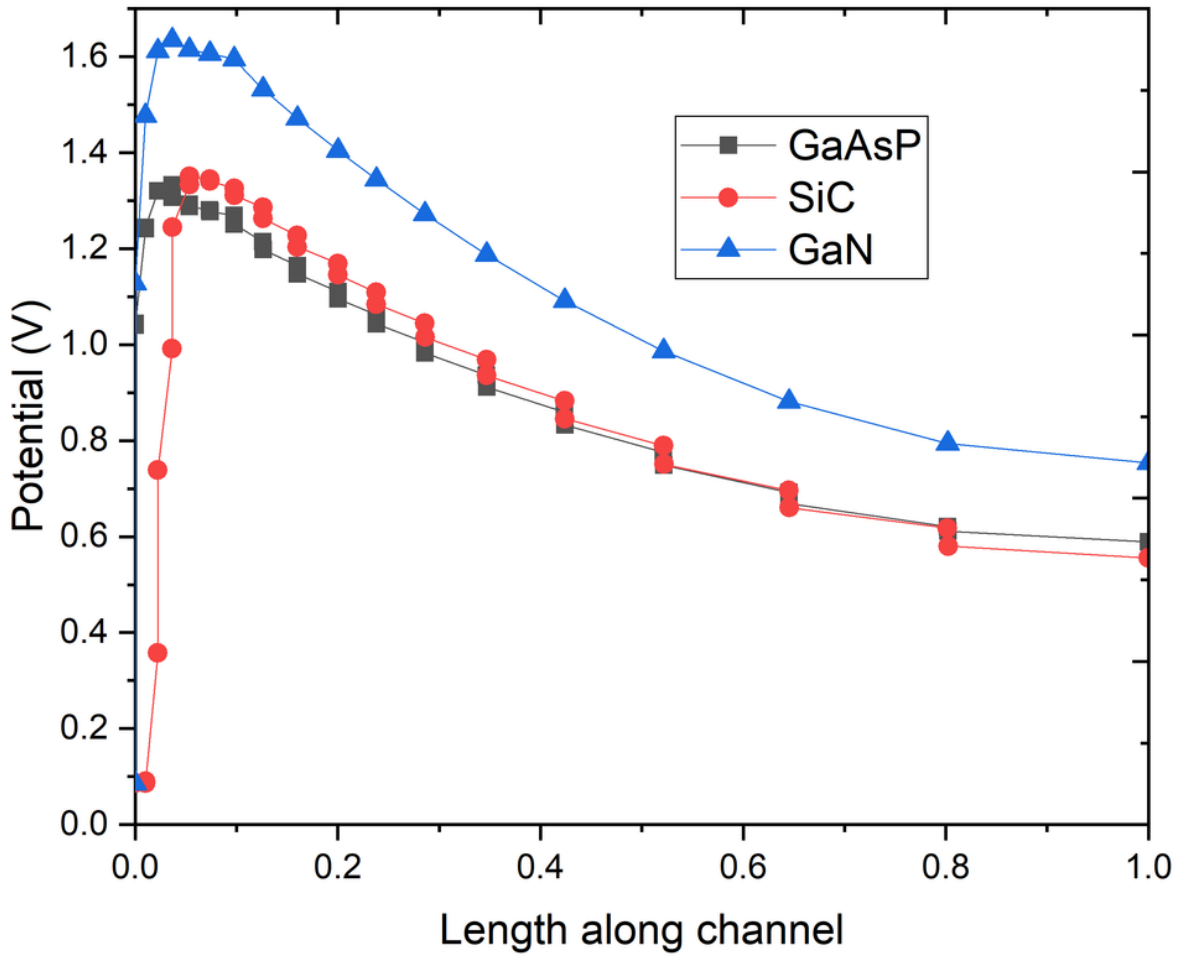

Figure 8

Potential Vs channel length for proposed structure