

Effect of Cooling Rate During Thermal Processes on the Electrical Properties of Cast Multi-Crystalline Silicon

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Abstract

Photoluminescence (PL) imaging techniques and the minority carrier lifetime test system were employed to investigate the variation of the interstitial iron (Fe_i) concentration, the recombination activity of structural defects and the minority carrier lifetime of cast multicrystalline silicon (mc-Si) in response to the cooling rate after heating. The results showed that when the mc-Si wafers are heated to high-temperature (1000 °C) and then cooled to ambient temperature with different cooling rate, the Fe_i concentration, the number of recombination active dislocations and grain boundaries increased as the cooling rate rises while the minority carrier lifetime decreased. If cast mc-Si is heated followed by faster cooling at 30 °C/s, the Fe_i concentration increase by 223% and the electrical activity of grain boundaries, dislocations and intragrain increase significantly, that is to say, the whole wafer is heavily contaminated with metal impurities, and present extremely low minority carrier lifetime.

1. Introduction

The cast multicrystalline silicon (mc-Si) was once considered to be one of main materials for fabrication of solar cells due to its low production cost. However, large amount of structural defects and higher contents of metallic impurities in mc-Si result in lower cell efficiency^[1-3], which limits its application in solar cells. In recent years, as the production cost of monocrystalline silicon (mono-Si) has decreased year by year, the dominant position of cast mc-Si in photovoltaic cell materials has been gradually replaced by mono-Si, and its share in the photovoltaic market has been declining^[4]. In order to reduce/eliminate the undesired effects and narrow the photovoltaic performances gap between mc-Si and mono-Si, take advantages of cast mc-Si in production cost again, it is important to understand the effects of metal impurities and structural defects on the electrical properties of cast mc-Si.

The influence of metal impurities and structural defects on the electrical properties of cast mc-Si wafer mainly occurs during the thermal processes in solar cells fabrication. A lot of researches show that during thermal process the minority carrier lifetime of mc-Si will decrease after heating at high temperature and then cooling at a fast rate^[5-7]. Our previous studies indicates that the minority carrier lifetime decreases with increase of cooling rate, which is referred to as thermally-induced degradation (TID) of minority carrier lifetime^[8,9]. It means that the photoelectric transformation efficiency of solar cell will be reduced potentially during the thermal processes of silicon wafer-based solar cells fabrication, such as phosphorus diffusing, annealing and electrode sintering processes. It is generally considered that the effects of the TID of minority carrier lifetime is due to the generation of smaller and more dispersed recombination centers^[5-7], substitutional boron and other Fe-related defects^[10,11] during high temperature heating and fast cooling processes. There are many structural defects such as grain boundaries and dislocations in cast mc-Si. However, what is the effect of these defects on the TID of minority carrier lifetime? Is there any interaction between defects and metal impurities during the cooling of the thermal process, and will this interaction affect the electrical properties of the cast mc-Si? These issues are not clear and have not been reported.

To further assess the role of metallic impurities and structural defects in decreasing cast mc-Si materials performance after thermal processes, the photoluminescence (PL) imaging techniques and the minority carrier lifetime test system were used to investigate the variation of the electroactivity of structural defects and Fe_i concentration in response to the cooling rate after heating.

2. Experiments Methods

Three p-type sister wafers (156 mm×156 mm) of cast mc-Si, i.e., adjacent vertical slices of the ingot, possessing virtually identical initial crystal structure and chemical component, with resistivity ranging from 1 to 3 $\Omega\cdot\text{cm}$ and thickness of 180 μm were selected for this analysis. The total Fe concentration (including Fe_i and Fe in precipitations) of these wafers measured in the same batch of wafer by inductively coupled plasma mass spectrometry (ICP-MS) is $3.9\times 10^{14}\text{ cm}^{-3}$.

The first wafer was left unprocessed and used as reference. The second and the third wafers were processed at 1000°C for 30 minutes in a controlled atmosphere furnace under argon atmosphere. Then the second wafer was slow cooled at 0.05 °C/s and the third was fast cooled at 30 °C/s to room temperature. The two heat treated wafers were soaked in 10 wt.% HF solution to remove the oxide layer on the surface, washed with deionized water and then dried with nitrogen.

The minority carrier lifetime was measured with the microwave-induced photoconductive decay ($\mu\text{-PCD}$) method, and the Fe_i concentration was evaluated with different lifetime measurement techniques^[3, 12, 13]. the Fe_i concentration [Fe_i] can be found via measurement of the carrier lifetime before and after breaking Fe_iB pairs in a boron doped p-type silicon sample. The iron concentration is determined by

$$[Fe_i] = C_{\mu\text{-PCD}} \left(\frac{1}{\tau_{\text{before}}} - \frac{1}{\tau_{\text{after}}} \right)$$

where τ_{before} and τ_{after} are the lifetimes measured before and after breaking the Fe_iB pairs. The conversion factor $C_{\mu\text{-PCD}}$ depends on the the injection level and capture cross sections of the Fe_i and Fe_iB states and the doping concentration, here is $3.4E13\ \mu\text{s}/\text{cm}^3$ by user manual suggestions according to the injection level when the minority carrier life is measured^[13].

The photoluminescence imaging was taken by PLI-1001A tester to assess the recombination activity of structure defects, including grain boundaries and dislocations. After that, the samples were dipped in an acid mixture solution ($\text{HF}:\text{HNO}_3 = 1:3$) in order to obtain a polished surface, and then the minority carrier lifetime was measured using a surface-passivation technique where wafers were immersed in a plastic bag filled with iodine of 0.08 mol/L to reduce the impact of surface recombination. In the end, the

samples were etched in a mixture solution (4.15wt%K₂Cr₂O₇ solution:HF: glacial acetic acid = 25:50:1), required for observing the dislocation on a metalloscope, and calculated the dislocation density by the Image Pro-Plus image processing and calculation software.

3. Results And Discussion

3.1. Effect of cooling rate on the interstitial iron concentration

Figure 1. shows the distribution mapping and average concentration of Fe_i in original wafer and its sister wafers after 1000 °C heating for 30 min, and cooling at 0.05 °C/s, and 30°C/s respectively.

The Fe_i concentration of the original wafer, the “slow cooling” (0.05 °C/s) wafer and the “fast cooling” (30 °C/s) wafer are $4.97 \times 10^{11} \text{ cm}^{-3}$, $1.05 \times 10^{12} \text{ cm}^{-3}$ and $1.60 \times 10^{12} \text{ cm}^{-3}$, respectively. Compared with the original wafer, the increase percentage of iron concentration is 112% for the “slow cooling” wafer and 223% for the “fast cooling” wafer, respectively. Each mc-Si wafer is cooling from the melt point temperature to room temperature at an extremely slow cooling rate during directional solidification process. So the original wafer could be considered as a sample with a slower cooling rate than those of the other two processed wafers. The results in Fig. 1 suggested that the Fe_i concentration increases as the cooling rate increases.

During high temperature heating, iron precipitates and complexes of all or part in silicon will be dissolved. According to the formula of solid solubility of iron in silicon^[14]: $5 \times 10^{22} \exp(8.2 - 2.94\text{eV}/k)$ ($900^\circ\text{C} < T < 1200^\circ\text{C}$), the solid solubility of iron in silicon at 1000°C is $4.1 \times 10^{14} \text{ cm}^{-3}$. The total iron content of the cast mc-Si wafer used is $3.9 \times 10^{14} \text{ cm}^{-3}$, indicating that all of iron precipitates and complexes in silicon will be dissolved during 1000°C heating. These iron atoms are released and distribute uniformly in silicon lattice. During the subsequent cooling, most of the iron atoms precipitate again, while the others do not and became Fe_i atoms^[8]. The faster the cooling rate, the shorter the time for diffusion and precipitation of iron atoms, and thus the fewer iron precipitates and the higher Fe_i concentration.

It is also found that the distribution mapping of Fe_i concentration in original wafer is about the same as that of the “slow cooling” wafer: iron concentration varies from grain to grain, and is uniform within each grain. Since each two-dimensional grain in Fig. 1 represents a specific crystal orientation, the above situation means that the iron atoms prefer to precipitate on some specific crystal planes when slowly cooled after heating. So far, no conclusion has been reached on which crystal planes iron atoms tend to gather in. In contrast, the distribution of Fe_i in the “fast cooling” wafer is not restricted by grain boundaries and tends to be uniform in silicon, which should be the reason that the fast cooling does not provide enough time for iron atoms to diffuse to the specific crystal planes.

3.2. Effect of cooling rate on the recombination activity of structural defects

Figure 2 shows the PL image of original wafer and its sister wafers after 1000°C heating for 30min, with 0.05 °C/s slow cooling and 30 °C/s fast cooling, respectively.

The color of purple and green are automatically painted by the equipment. The purple areas represent recombination active dislocations area which lifetime differ from the surrounding area by at least the lifetime value specified as “defect area limit” (0.35μs). It is the same with the green areas, representing recombination active grain boundaries area [15]. In the original wafer, as shown in Fig. 2 (a), the percentage of recombination active dislocations(the purple areas)and recombination active grain boundaries—the green areas—are both relatively low, 2.61% and 1.75% respectively, which indicated a good electrical activity of defects. In the “slow cooling” wafer, as shown in Fig. 2(b), the purple and green areas increase significantly, and the percentages of recombination active dislocations and recombination active grain boundaries are 7.03% and 3.10%, respectively. Compared to the original wafer, they increase by 169% and 77%. It indicates that the recombination active dislocations and grain boundaries of the mc-Si wafers increase significantly after high temperature heating, even when the cooling is as slow as 0.05 °C/s.

Dislocations without metal decoration and grain boundaries without metal aggregation have no electrical activity, or very weak electrical activity. As thus they are not the recombination centers of charge carriers and do not affect the electrical properties of cast mc-Si [16–18]. If metals and other impurities gather and precipitate on dislocations or grain boundaries, new deep level centers will be formed on them, and their electrical activity and hence the electrical properties of silicon are related to the state of aggregation of metal impurities. Fine and dispersive precipitates/atomic aggregates reduce the diffusion length of minority carriers significantly [5, 6], and corresponding dislocations and the grain boundaries have a strong electrical activity.

When cast mc-Si is heated at high-temperature, metal precipitates are dissolved to an extent and metallic atoms are released and distribute in silicon crystal lattice uniformly. During cooling, according to the theory of solid solution, metal atoms would gather again and their state are associated with the undercooling of cooling process. Lower cooling rate means smaller undercooling, and metal atoms tend to gather in the grain boundaries and dislocations. In this case, nucleation rate is low and small number of nucleates grow into large size precipitates. Density of precipitates is low and exhibit low electrical activity, which is usually the case with the original wafer, where extremely slow cooling from high temperature to room temperature is involved after directional solidification. The PL image of original wafer is shown in Fig. 2 (a).

When the cooling rate after high temperature heating is faster, i.e., undercooling is larger, the metal atoms tend to gather uniformly within grains in addition to those on grain boundaries and dislocations, and nucleate with homogeneous nucleation method subsequently. Nucleation rate is high and large number

of nucleates appear in the system. Since the period for nucleates to grow is much limited, the resulting precipitates are small in size and high in density (number of precipitates per unit volume), which leads to a higher electrical activity. For “slow cooling” wafer, the cooling rate of 0.05 °C/s is still much higher than that after directional solidification, so the precipitates and atomic aggregations of metallic impurities are smaller and more dispersed than those in the original wafer, which shows a higher electrical activity of grain boundaries and dislocations. The PL image is shown in Fig. 2 (b).

Figure 2 (c) is the PL image of the cast mc-Si wafer after 1000°C heating with 30°C/s rate fast cooling. It can be seen that the purple and the green areas disappear, the whole silicon wafer, including grains, grain boundaries and dislocations, are all dark, the “dark area percent” defined as area of the wafer that has lower lifetime than the absolute limit specified as “dark limit” ($1\mu\text{s}$)^[15] is 100% (that of the original wafer and the “slow cooling” wafer are 0.23% and 1.48% respectively), indicating that the whole “fast cooling” wafer is contaminated by metallic impurities, and the whole crystalline silicon wafer has a high recombination activity. This is due to the 30°C/s rapid cooling after high temperature heating. In this case, vast majority of metal atoms in crystal nucleate in homogeneous way, and the nucleation rate is very high, more than 99% of the metal impurity distribute in grains, grain boundaries and dislocations in extremely small dispersion state of precipitations, less than 1% of the metal impurities are “frozen” down in the atomic state^[19], and also distribute in grains, grain boundaries and dislocations scatterly, the results make whole crystal recombination active area greatly increase. The lifetime difference between the structure defects of dislocations or grain boundaries and the surrounding area is less than “defect area limit”, so the purple and the green areas disappear and the PL image of the whole wafer are dark, and the “dark area percent” is 100%.

The cooling process may cause the dislocation multiplication and increase the recombination active dislocation. In order to discriminate the main reason of the increase of recombination active dislocation, the microstructure of the original wafer and the “slow cooling” wafer were observed and the average dislocation density of the 9 pairs corresponding positions in the same area on the original and “slow cooling” wafer were measured. Figure 3 shows the 6 position dislocation outcrops. Table 1 shows the contrast of dislocation density between the original wafer and its slow cooled sister wafer.

Table 1. Contrast of dislocation densities of the 9 pairs corresponding points of the original wafer and its sister wafer after 1000°C heating for 30 min and then cooling down at 0.05 °C/s rate.

Position	Dislocation density of original wafer (cm ⁻²)	Dislocation density of slower cooling wafer (cm ⁻²)	Rate of change (%)	Average rate of change (%)
1	5.67 × 10 ⁵	6.02 × 10 ⁵	+6.2	
2	4.85 × 10 ⁵	4.87 × 10 ⁵	+0.4	
3	1.73 × 10 ⁵	1.84 × 10 ⁵	+6.4	
4	5.31 × 10 ⁵	5.28 × 10 ⁵	-0.6	
5	2.29 × 10 ⁵	2.25 × 10 ⁵	-1.7	+3.5
6	3.84 × 10 ⁵	3.91 × 10 ⁵	+1.8	
7	7.91 × 10 ⁵	8.46 × 10 ⁵	+7.0	
8	6.27 × 10 ⁵	6.79 × 10 ⁵	+8.3	
9	4.52 × 10 ⁵	4.68 × 10 ⁵	+3.3	

Table 1 and Fig. 3 show that there is a slight increase in dislocation density of the cast mc-Si wafer after 1000 °C heating for 30 min and then cooling down at 0.05 °C/s rate (average increase of + 3.5%), which is far smaller than the increase of active dislocation area (169%). This further indicates that the increase of the recombination active dislocations is not mainly caused by the increase of dislocation density but by the contamination of metallic impurities.

3.3. Effect of cooling rate on the minority carrier lifetime

Figure 4 shows the minority carrier lifetime mapping of original wafer and its sister wafers after 1000 °C heating for 30 min, with 0.05 °C/s slow cooling and 30 °C/s fast cooling, respectively. The minority carrier lifetime of the original wafer, the “slow cooling” wafer and the “fast cooling” wafer are 46.3μs, 11.2μs, and 1.3μs, respectively. The result shows that the minority carrier lifetime decreases with increase of the cooling rate.

According to the experimental results, the reasons for the TID of minority carrier lifetime is explained as follows:(1)After high temperature heating, the iron precipitates in the cast mc-Si decompose and the Fe_i concentration are increased. Although the iron precipitation and Fe_i atoms are both deep level centers, the distribution of Fe_i atoms in the crystal is more dispersive, and this actually increases the spatial density of the deep level center in the silicon crystal; (2) Compared with the cooling process after directional solidification of the original cast mc-Si, the undercooling and the nucleation rate during the cooling after high temperature heating in this study is larger and the re-formed iron precipitate is finer and more dispersive. The result is that the spatial density of the deep level center in the silicon crystal is increased. Both the above two points can enhance recombination activity of the cast mc-Si, and minimize the diffusion length of the minority carriers. (3) The high temperature heating increases the recombination active grain boundaries and dislocations, which also reduces the diffusion length of minority carriers.

4. Conclusion

We studied the recombination activity of structural defects, variation of the Fe_i concentration and the minority carrier lifetime of cast mc-Si in response to the cooling rate after heating. The PL imaging and the minority carrier lifetime test showed that the Fe_i concentration, the electrical activity were higher and the minority carrier lifetime was lower in the silicon wafers which is heated at 1000°C for 30 min and cooled to room temperature than those in the original silicon wafer. When the cast mc-Si wafer was heated at 1000 °C for 30 min followed by slow cooling at 0.05°C/s the Fe_i concentration, the recombination active dislocations and the recombination active grain boundaries increased by 112%, 169% and 77%, respectively. And the minority carrier lifetime decreased by 76%. When the cooling process at 30°C/s rate, the Fe_i concentration increased by 223% and the electrical activity of the whole cast mc-Si increased significantly. The experimental results also showed that the increase of recombination active dislocations after heating was not caused by the increase of dislocation density, which is considered to be caused by contamination of dislocation by metal impurities.

Declarations

Ethics approval

This manuscript has not been published or presented elsewhere in part or in entirety and is not under consideration by another journal. We have read and understood your journal's policies, and we believe that neither the manuscript nor the study violates any of these. There is no plagiarism or copyright dispute in this manuscript.

Consent to participate

All of our authors understand that my participation is entirely voluntary and that we can withdraw from the study at any time without giving an explanation and with no disbenefit. We understand who will have access to my data, how it will be stored, in what form it will be shared, and what will happen to it at the end of the study.

Consent for publication

All of our authors confirm that the work described has not been published before, and it is not under consideration for publication elsewhere. We all agree to publish in the esteemed journal "Silicon".

Availability of data and materials

All data generated or analysed during this study are included in this published article (and its supplementary information files).

Competing interests

All authors certify that they have no affiliations with or involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript.

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Authors' contributions

All the authors contributed to the manuscript. Panbing Zhou: Conceptualization, Methodology, Writing - Original Draft, Validation. Naigen Zhou: Writing- Reviewing and Editing, Formal analysis, Data curation. Shilong Liu: Investigation, Validation. Xiuqin Wei: Writing - Review and Editing. Lang Zhou: Resources, Supervision, Project administration.

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Disclosure of potential conflicts of interest

All authors have no potential conflicts of interest to declare that are relevant to the content of this article.

Research involving Human Participants and/or Animals

Not applicable.

Informed consent

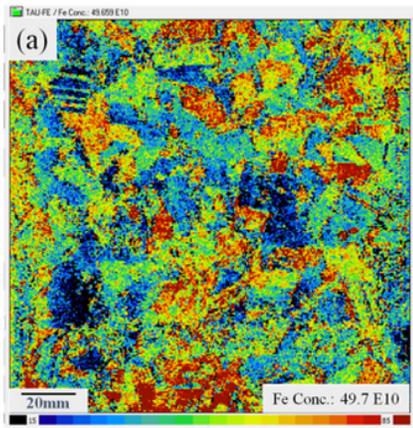
Not applicable.

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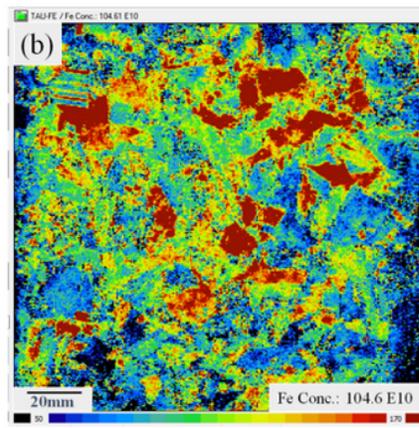
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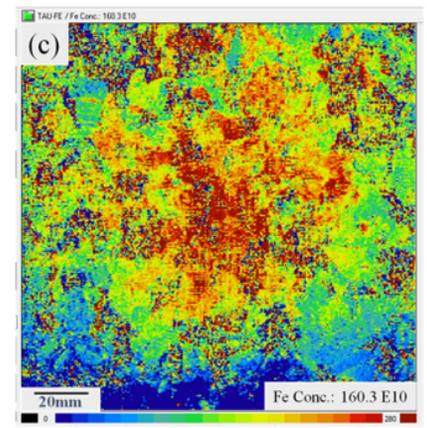
Figures



(a) original wafer



(b) 0.05 °C/s cooling rate



(c) 30 °C/s cooling rate

Figure 1

The concentration mapping and average concentration of Fe in original wafer (a) and its sister wafers after 1000 °C heating for 30 min and then cooling at 0.05 °C/s (b) and 30 °C/s (c).

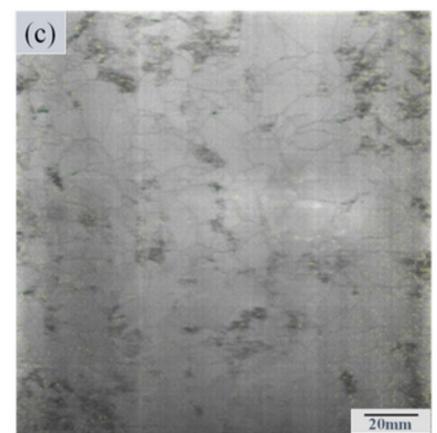
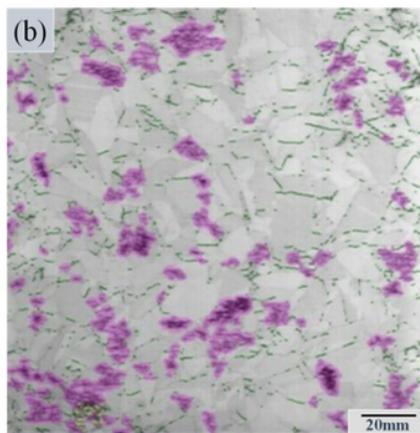
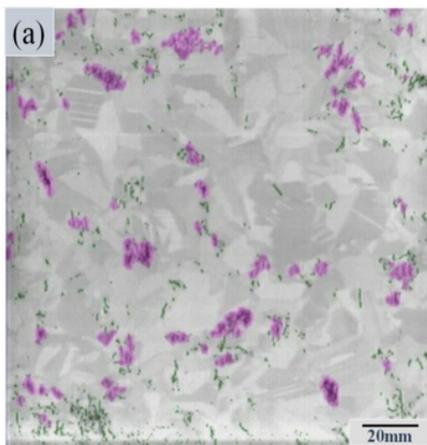


Figure 2

PL image of original wafer (a), and its sister wafers after 1000°C heating for 30 min and then cooling down at 0.05 °C/s rate (b) and 30 °C/s rate (c).

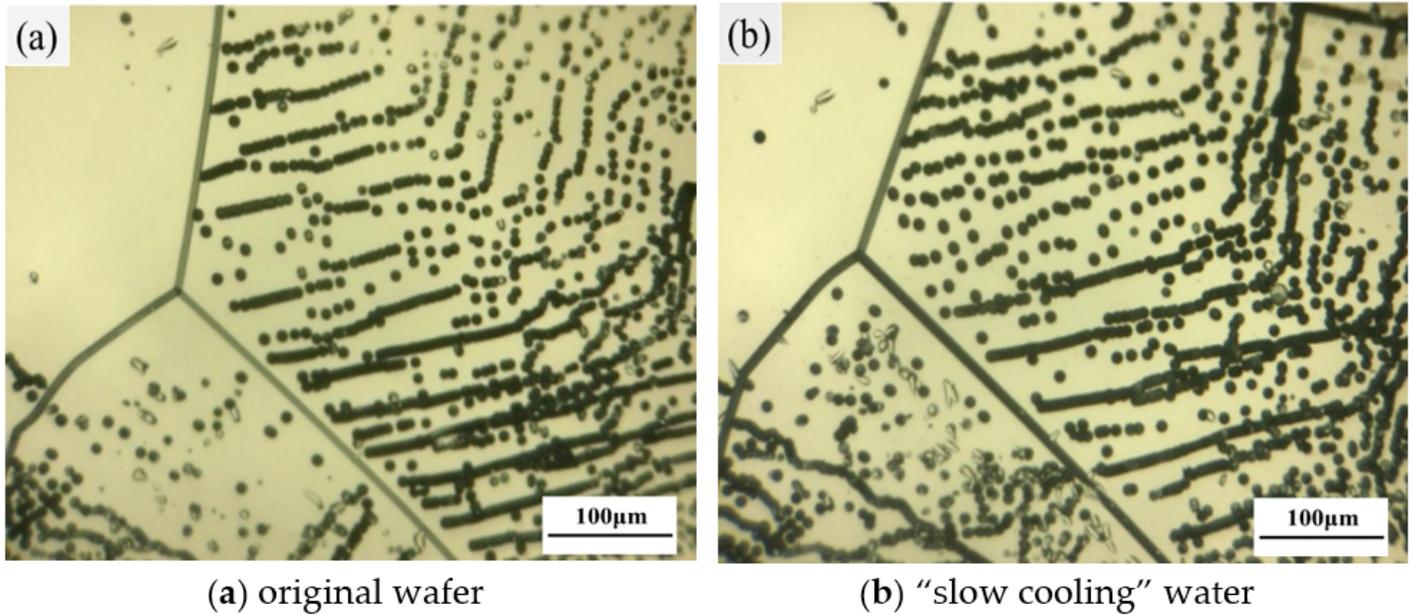


Figure 3

Dislocation etch pit images of original mc-Si wafer (a) and its sister wafer after 1000°C heating for 30 min and then cooling down at 0.05 °C/s rate (b).

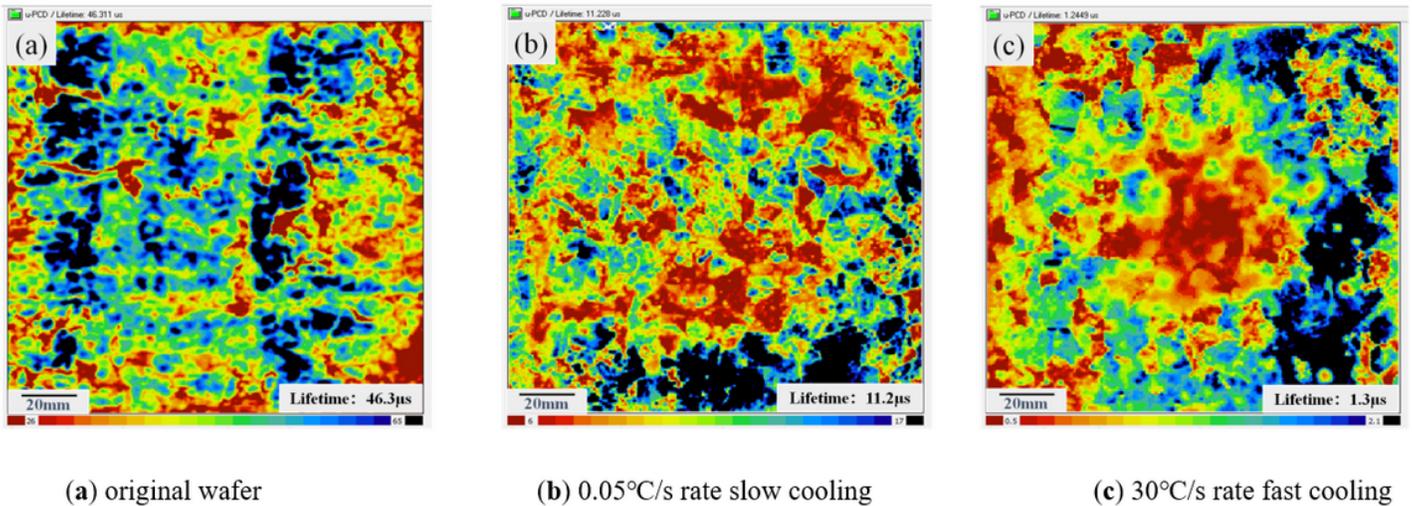


Figure 4

Minority carrier lifetime mapping and average lifetime of original wafer (a) and its sister wafers after 1000°C heating for 30 min with 3°C/min slow cooling (b) and 30°C/s fast cooling (c).