

Temperature Sensitivity Analysis of Dual Material Stack Gate Oxide Source Dielectric Pocket TFET

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Research Article

Keywords: Dielectric pocket, Temperature sensitivity, stack gate-oxide, Linearity

Posted Date: October 5th, 2021

DOI: <https://doi.org/10.21203/rs.3.rs-916159/v1>

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Received: date / Accepted: date

Abstract Temperature dependence performance variation is one of the major concerns in predicting the actual electrical characteristics of the device as the bandgap of semiconducting material varies with temperature. Therefore, in this article, for the first time the impact of temperature variations ranging from 300K to 450K on the DC, analog/ radio frequency, and linearity performance of dual material stack gate oxide-source dielectric pocket-tunnel-field-effect transistor (DMSGO-SDP-TFET) is investigated. In this regard, technology computer-aided design (TCAD) simulator is used to analyze DC, and analog/radio frequency performance parameters such as carrier concentration, energy band variation, electric field variation, $I_{DS} - V_{GS}$ characteristics, transconductance (g_m), cut off frequency (f_T), gain-bandwidth product (GBP), maximum oscillating frequency (f_{max}), transconductance frequency product (TFP), and transit time (τ) considering the impact of temperature variations. Furthermore, linearity parameters such as third-order transconductance (g_{m3}), third-order voltage intercept point (VIP3), third-order input-interception point (IIP3), and intermodulation distortion (IMD3) are also analyzed with temperature variations as these performance parameters are significant for linear and analog/radio frequency applications. Moreover, the performance of the proposed DMSGO-SDP-TFET is compared with the conventional dual-material stack gate oxide-tunnel-field-effect transistor (DMSGO-TFET). From the comparative analysis, in terms of % per kelvin, DMSGO-SDP-TFET demon-

strates lesser sensitivity towards temperature variation. Hence, the proposed DMSGO-SDP-TFET can be a suitable candidate for low power switching and analog/radio frequency applications at elevated temperatures as compared to conventional DMSGO-TFET.

Keywords Dielectric pocket · Temperature sensitivity · stack gate-oxide · Linearity

1 Introduction

To overcome the scaling issues of conventional MOSFETs, a tunnel field-effect transistor (TFET) based on the quantum tunneling mechanism has emerged as an alternative device to conventional MOSFETs due to lower subthreshold swing (SS) below 60 mV/decade, immunity to various short channel effects, and low OFF-state current (I_{OFF}) [1]-[8]. However, TFETs have been reported some major limitations such as ambipolar current, lower ON-state current (I_{ON}) and poor analog/radio frequency performance due inefficient band-to-band tunneling [9]. Therefore, to overcome the lower ON-state current issue, various methods have been reported by the researchers, such as double-gate TFET, work-function engineering, hetero-dielectric, stacked gate structure, electrically doped (ED), pocket doping, dielectric pocket, Extended Source TFET, dual material and gate over source overlap [9]-[22]. Furthermore, to address the ambipolar current issue, various methods have been reported such as, hetero-dielectric, work-function engineering, stacked gate structure, pocket doping, dual material gate [23]-[25]. In addition to the above issues, performance variation with temperature is also one of the major causes of concern in TFETs. Several studies [26]-[29] have reported temperature dependence performance of various TFET structures.

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In the previous work [21], to enhance the DC, analog/radio frequency performance of the device, authors have proposed DMSGO-SDP-TFET with optimized dielectric pocket at the source-channel junction and reported an improved performance in terms of higher ON-state current ($I_{ON} = 1.47 \times 10^{-4}$ A) at ($V_{GS} = V_{DS} = 1.0$ V), smaller point subthreshold swing (SS) = 15.7 mV/decade, maximum I_{ON}/I_{OFF} ratio (3.14×10^{12}), transconductance ($g_m = 1.02 \times 10^{-3}$ S), and cut-off frequency ($f_T = 193$ GHz). This motivated us to further investigate the reliability of the proposed device at different temperatures. For this, in this work, we investigate the temperature sensitivity of DMSGO-TFET and DMSGO-SDP-TFET in terms of DC characteristics, analog/radio frequency and linearity distortion performance parameters using TCAD simulations.

Remaining part of this paper is organised as follows. Section 2 presents the structural and simulation setup details. Section 3 describes the temperature sensitivity of DMSGO-TFET and DMSGO-SDP-TFET in three parts. The first part presents temperature sensitivity analysis of various DC parameters, second part investigates the analog/radio frequency performance and the third part presents the linearity and distortion performance at different temperatures. Finally, the main findings of this work are concluded in Section 4.

2 Device structure, parameters and simulation details

Figs. 1(a) and 1(b) illustrate the 2D structural views of conventional DMSGO-TFET and the proposed DMSGO-SDP-TFET for the parameters listed in Table 1. A stack gate oxide approach (low-k/high-k stack gate oxide i.e. SiO_2/HfO_2 stack) is used to provide better quality oxide/channel interface which enhances the ON-state current [29]. The entire length of the stack gate (L_G) is considered 50 nm with SiO_2 oxide layer thickness of (0.8 nm) and HfO_2 oxide layer thickness of (1.2 nm) [19]. Furthermore, the total gate length (L_G) of both devices is partitioned into three parts: tunneling gate (M_1), control gate (M_2), and auxiliary gate (M_3) with different length (L_1 , L_2 , L_3) and work function (ϕ_1 , ϕ_2 , ϕ_3), respectively. The control gate workfunction (ϕ_2) is considered 4.4 eV which corresponds to the metal molybdenum (Mo) (4.36 eV - 4.95 eV). The work functions (ϕ_1 and ϕ_3) are considered 4.0 eV which corresponds to metal aluminum (Al) (4.0 eV - 4.26 eV) [24]. The combination of stack gate oxide approach with workfunction engineering ($\phi_1 = \phi_3 = 4.0$ eV < $\phi_2 = 4.4$ eV) and dielectric pocket at the source-channel interface is used to enhance the ON-state current, reduce leakage current and improve the switching ratio.

The temperature sensitivity of the proposed DMSGO-SDP-TFET is analyzed using TCAD simulations. For this, suitable models are incorporated such as the non-local band-to-band tunneling (BTBT) model is considered to measure the tunneling probability across the junctions. Shockley-Read-Hall model is enabled to account the minority carrier recombination effect. Bandgap narrowing model is used to consider the band gap narrowing caused by high doping concentration. In our simulations, Quantum confinement effect is not taken into account as it is significant only if the thickness of the Si body is less than 10 nm.

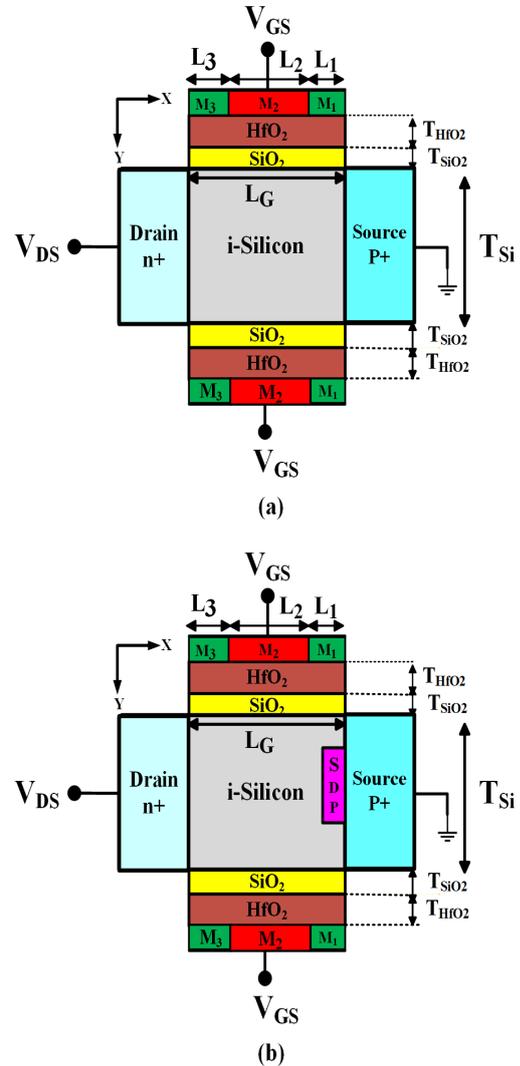


Fig. 1 2-D schematic view of (a) DMSGO-TFET and (b) DMSGO-SDP-TFET [21]

Table 1 List of device parameters

| Parameters | DMSGO-TFET | DMSGO-SDP-TFET |
|---|------------------------------------|------------------------------------|
| Gate Length (L_G) | 50 nm | 50 nm |
| SiO_2 thickness (T_{SiO_2}) | 0.8 nm | 0.8 nm |
| HfO_2 thickness (T_{HfO_2}) | 1.2 nm | 1.2 nm |
| Pocket thickness | - | 2 nm |
| Pocket height | - | 4 nm |
| Silicon Film Thickness (T_{Si}) | 10 nm | 10 nm |
| Channel doping (N_{ch}) | $1 \times 10^{17} \text{ cm}^{-3}$ | $1 \times 10^{17} \text{ cm}^{-3}$ |
| Source doping(p type) (N_S) | $1 \times 10^{20} \text{ cm}^{-3}$ | $1 \times 10^{20} \text{ cm}^{-3}$ |
| Drain doping(n type) (N_D) | $5 \times 10^{18} \text{ cm}^{-3}$ | $5 \times 10^{18} \text{ cm}^{-3}$ |
| HfO_2 dielectric constant (K) | 25 | 25 |
| Tunnel gate Length (L_1) | 10 nm | 10 nm |
| Control gate Length (L_2) | 25 nm | 25 nm |
| Auxiliary gate Length (L_3) | 15 nm | 15 nm |
| Tunnel gate workfunction(ϕ_1) | 4.0 eV | 4.0 eV |
| Control gate workfunction(ϕ_2) | 4.4 eV | 4.4 eV |
| Auxiliary gate workfunction(ϕ_3) | 4.0 eV | 4.0 eV |

3 Results and discussion

3.1 Temperature sensitivity analysis of DC Parameters

This section presents the comparative temperature sensitive performance analysis of conventional DMSGO-TFET and proposed DMSGO-SDP-TFET in terms of carrier concentration, energy band variation, electric field variation, $I_{DS}-V_{GS}$ characteristics, threshold voltage variation (V_T) and subthreshold swing variation at elevated temperatures ranging from 300K to 450K.

Figs. 2(a) and 2(b) depict the ON-state carrier concentration variation with temperature ranging from 300K to 450K for DMSGO-TFET and DMSGO-SDP-TFET, respectively. It is evident from these figures, due to stack gate oxide with lower work functions ($\phi_1 = \phi_3 = 4.0 \text{ eV}$), at the source (drain) junctions, electron (hole) concentration increases (decreases), respectively for both the devices. Moreover, as the temperature rises, the minority carrier concentration rises significantly, whereas the majority carrier concentration variation is negligible. Furthermore, DMSGO-SDP-TFET exhibits more abruptness in majority carrier concentration at the source-channel junction compared to conventional DMSGO-TFET.

To understand the BTBT process the energy band variation of DMSGO-TFET and DMSGO-SDP-TFET are illustrated in Figs. 2(c) and 2(d), respectively. The energy bandgap of the semiconductor material decreases as temperature increases, influencing device characteristics accordingly. The energy bandgap variation with temperature can be formulated using the equation [29],[31]

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \quad (1)$$

Where $E_g(T)$ represents energy band gap at absolute temperature T, $E_g(0)$ is the energy bandgap at T= 0 K, and α, β represents material specific fitting parameters. The ON-state energy band variation with temperature ranging from 300K to 450K for DMSGO-TFET and DMSGO-SDP-TFET are illustrated in Figs. 2(c) and 2(d), respectively. These results demonstrate that irrespective of temperature variations, a significant decrease in tunneling width is observed at the source junction for DMSGO-SDP-TFET, which increases band-to-band tunneling current for DMSGO-SDP-TFET as compared to conventional DMSGO-TFET. Furthermore, the impact of temperature variation is negligible in both devices.

Figs. 2(e) and 2(f) illustrate the ON-state electric field variation with temperature ranging from 300K to 450K for DMSGO-TFET and DMSGO-SDP-TFET, respectively. The above figures show that, with temperature variation, no significant change in the electric field has been noted for either device. Furthermore, results demonstrate that, inclusion of a low k dielectric pocket increases the electric field at the source junction for DMSGO-SDP-TFET compared to DMSGO-TFET.

Figs. 3(a) and 3(b) illustrate the effect of temperature variations on $I_{DS}-V_{GS}$ characteristics for DMSGO-TFET and DMSGO-SDP-TFET, respectively. These figures show a smaller I_{ON} variation with temperature for both devices because I_{ON} depends mainly on the band-to-band tunneling instead of temperature. However, the OFF-state current (I_{OFF}) varies significantly with temperature because of its dependence on minority carrier concentration, which increases with temperature. These results also demonstrate that the temperature dependence of DMSGO-SDP-TFET provides 0.23%/K change in I_{ON} . Whereas DMSGO-TFET pro-

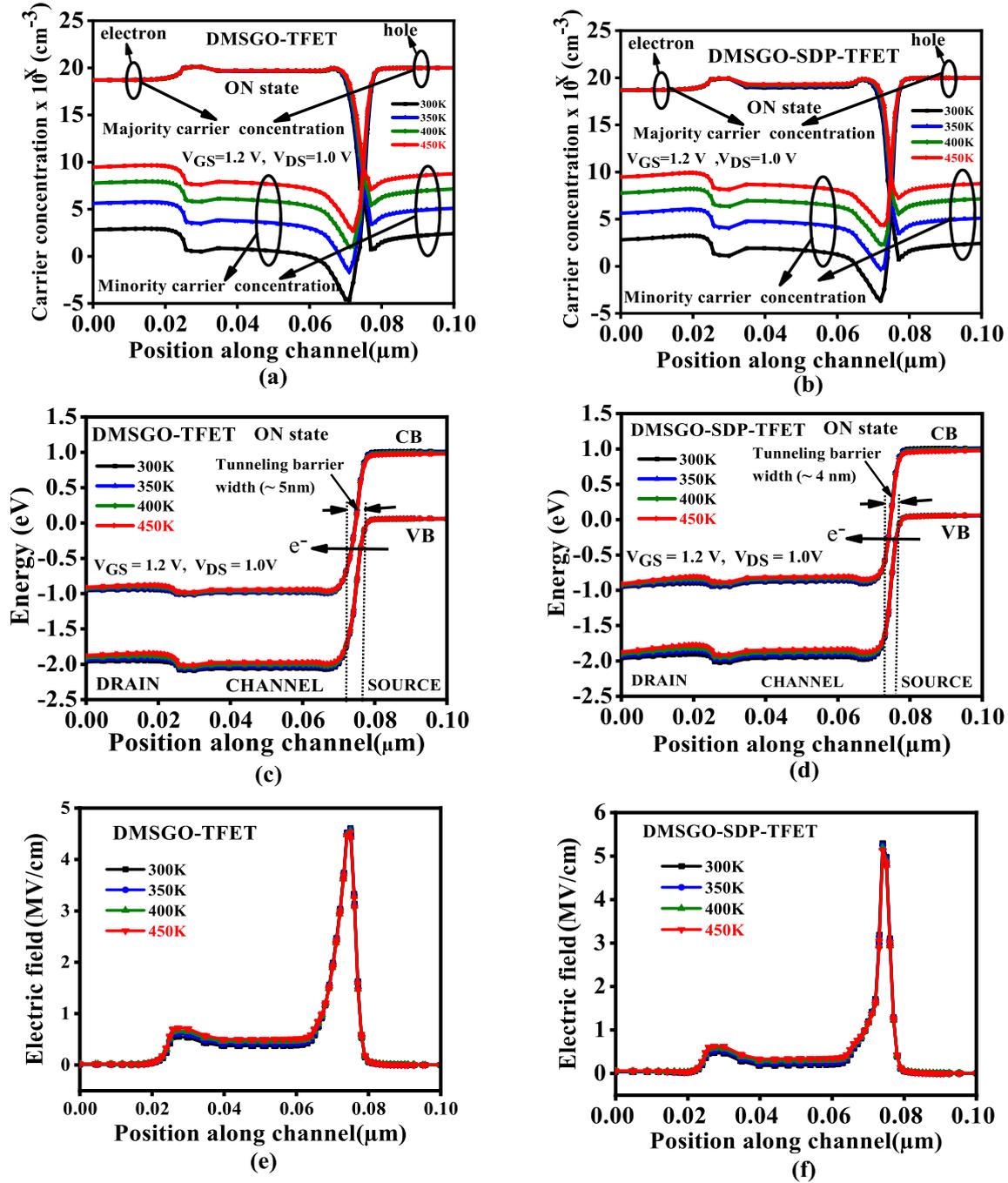


Fig. 2 Variation of carrier concentration with temperature for (a) DMSGO-TFET and (b) DMSGO-SDP-TFET, Variation of energy band with temperature for (c) DMSGO-TFET and (d) DMSGO-SDP-TFET, Variation of electric field with temperature for (e) DMSGO-TFET and (f) DMSGO-SDP-TFET.

vides 1.12%/K at $V_{GS} = 1.0$ V. Hence, the I_{ON} variation with temperature ranging from 300K to 450K is 0.89%/K lesser for the DMSGO-SDP-TFET as compared to DMSGO-TFET. This indicates that DMSGO-SDP-TFET is more resistant to temperature compared to DMSGO-TFET. Furthermore, because of the dielec-

tric pocket, DMSGO-SDP-TFET has a higher I_{ON} than DMSGO-TFET.

Fig. 4(a) illustrates the effect of temperature on V_T for DMSGO-TFET and DMSGO-SDP-TFET. The results reveal that, V_T decreases for both devices as temperature increases. Moreover, the temperature dependency of DMSGO-SDP-TFET exhibits 0.095%/K

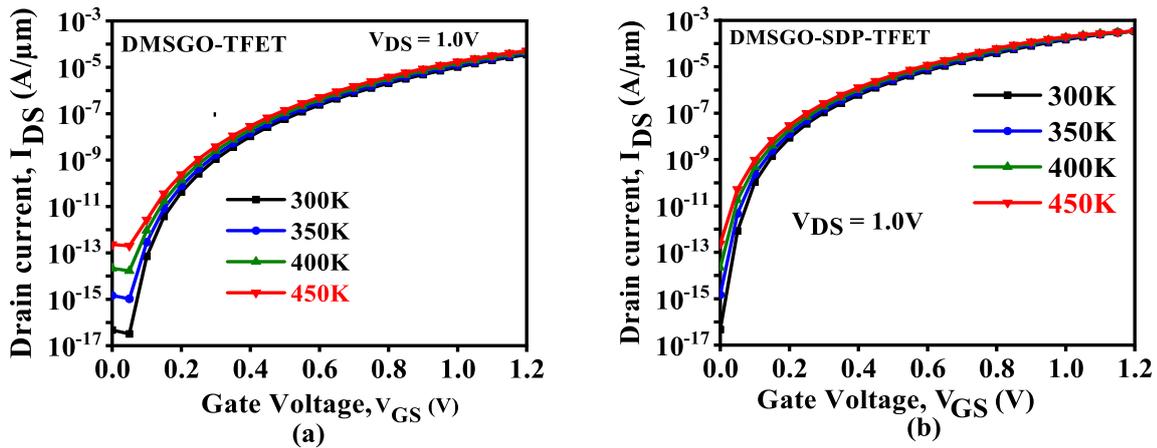


Fig. 3 Variation of $I_{DS} - V_{GS}$ characteristics with temperature for (a) DMSGO-TFET, (b) DMSGO-SDP-TFET.

change in V_T , whereas it exhibits 0.069 %/K change for DMSGO-TFET. Hence, the V_T variation with temperature ranging from 300K to 450K is 0.026 %/K higher for DMSGO-SDP-TFET compared to DMSGO-TFET. Hence, a substantial increase in drain current is observed at lower V_{GS} in the proposed DMSGO-SDP-TFET as shown in the transfer characteristics.

Fig. 4(b) illustrates the effect of temperature variation on the average subthreshold swing (SS_{AVG}) for DMSGO-TFET and DMSGO-SDP-TFET. The SS_{AVG} is formulated using the following expression [9].

$$SS_{AVG} = \frac{(V_T - V_{OFF})}{\log(I_{VT}) - \log(I_{OFF})} \quad (2)$$

The above figure show that SS_{AVG} for both devices increases as the temperature rises. Moreover, temperature dependency of DMSGO-SDP-TFET provides 0.28%/K change in SS_{AVG} , whereas it exhibits 0.32%/K change for DMSGO-TFET. Hence, SS_{AVG} variation with temperature ranging from 300K to 450K is 0.04%/K lower for DMSGO-SDP-TFET compared to DMSGO-TFET.

3.2 Temperature sensitivity analysis of analog/radio frequency performance

This section presents the temperature dependence of various analog/radio frequency performance parameters such as g_m , f_T , GBP, f_{max} , TFP, τ for conventional DMSGO-TFET and the proposed DMSGO-SDP-TFET.

The parasitic capacitances (C_{gs} and C_{gd}) are crucial parameters to analyze the analog/radio frequency and linearity performance of the device. In this regard, Figs. 5(a) and 5(b) illustrate the C_{gs} variation with V_{GS} at the temperature range from 300K to 450K for DMSGO-TFET and DMSGO-SDP-TFET, respectively. Similarly, Figs. 5(c) and 5(d) illustrate the C_{gd}

variation for both the devices, respectively. From these figures, temperature variations in C_{gs} and C_{gd} for both the devices are noted smaller at lower V_{GS} than higher V_{GS} .

Transconductance (g_m) is one of the most crucial parameters when evaluating a device for its analog/radio frequency and linearity performance. Therefore, higher g_m results in achieving higher gain, f_T and GBP in the design of analog circuits [30]. In this regard, Figs. 5(e) and 5(f) illustrate the g_m variation with temperature for DMSGO-TFET and DMSGO-SDP-TFET, respectively. It is evident from the results in the subthreshold region g_m of both the devices are very small and it starts increasing due to a steep rise in the ON-state current. However, it starts decreasing after a particular value of V_{GS} because of mobility degradation [32]. The results also reveal that, with increasing temperature, peak of g_m is shifted more towards lower V_{GS} in DMSGO-SDP-TFET which means that a lower V_{GS} is needed to achieve better analog/radio frequency performance as compared to DMSGO-TFET. Moreover, DMSGO-SDP-TFET exhibits 0.37%/K variation in g_m for temperature ranging from 300K to 450K at $V_{GS} = 0.75$ V, whereas for the same biasing conditions and temperature range DMSGO-TFET exhibits 0.55 %/K variation. Hence, g_m of DMSGO-SDP-TFET exhibits better immunity to temperature variations when compared to DMSGO-TFET. This indicates that the proposed device is appropriate for analog/radio frequency applications at higher temperatures.

Another critical parameter for evaluating the device's analog/radio frequency performance is the cutoff frequency (f_T). It is defined as the frequency at which current gain becomes 0 dB [28]. It is obtained using the expression $f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$. It can be noted that f_T depends on C_{gs} , C_{gd} and g_m of the device. Figs. 6(a)

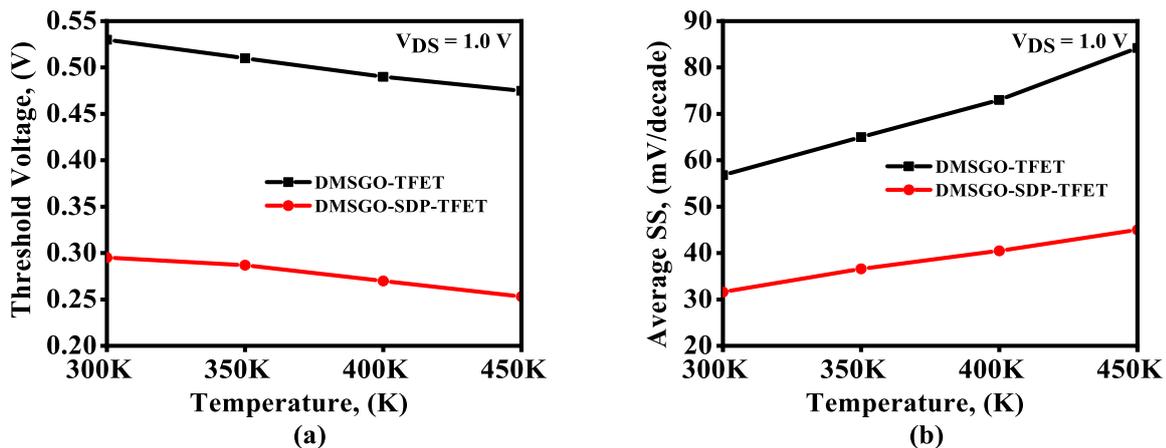


Fig. 4 (a) Comparative threshold voltage and (b) Average subthreshold swing variation with temperature for DMSGO-TFET and DMSGO-SDP-TFET

and 6(b) depict the variation in f_T with V_{GS} at temperatures ranging from 300K to 450K for DMSGO-TFET and DMSGO-SDP-TFET. As seen from Figs. 6(a) and 6(b), f_T initially increases with V_{GS} due to an increase in g_m and then decreases after a certain value of V_{GS} due to the increased parasitic capacitances and reduced g_m because of mobility degradation. The results also reveal that, with increasing temperature, peak of f_T is shifted more towards lower V_{GS} in DMSGO-SDP-TFET which means that a lower V_{GS} is needed to achieve better high frequency performance as compared to DMSGO-TFET. Moreover, DMSGO-SDP-TFET exhibits 0.19%/K variation in f_T for temperature range from 300K to 450K at $V_{GS} = 0.75$ V, whereas for the same biasing conditions and temperature range DMSGO-TFET exhibits 0.39 %/K variation. Hence, the proposed DMSGO-SDP-TFET exhibits better immunity and reliability to temperature variations for high-frequency applications at higher temperatures when compared to DMSGO-TFET.

The GBP is another important parameter for evaluating the analog/radio frequency performance of the device. It is formulated as $GBP = \frac{g_m}{20\pi C_{gd}}$. The GBP variations for DMSGO-TFET and DMSGO-SDP-TFET with V_{GS} at the temperature range from 300K to 450K, is shown in Figs. 7(a) and 7(b), respectively. The results reveal that, GBP of conventional DMSGO-TFET is inferior to DMSGO-SDP-TFET for the same reasons discussed earlier for the f_T . Further, it is evident from the results as the temperature increases, GBP starts decreasing in both the devices due to mobility degradation. Also, the mobility degradation observed at lower V_{GS} in DMSGO-SDP-TFET which means that a lower V_{GS} is needed to achieve higher GBP as compared to DMSGO-TFET. Therefore, before the mobility degradation i.e., at $V_{GS} = 0.75$ V and temperature

range from 300K to 450K, in terms of %/K variation DMSGO-TFET exhibits 0.27 %/K variation in GBP and DMSGO-SDP-TFET exhibits 0.09%/K. Hence, the proposed DMSGO-SDP-TFET shows better immunity to temperature variations compared to DMSGO-TFET.

Another crucial parameter for the analog/radio frequency performance evaluation of the device is the maximum oscillating frequency (f_{max}). It is obtained as $f_{max} = \sqrt{\frac{f_T}{8\pi C_{gd} R_{gd}}}$. Figs. 7(c) and 7(d) illustrate the f_{max} variation with V_{GS} at temperature ranges from 300K to 450K for DMSGO-TFET and DMSGO-SDP-TFET, respectively. It is evident from the results, due to higher f_T , f_{max} of DMSGO-SDP-TFET is greater than that of DMSGO-TFET. Furthermore, as temperature rises, f_{max} in both devices begins to fall due to a decrease in f_T caused by mobility degradation. Further, mobility degradation started at lower V_{GS} in DMSGO-SDP-TFET which means that a lower V_{GS} is needed to achieve higher f_{max} as compared to DMSGO-TFET. Therefore, before the mobility degradation i.e., at $V_{GS} = 0.75$ V, and temperature range from 300K to 450K, in terms of %/K variation for f_{max} , DMSGO-TFET exhibits 0.104 %/K variation and DMSGO-SDP-TFET exhibits 0.075%/K. Hence, the proposed DMSGO-SDP-TFET shows better immunity to temperature variations and exhibits better analog/radio frequency performance at lower V_{GS} and elevated temperatures compared to DMSGO-TFET.

TFP is also an important parameter to consider for high-frequency performance assessment of the device. It is formulated as $TFP = \left(\frac{g_m}{I_{DS}}\right) f_T$. Fig. 8(a) and 8(b) depict the TFP variation with temperature for DMSGO-TFET and DMSGO-SDP-TFET, respectively. It is evident from the results, for both devices, TFP increases linearly up to a certain value of V_{GS}

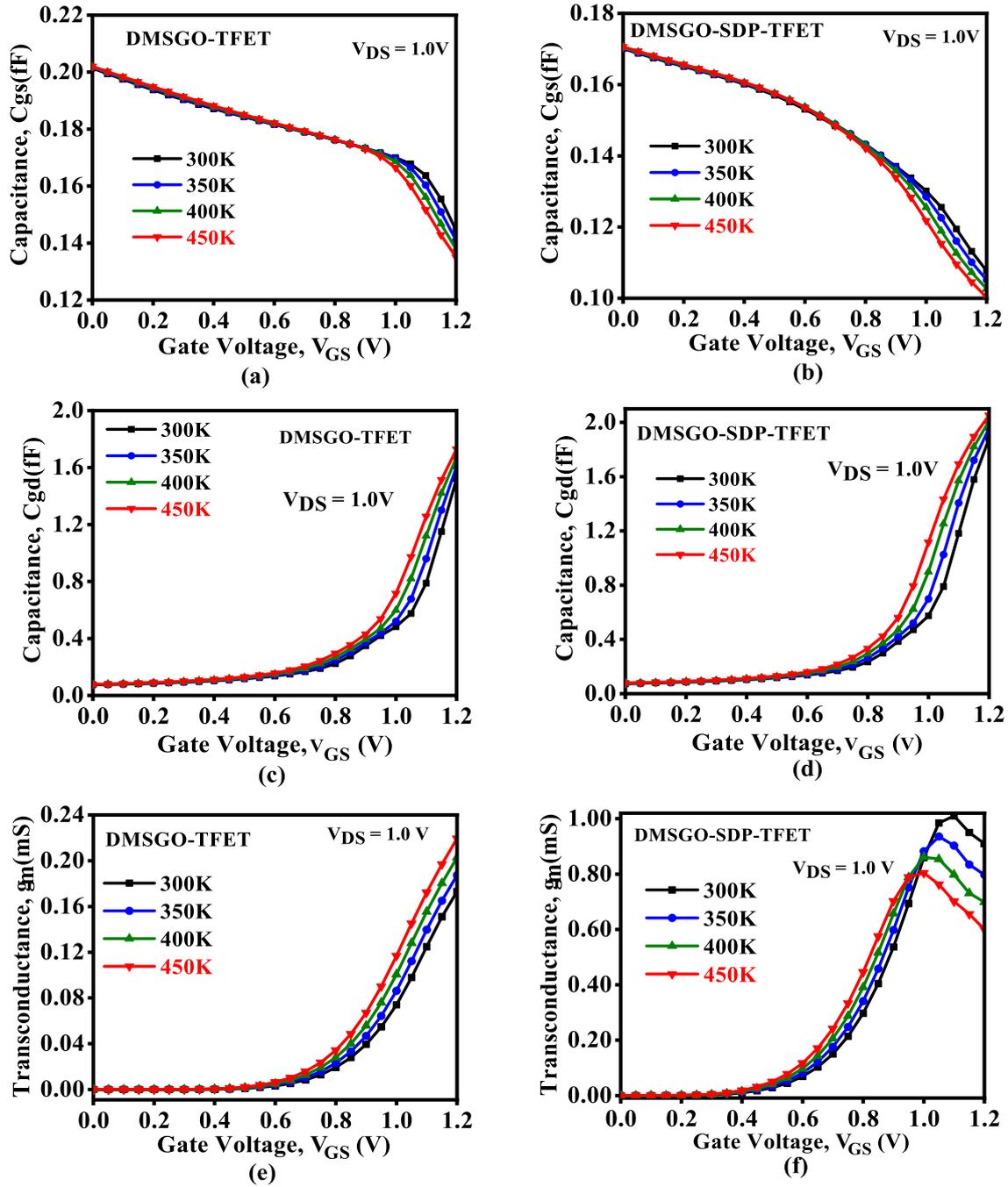


Fig. 5 Variation of C_{gs} with temperature for (a) DMSGO-TFET, (b) DMSGO-SDP-TFET. C_{gd} Variation with temperature for (c) DMSGO-TFET, (d) DMSGO-SDP-TFET. g_m Variation with temperature for (e) DMSGO-TFET, DMSGO-SDP-TFET.

due to increased g_m . After reaching its peak value, it begins to fall due to a decrease in g_m and increased parasitic capacitance. The results also reveal that, as the temperature rises, TFP of both devices falls due to decrease in f_T and g_m because of mobility degradation. Moreover, the results also reveal that at $V_{GS} = 0.75$ V and temperature range 300K to 450K, in terms of %/K variation, DMSGO-TFET exhibits 0.32 %/K vari-

ation in TFP and the proposed DMSGO-SDP-TFET exhibits 0.13%/K. Hence, the proposed DMSGO-SDP-TFET shows better immunity to temperature variations compared to DMSGO-TFET.

The transit time (τ) is another important parameter for the radio frequency performance assessment of the device. It is defined as the time taken by the device to transfer the carriers from source to drain region [24]. It

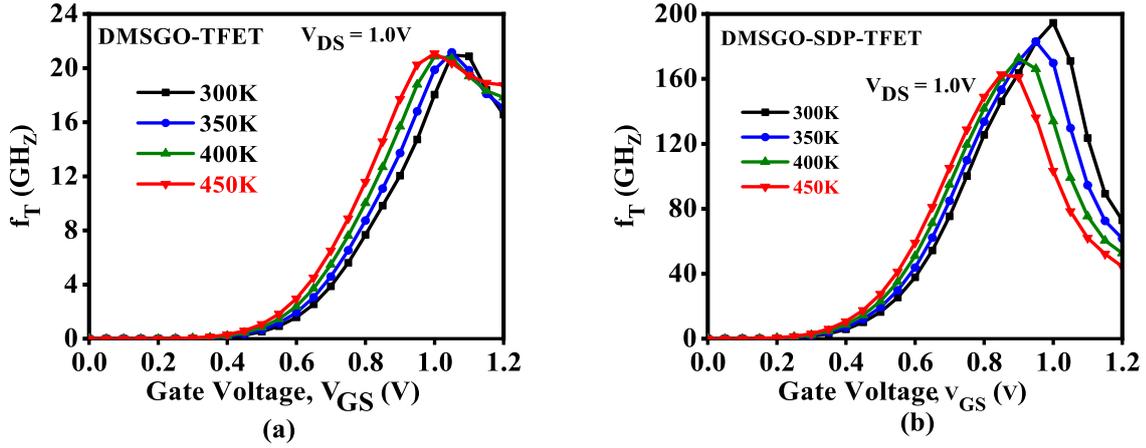


Fig. 6 variation of f_T with temperature for (a) DMSGO-TFET, (b) DMSGO-SDP-TFET.

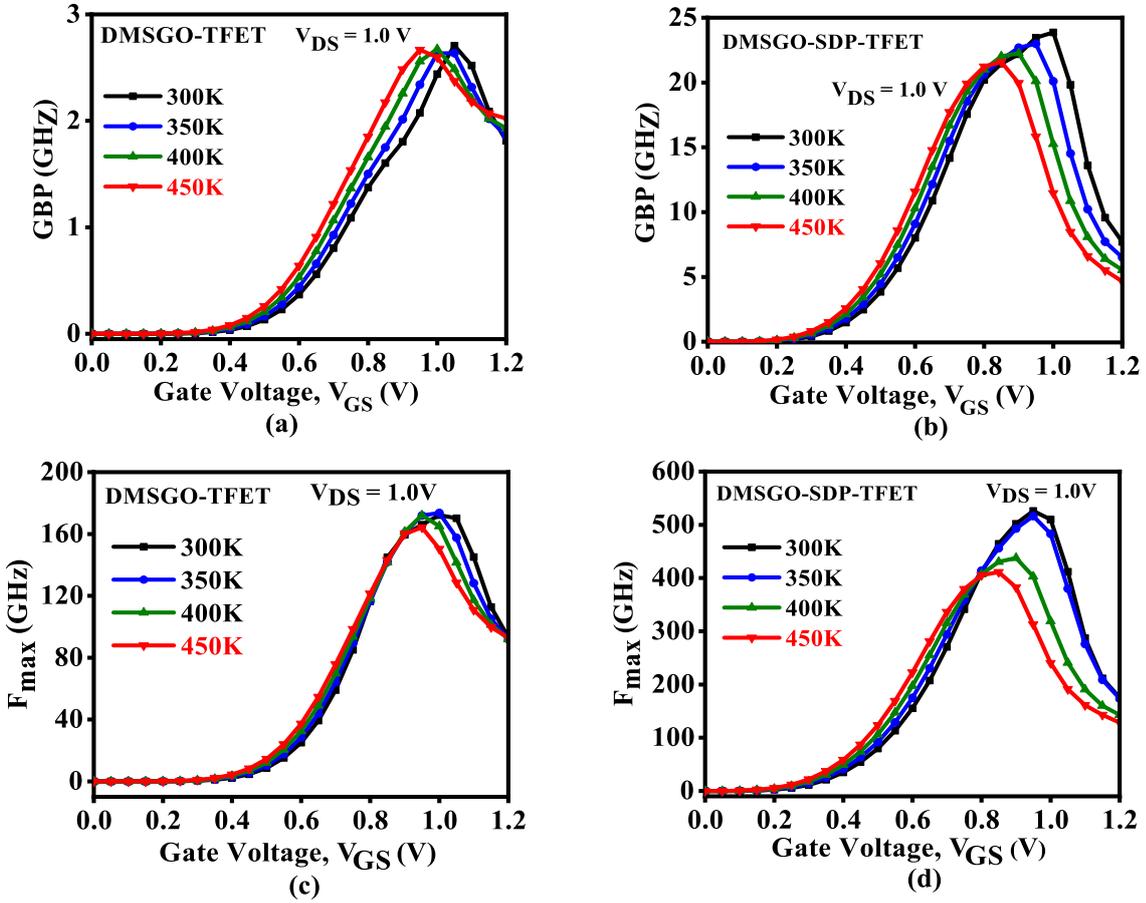


Fig. 7 Variation of GBP with temperature for (a) DMSGO-TFET, (b) DMSGO-SDP-TFET. Variation of f_{max} with temperature for (c) DMSGO-TFET, (d) DMSGO-SDP-TFET.

is formulated as $\tau = \frac{1}{2\pi 10 f_T}$. From the above expression, it is evident that transit time depends on f_T . Figs. 8(c) and 8(d) depicts the transit time variation with temperature for DMSGO-TFET and DMSGO-SDP-TFET, respectively. From Fig. 8(c), it can be seen that with increasing V_{GS} , τ decreases in both devices, whereas in

the case of DMSGO-SDP-TFET shown in Fig. 8(d) after a certain V_{GS} transit time starts increasing due to decrease in f_T because of mobility degradation. Moreover, the results also reveal that, effect of temperature variations on conventional DMSGO-TFET is negligible,

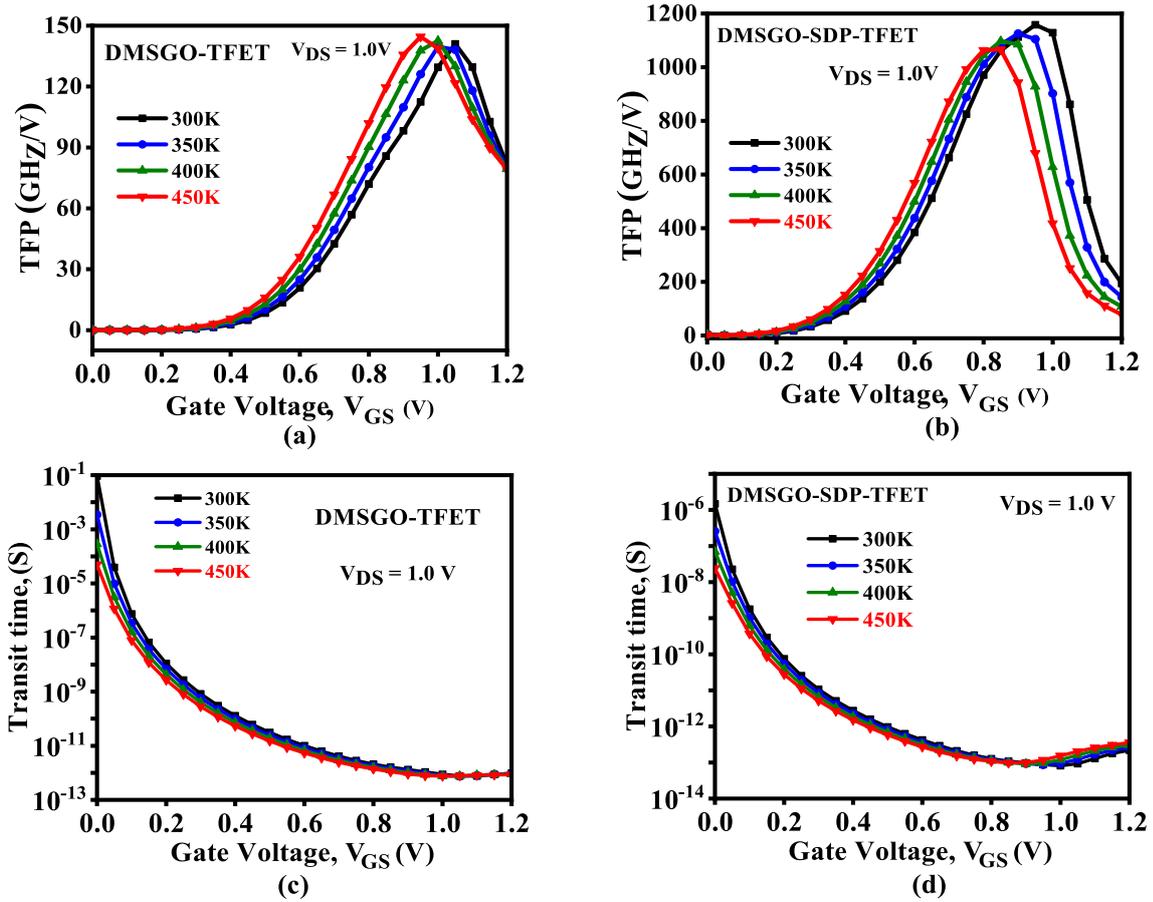


Fig. 8 TFP Variation with temperature for (a) DMSGO-TFET, (b) DMSGO-SDP-TFET. Transit time variation with temperature for (c) DMSGO-TFET, (d) DMSGO-SDP-TFET.

whereas DMSGO-SDP-TFET exhibit significant variation in transit time.

3.3 Temperature sensitivity analysis of linearity and distortion figure of merits

In this section, the impact of temperature variations on the linearity and distortion performance parameters for conventional DMSGO-TFET and the proposed DMSGO-SDP-TFET have been analyzed. In this regard, various linearity and distortion parameters such as g_{m3} , VIP3, IIP3, and IMD3 are considered for analysis. These parameters are defined as follows [30].

$$VIP3 = \sqrt{24 \times \left(\frac{g_{m1}}{g_{m3}} \right)} \quad (3)$$

$$IIP3 = \frac{2}{3} \times \left(\frac{g_{m1}}{g_{m3} \times R_S} \right) \quad (4)$$

$$IMD3 = \left[\frac{9}{2} \times (VIP3)^2 \times (g_{m3})^2 \times R_S \right] \quad (5)$$

Where R_S is assumed to be 50Ω for most RF applications.

To obtain better linearity and minimum distortion VIP3, IIP3 parameters of the device should be higher, and IMD3 parameter must be lower [26], [30]. Figs. 9(a) and 9(b) illustrate the impact of temperature variations ranging from 300K to 450K on higher-order transconductance (g_{m3}) for DMSGO-TFET and DMSGO-SDP-TFET, respectively. It is evident from the above figures that g_{m3} variation is negligible at lower V_{GS} for both devices. Moreover, the results also reveal that DMSGO-SDP-TFET is more sensitive to temperature variations at higher gate voltage compared to DMSGO-TFET.

A device with a higher value of VIP3 shows better linearity [25],[30]. Here, Figs. 9(c) and 9(d) illustrate VIP3 variation with V_{GS} at different temperature ranging from 300K to 450K for DMSGO-TFET and DMSGO-SDP-TFET, respectively. It is evident from the results VIP3 of the proposed DMSGO-SDP-TFET is higher and shows better linearity compared to DMSGO-TFET. Further, the results also reveal that both the devices are temperature sensitive for higher V_{GS} .

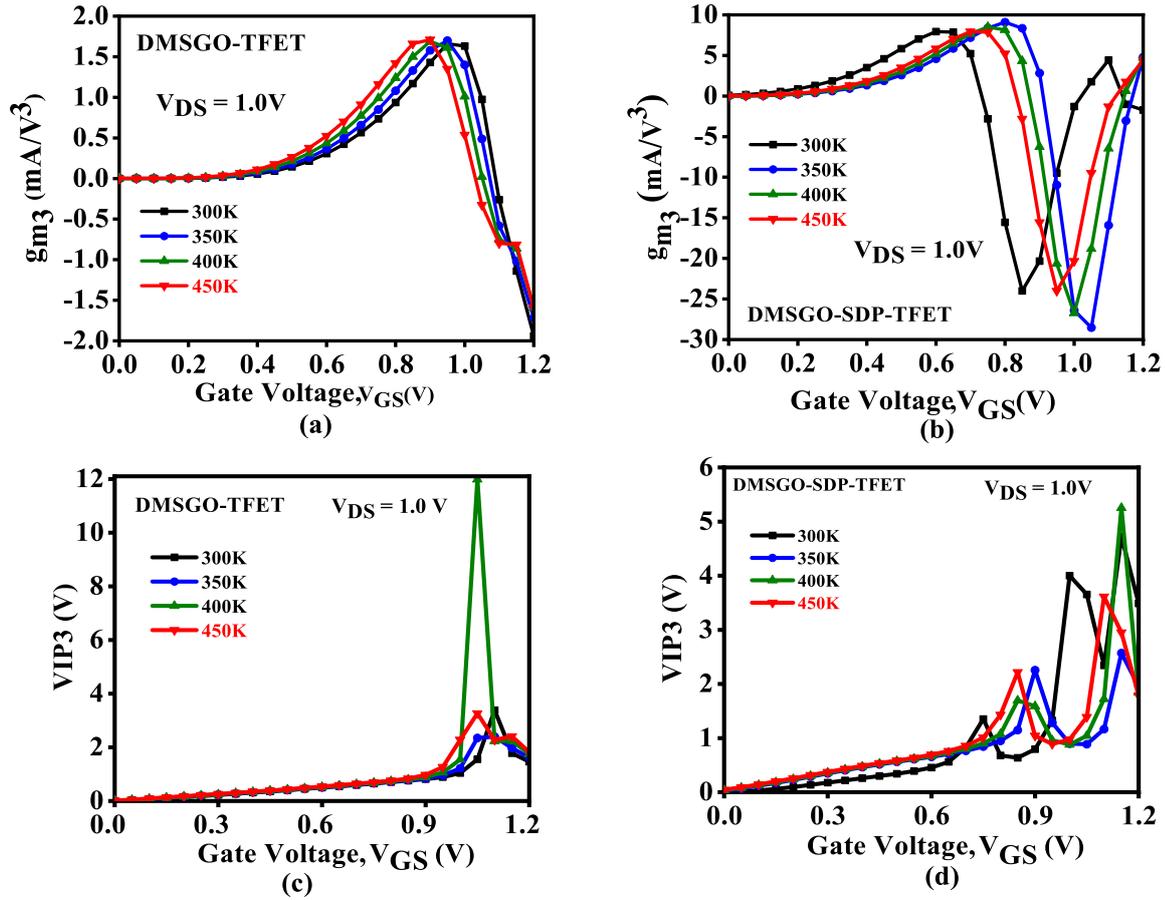


Fig. 9 Variation of g_{m3} with temperature for (a) DMSGO-TFET, (b) DMSGO-SDP-TFET. Variation of VIP3 with temperature for (c) DMSGO-TFET, (d) DMSGO-SDP-TFET.

The impact of temperature variations on the IIP3 for DMSGO-TFET and DMSGO-SDP-TFET are illustrated in Figs. 10(a) and 10(b), respectively. It is evident from the results that IIP3 of the proposed DMSGO-SDP-TFET is higher than DMSGO-TFET, this increase in IIP3 parameter indicates improvement in the linearity performance of the device. Therefore, DMSGO-SDP-TFET shows better linearity compared to DMSGO-TFET. Further, the results also reveal that as the temperature increases from 300K to 450K, both the devices are temperature sensitive at lower and higher V_{GS} .

A lower IMD3 parameter indicates that the device can withstand higher distortions [30]. In this regard, Figs. 10(c) and 10(d) illustrate IMD3 variation with temperature for DMSGO-TFET and proposed DMSGO-SDP-TFET, respectively. These figures demonstrate that DMSGO-SDP-TFET exhibits 0.10%/K variation in IMD3 with temperature ranging from 300K to 450K at $V_{GS} = 1.2$ V and $V_{DS} = 1.0$ V, whereas, for the temperature range and biasing conditions, DMSGO-TFET exhibits 0.41 %/K variation. This indicates that DMSGO-SDP-TFET shows better intermodulation distortion performance

Table 2 Temperature sensitivity in % per kelvin for DMSGO-TFET and DMSGO-SDP-TFET.

| Parameters | DMSGO-TFET | DMSGO-SDP-TFET |
|------------|------------|----------------|
| V_T | 0.069 %/K | 0.095 %/K |
| SS_{AVG} | 0.32 %/K | 0.28 %/K |
| I_{ON} | 1.12 %/K | 0.23 %/K |
| g_m | 0.55 %/K | 0.37 %/K |
| f_T | 0.39 %/K | 0.19 %/K |
| GBP | 0.27 %/K | 0.09 %/K |
| f_{max} | 0.104 %/K | 0.075 %/K |
| TFP | 0.32 %/K | 0.13 %/K |

as compared to DMSGO-TFET. Finally, the temperature sensitivity of different device parameters in % per kelvin for DMSGO-TFET and DMSGO-SDP-TFET are presented in Table 2.

4 Conclusions

A comparative temperature sensitivity analysis of DC, analog/radio frequency, linearity, and distortion performance has been carried out for conventional DMSGO-

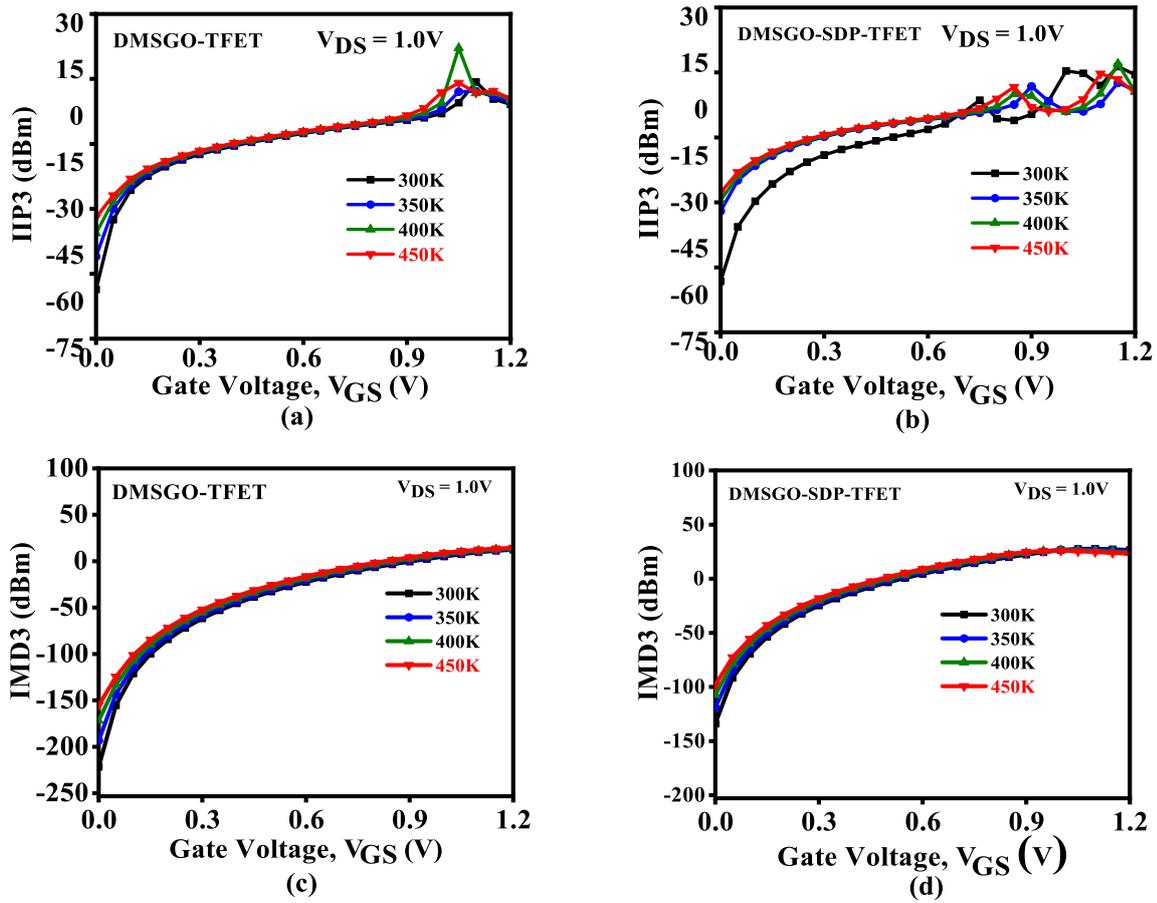


Fig. 10 Variation of IIP3 with temperature for (a) DMSGO-TFET, (b) DMSGO-SDP-TFET. IMD3 Variation with temperature for (c) DMSGO-TFET, (d) DMSGO-SDP-TFET.

TFET and the proposed DMGOSDG-TFET at the temperature ranging from 300K to 450K. Based on this study, it can be stated that for the same biasing conditions and temperature range, the DC, analog/radio frequency, and linearity performance parameters of the proposed DMSGO-SDP-TFET are less sensitive to the temperature variation compared to conventional DMSGO-TFET. Further, the results summarized in table 2 in % variation per kelvin, indicate that DMSGO-SDP-TFET is more reliable when compared to DMSGO-TFET. Hence, it can be concluded that the proposed DMSGO-SDP-TFET is a better choice for low power switching and analog/radio frequency applications for elevated temperature range .

Declarations

Funding: The authors did not receive any financial support from any agency/organization for the submitted work.

Conflict of Interests: No conflicts of interest.

Availability of data and material (data transparency): All the data taken from another resource

has been given the corresponding reference. The data, for which reference is not provided, is the original data.
Code availability (software application or custom code): The code has been implemented on 2-D silvaco ATLAS device simulator.

Author contributions: Dharmender, Kaushal Nigam and Satyendra Kumar in this work contributed equally to the design and implementation of the research, to the analysis of the results and to the writing of the manuscript.

Compliance with ethical standards: The manuscript follows all the ethical standards, including plagiarism.

Consent to Participate Yes.

Consent for publication: Yes.

Acknowledgements: The authors are thankful to the Department of Electronics and Communication Engineering, Jaypee Institute of Information Technology, Noida, Uttar Pradesh, India, for providing computational resources to carry out this work.

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