Enhanced All-optical Y-shaped Plasmonic NAND Gate Model, Analysis, and Simulation for High Speed Computations

Ipshitha Charles
G Pullaiah College of Engineering and Technology
Alluru Sreevani
G Pullaiah College of Engineering and Technology
SabbiVamshi Krishna
Ravindra College of Engineering for Women
Sandip Swarnakar (sandipswarnakar.2008@gmail.com)
G. Pulliah College of Engineering and Technology https://orcid.org/0000-0003-3767-0916
Santosh Kumar
Liaocheng University

Research Article

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Abstract

In this digital era, all-optical logic gates (OLGs) proved its effectiveness in execution of high-speed computations. A unique construction for all optical NAND gate based on the notion of power combiner employing metal–insulator–metal (MIM) waveguide in the Y-shape in a minimal imprint of 6.2 μm × 3 μm is presented and the structure is evaluated by finite-difference time-domain (FDTD) technique. The insertion loss (IL) and extinction-ratio (ER) for proposed model are 6 dB and 27.76 dB. The simplified model is used in the construction of complex circuits to achieve greater efficiency, which contributes to the emergence of a new technique for designing plasmonic integrated circuits.

1. Introduction

The modern technology aims for rapid communication devices that can surpass the diffraction limit of photonic devices, and plasmonics have shown to be a viable option in this regard [1–3]. It is the science that focuses on generating, optical signal detecting and processing at metal-dielectric interface [4]. Plasmonic waveguides may be used to address the main disadvantages in a plasmonic circuit, such as restricted propagation time, rise in temperature and difficulty in changing the signal direction. In recent years, researchers have examined different plasmonic waveguides including MIM, IMI, and dielectric-loaded surface plasmon polaritons (DLSPP) [5]. Compared to insulating waveguides, plasmonic MIM waveguides enable greater confinement and therefore been presented as a potential option for nanoscale optical circuits [6–10]. Logic gates are essential components in all optical circuit design and a numerous optical equipments, like directional coupler (DC), Mach–Zehnder interferometer (MZI), power couplers, and power dividers, are utilized to realise logic gates such as AND, OR, NOT, XOR, and XNOR, along with universal gates such as NAND and NOR [11]. As a result, these all-OLGs may be utilised to construct any combinational circuit, including multiplexers, de-multiplexers, parity generator, adders and subtractors, and code translators [12–15]. Conventional OLGs give cut-off states and interferometric effects, but plasmonic logic gates greatly minimise size and signal losses; it can also lower signal thresholds of logic operations and offer rapid switching in optical devices.

The framework of the suggested paper presents a simplified all-optical NAND gate design with power coupling concept employing a Y waveguide and simulated in FDTD software. The Y-power coupler plasmonic NAND gate design is reported in Sect. 2. Section 3 presents the simulation findings. Section 4 has a results analysis, in which the current study is also compared to prior published studies, and Sect. 5 concludes the paper.

2. The all-optical plasmonic NAND gate structure employing Y-power combiner

A miniaturized all-optical plasmonic NAND gate is modelled by arranging S-bend and linear waveguides of equal width (W) using power combiner concept. The presented design is obtained in a wafer size of 6.2 μm × 3 μm by arranging two parallel S-bend waveguides of equal length (L_s) along XZ axis in Y shape separated by a distance (D) and joined to single end of a linear waveguide of length (L) whose structure is shown in Fig. 1. An external change in the phase controls the inputs supplied to both ends of the power

combiner. The final minimised structure is achieved by varying the Y-combiner parameters such as the L_s, D, and L.

By altering the length of S-bend waveguide (L_s) and maintaining the separation gap between inputs (D) as 2.5 μm, different factors like the highest output power when turned ON and OFF and also ER may be determined, as shown in Table 1. It is observed that for S-bend length of 3.6 μm, the obtained ER value is 27.76 dB that is higher compared to the rest. The S-bend length versus ER plot is depicted in Fig. 2.

Table 1
ER for different values of S-bend length (L_s) in Y-shaped plasmonic NAND gate

Sl. No.	S-bend length (μm)	P_{ON}	P_{OFF}	Extinction ratio (dB)
1	3.1	4.26	0.009	26.75
2	3.2	4. 31	0.008	27.31
3	3.3	4. 36	0.008	27.36
4	3.4	4. 37	0.008	27.37
5	3.5	4. 32	0.008	27.32
6	3.6	4.18	0.007	27.76
7	3.7	4.28	0.011	25.90

Similarly, all parameters indicated are indeed computed by changing the value of D by maintaining L_s at 3.6 μm, the results are tabulated in Table 2. It is observed that ER is more for a separation between waveguide of 2.6 μm resulting in 27.76 dB. The separation between waveguides versus ER is plotted and displayed in Fig. 3.

Table 2
ER for various separations between S-bend waveguides (D) of the Y shaped plasmonic NAND gate power combiner

Sl. No.	D	P_{ON}	P_{OFF}	Extinction ratio (dB)
1	2.6	4.18	0.007	27.76
2	2.7	4. 40	0.01	26.43
3	2.8	4. 46	0.01	26.49
4	2.9	4. 46	0.01	26.49
5	3.0	4. 41	0.01	26.44

The length of S-bend waveguide and D are maintained constant at 3.6 μm and 2.6 μm, correspondingly, whereas the linear length of waveguide is adjusted to get the highest ER. Table 3 presents the ER for various linear lengths of waveguide. The higher ER of 26.87 dB is reported for L = 2.5 μm. A linear length waveguide versus ER plot is depicted in Fig. 4 and the final dimensions of the Y-power coupler plasmonic NAND gate with the highest ER are tabulated in Table 3.

Table 3
ER of different linear waveguide lengths of Y-shaped plasmonic NAND gate

Sl. No.	Linear length	P_{ON}	P_{OFF}	Extinction ratio (dB)
1	2.4	4.32	0.009	26.81
2	2.5	4. 38	0.009	26.87
3	2.6	4. 36	0.009	26.85
4	2.7	4. 31	0.009	26.80
5	2.8	4. 29	0.009	26.78
6	2.9	4.35	0.009	26.84

The structural requirements obtained by altering dimensions of the presented Y- power combiner plasmonic NAND gate design are tabulated in Table 4.

Table 4
The design parameters of plasmonic Y shaped NAND gate

Sl. No.	Parameter	Value
1	length of S-bend waveguide(L_s)	3.6 μm
2	Length of linear waveguide (L)	2.5 μm
3	Separation between input waveguides (D)	2.6 μm
4	Refractive index (n)	2.1
5	Width of the waveguide (W)	0.25 μm

3. The Y-power combiner plasmonic NAND gate FDTD simulation results

The optimized all-optical NAND gate design contains plasmonic waveguide of refractive index (n) = 2.1 and continuous-waveform (CW) in transverse electric (TE) mode, with wavelength (λ) of 1.55 μm is provided at both inputs. The power at input is $0.7e^9$ W/m and $3e^9$ W/m for low and high intensity optical signals, respectively. The presented structure is analysed using the FDTD technique and Table 5 shows the parameters of the simulation for the design proposed.

Table 5
Simulation parameters of Y-shaped plasmonic NAND gate power combiner

Parameter	Value
Polarization type	TE
λ	1550 nm
X mesh Size (μm)	0.0114
Z mesh Size (μm)	0.0114
X mesh cells	349
Z mesh cells	603
Transverse Input feld	Gaussian
Low-intensity power	0.7×10^9 W/m
High-intensity power	3×10^9 W/m

Figure 5 depicts the propagation of light along the proposed NAND gate for the specified input signal pairings using the FDTD method. When either one or both of the inputs are low, the NAND gate's output is high as shown in the truth Table 6; otherwise, the output is low.

Table 6
The NAND gate's truth table, as well as the given input phase

Input				Output
A	B	Phase A	Phase B	(A × B)'
0	0	0^0	0^0	1
0	1	0^0	0^0	1
1	0	0^0	0^0	1
1	1	180^0	0^0	0

2. The All-optical Plasmonic Nand Gate Structure Employing Y-power Combiner

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0	1	0^0	0^0	1
1	0	0^0	0^0	1
1	1	180^0	0^0	0

Instance 1:- A = 0, B = 0

In this instance, both the Y-combiner inputs are provided a signal of less- power intensity $0.7e^9$ W/m. According to the NAND gate truth table, the output power is noted to be high. Same phase of 180° or 0° is given to both input signals resulting in constructive interference and the NAND gate output is observed to be higher (Y = 1) as shown in Fig. 5(a).

Instance 2:- A = 0, B = 1

Here, the upper end of combiner is given less- power intensity ($0.7e^9$ W/m) in contrast the lower end of combiner is provided a signal of greater-power intensity ($3e^9$ W/m). A same phase of 180° or 0° is allowed in both inputs. As in the preceding example, destructive interference will arise, reducing the strength of the output signal. As a result, the NAND gate's output is high (Y = 1), as illustrated in Fig. 5(b).

Instance 3:- A = 1, B = 0

In contrast to the preceding instance, the upper end of combiner is given a greater intensity ($3e^9$ W/m) whereas the below end is provided a signal of less-intensity power ($0.7e^9$ W/m). Thereby, due to the same phase, constructive interference will arise, resulting in high output of NAND gate (Y = 1) as depicted in Fig. 5(c).

Instance 4:- A = 1, B = 1

Finally, the two inputs of power coupler are provided a high intensity power signal ($3e^9$ W/m) The phase for one input is 180° and the other is 0° resulting in destructive interference resulting in low output intensity (Y = 0) as shown in Fig. 5(d).

4. Result Analyses

The suggested device has a 6.2 μm × 3 μm footprint. The output findings are used to determine performance metrics such as IL and ER. The suggested NAND gate IL is calculated by

Insertion loss (IL) = $10log_{10}(\frac{P_{out}}{P_{in}})$

Where P_{out} and P_{in} are the peak output and input powers. The suggested NAND gate ER is given by

Extinction ratio (ER) = $10log_{10}(\frac{P_{out}|ON}{P_{out}|OFF})$

$P_{out}|ON$ and $P_{out}|OFF$ are power outputs in ON and OFF mode. So, the proposed design obtained IL and ER of 6 dB and 27.76 dB. The other parameters like response time of 32 fs and bit rate of 31.25 THz is observed. A comparison of the proposed structure with previous published works is made and tabulated in Table 7.

Table 7
Comparison of the suggested all-optical Y shaped plasmonic NAND gate with the previously proposed design performance

Sl. No.	Ref. No.	Material used	Extinction ratio (dB)	Footprint	Refractive index	Low intensity	High intensity	Structure
1	[16]	PhC waveguide	14.2	192 μm^2	n.r[a]	n.r[a]	n.r[a]	2D PhC
2	[17]	MIM waveguide	10.25	40 × 7.5 μm^2	2.01	$0.7e^9$ W/m	$3e^9$ W/m	Plasmonic MZI
3	[18]	Plasmonic MIM waveguide	14.11	7 × 4 μm^2	2.1	$2e^9$ W/m	$3e^9$ W/m	Y shaped power combiner
4	[19]	Plasmonic MIM waveguide	10.55	36 × 8 μm^2	2.01	$0.7e^9$ W/m	$3e^9$ W/m	two nonlinear MZI
5	This work	Plasmonic MIM waveguide	27.76	6. 2 × 3 μm^2	2.1	$0.7e^9$ W/m	$3e^9$ W/m	Y shaped power combiner

n.r[a]: not reported

5. Conclusions

The suggested Y-shaped MIM waveguide concept is utilised to construct an all-optical NAND logic gate. The structure has a surface area of 6.2μm × 3μm, which is less than earlier efforts. In this study, the IL and ER calculated are key factors that are determined to be 6 dB and 27.76 dB, respectively and response time of 32 fs and bit rate of 31.25 THz are also observed. The length of S-bend waveguide, input separation, and linear length of waveguide are designed to provide the highest ER while minimising waveguide losses. The Y-combiner-based NAND gate, with its simple construction and controllability, can provide a novel approach for implementing digital logic functions in electronics. The presented design has a simplified structure that might be utilized to develop ultra-compact devices for rapid optical computing in the future.

Declarations

Acknowledgment

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Availability of data and material

The authors can provide the data on request.

Code availability

No source code is available for this manuscript.

Conflicts of interest

The authors declare that they have no conflict of interest .

Consent to participate

For this type of study formal consent is not required.

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Figures

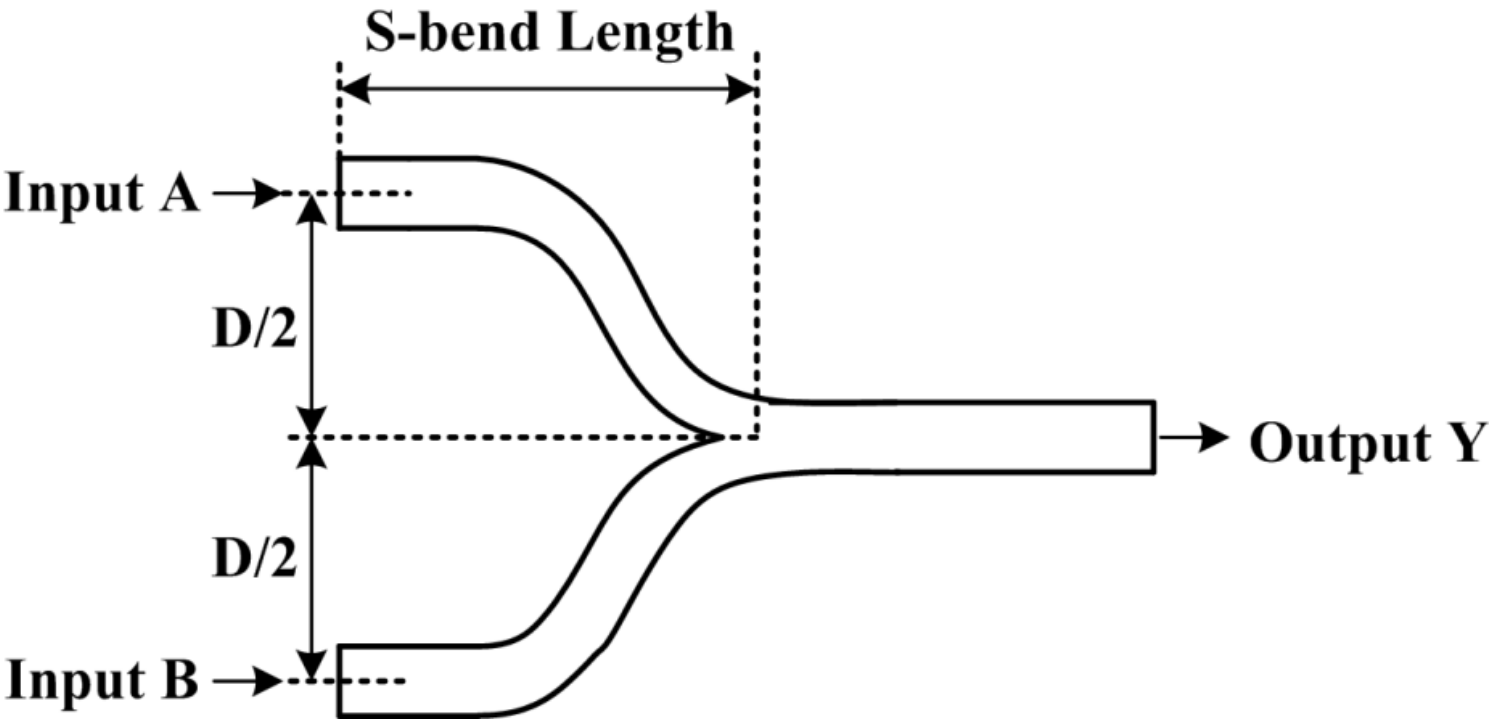

Figure 1

Schematic of Y shaped NAND logic gate using plasmonic waveguide

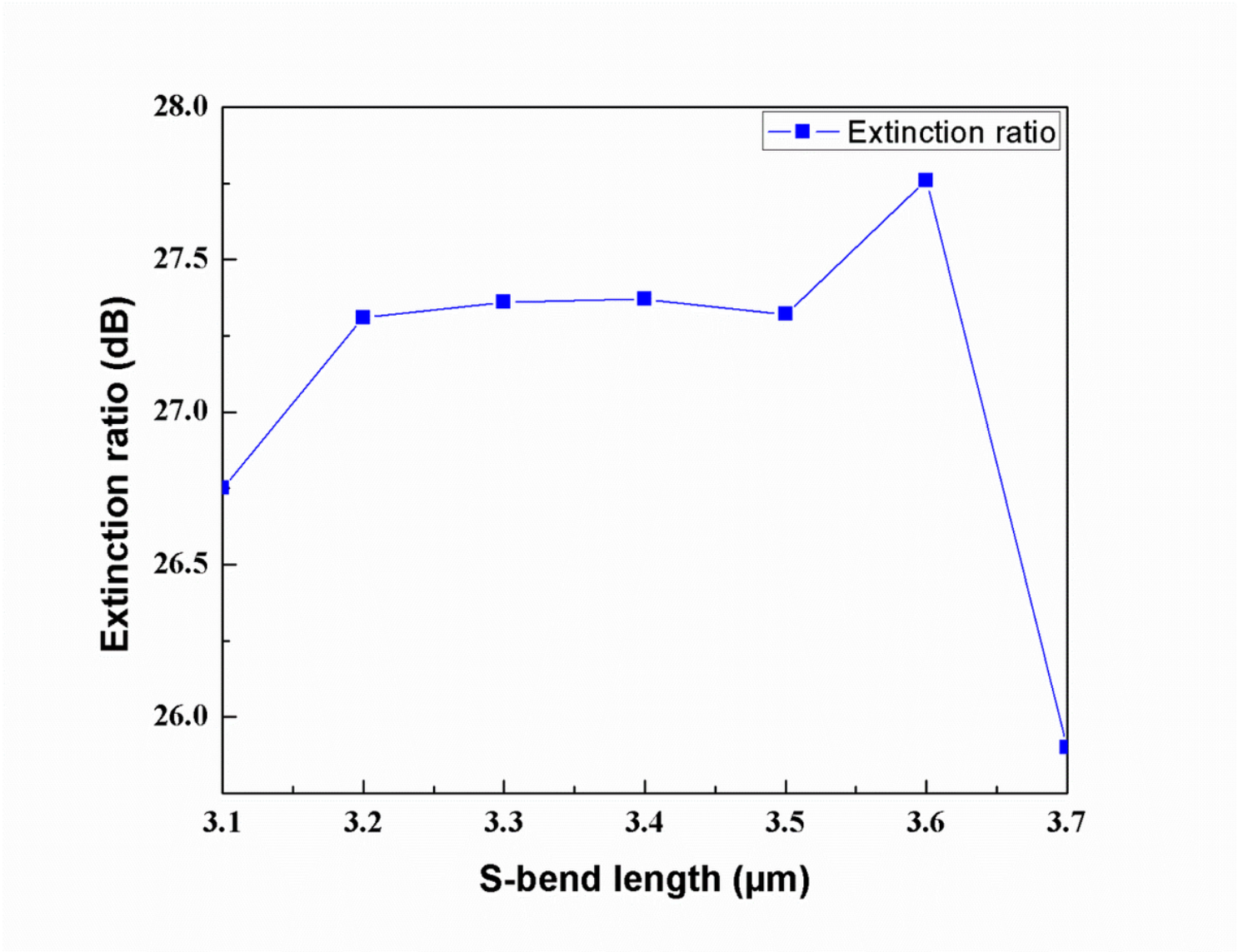

Figure 2

S-bend length versus ER plot at D = 2.5 μm

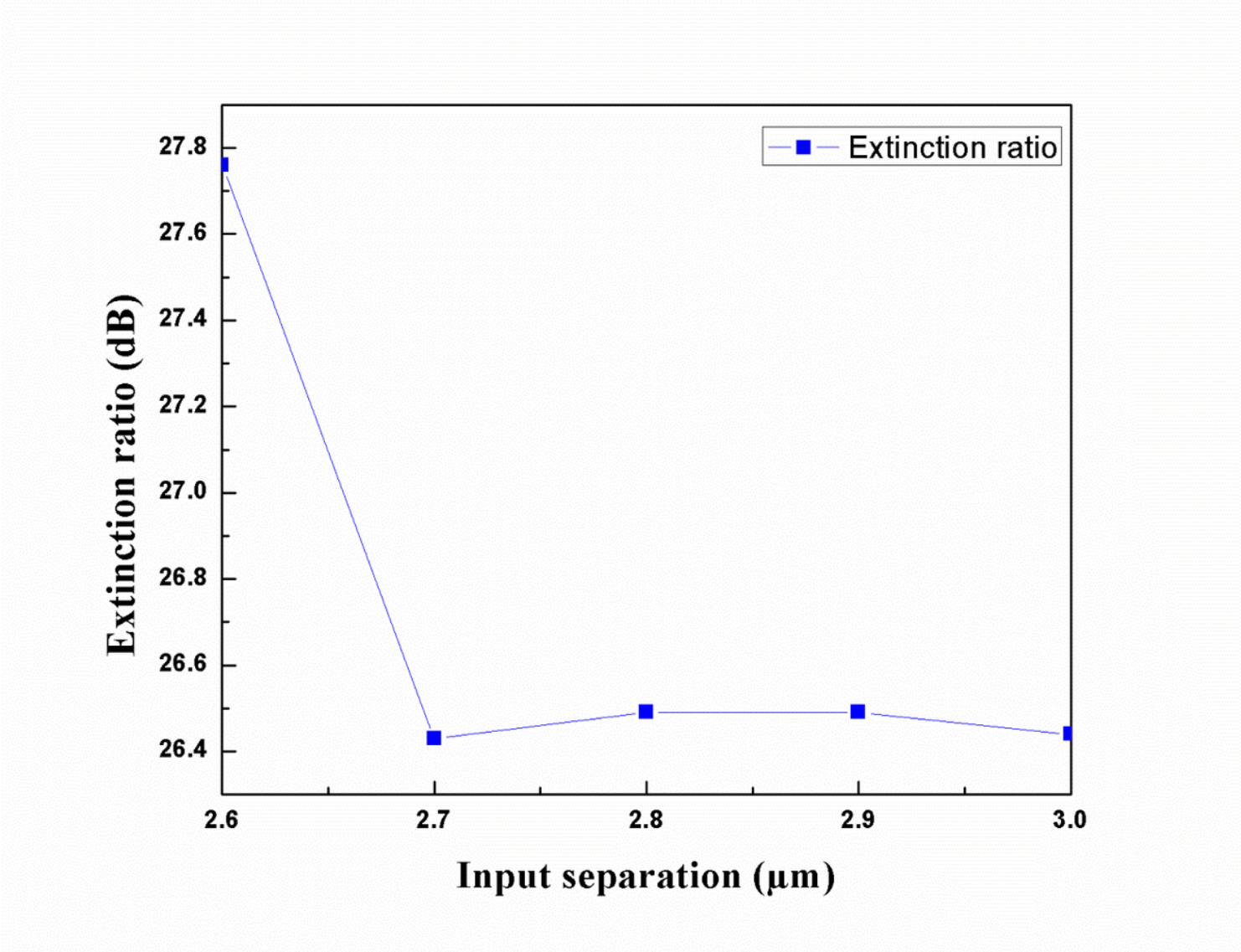

Figure 3

Separation between input waveguides (D) versus ER plot with Ls = 2.5 μm

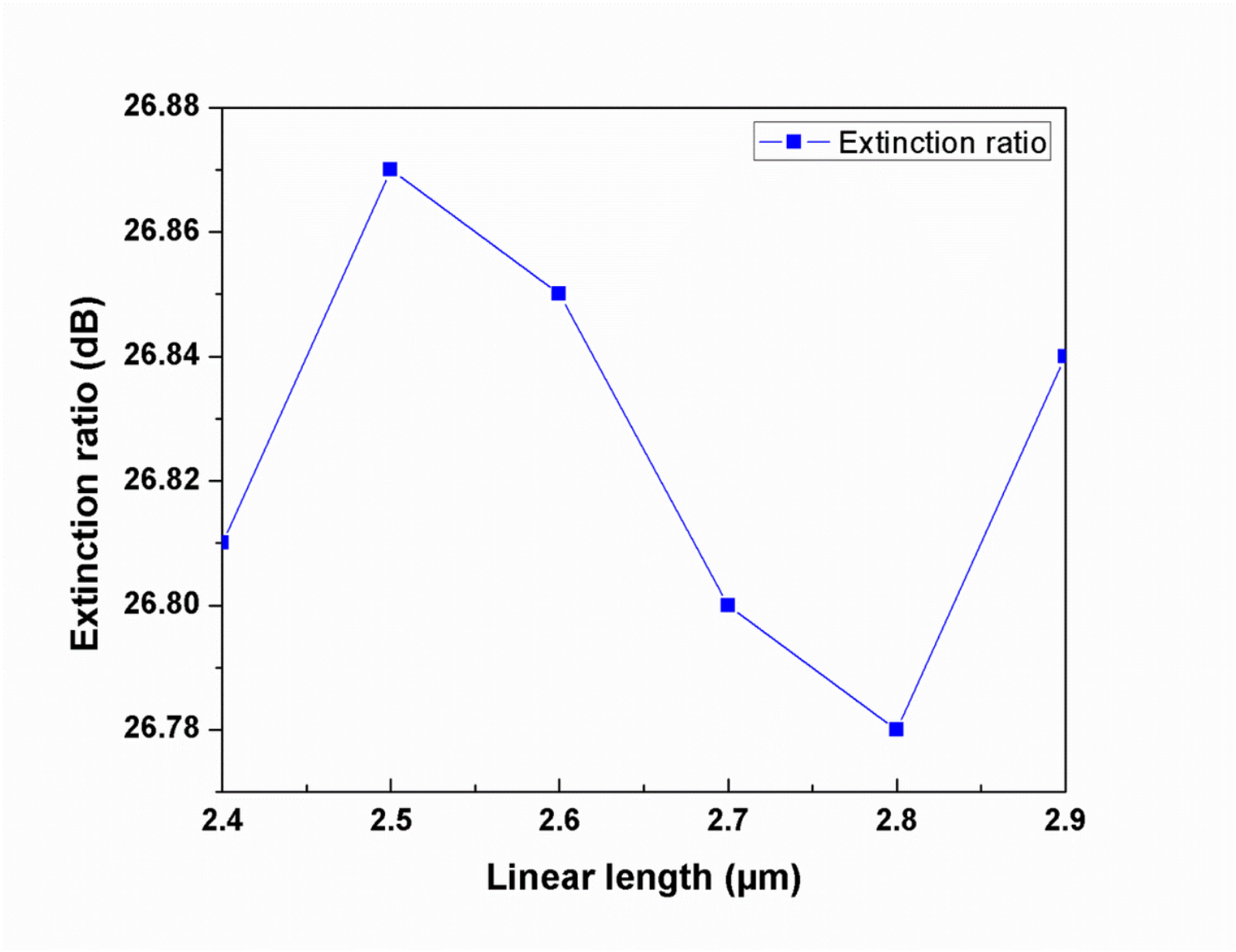

Figure 4

Linear length versus ER plot at Ls = 3.6 μm and D = 2.6 μm

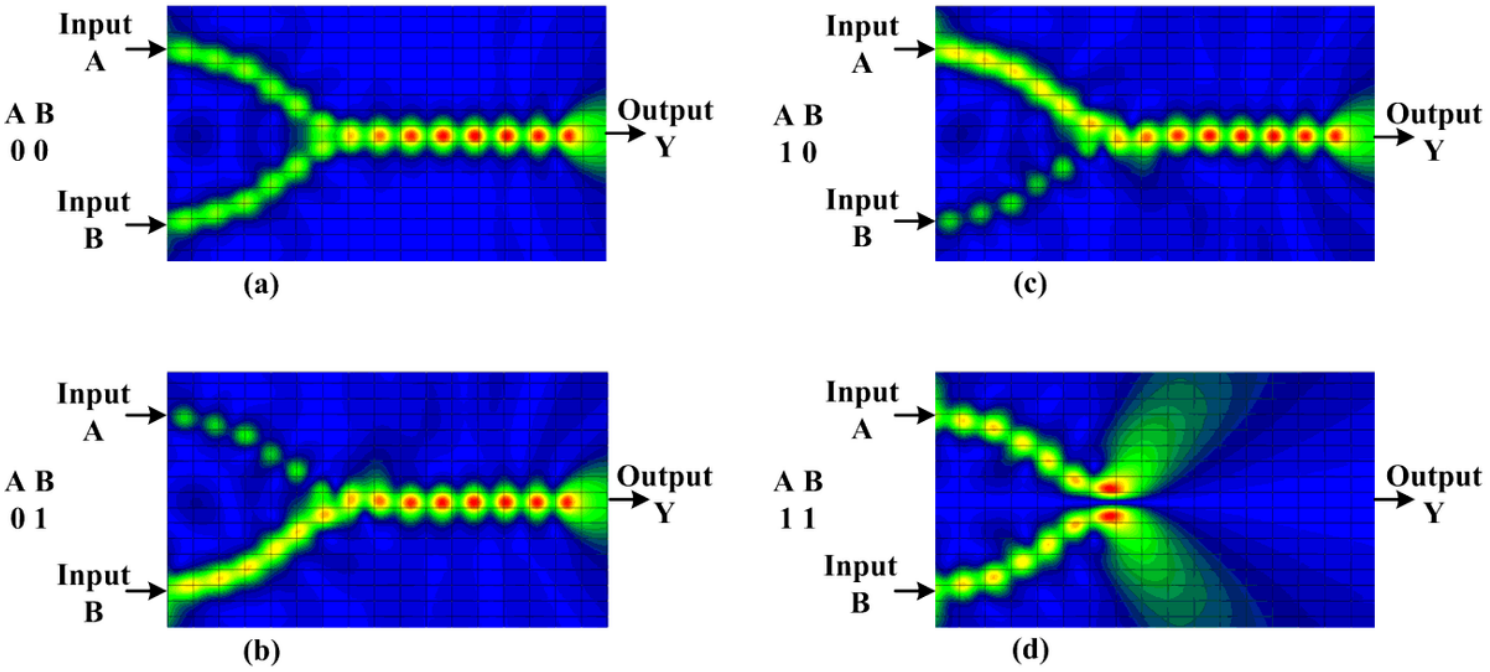

Figure 5

Propagation of light across the suggested Y shaped plasmonic NAND gate power combiner for various instances using FDTD method