A Novel Approach to Investigate Analog and Digital Circuit Applications of Silicon Junctionless-Double-Gate (JL-DG) MOSFETs

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Abstract

The double gate junctionless transistor (DG-JLT) has become the most promising device in sub nano-meter regime. DGJLT based circuits have improved performance and simpler fabrication than their inversion mode counterparts. This paper demonstrates the design of different analog and digital circuits using DGJLT. Amplifiers and inverters are the basic building block of electronic ICs. A MOS amplifier converts the variation of the gate to source voltage to a small current under transconductance and hence, the output voltage. A single-stage amplifier and differential amplifier have been designed with junctionless-double-gate (JL-DG) MOSFET. Trans-conductance, output voltage, and gain have been investigated using ATLAS 2D device simulator. The inverter is the primary logic gate that can be used to verify the device's response in digital applications. Further, CMOS inverter have been designed using JL-DG MOSFET, and its performance parameters such as switching voltage, noise margin, and logic delay have been analyzed. A switching voltage of 0.43 V, noise margin of 0.265 V, and a delay of 19.18 psec have been obtained for the basic cell. CMOS inverter using JL-DG MOSFET at 20 nm technology node have prompted better performance results. Thus, The JL-DG MOSFET has a bright future in low-power analog and digital applications.

1. Introduction

Continuous scaling of MOSFET is being done to achieve high packing density with higher speed. Although scaling has reduced the device size and power consumption, below 20nm it results in fabrication complexity and reduced gate control over channel [1]. Various alternative devices such as SOI, FinFET, TFET, and Junctionless transistors are being used to improve the device performance [2–3]. Numerous channel engineering and gate engineering techniques are used to improve mobility and drive current. High k dielectric gate material, dielectric spacer, dual material gate, nanowire, and nano-tubes have significantly enhanced the gate control over the channel [4–5]. Further, to improve mobility and to reduce the leakage current, charge plasma-based doping-less transistors are getting importance. In this charge plasma technique, the metals of different work functions are used to induce n-type or p-type charged plasma in the semiconductor film.

At smaller dimensions, the fabrication of junction-based devices has become quite complex and costly due to the requirement of abrupt change in doping concentration within a distance of 2–3 nm. This abrupt change in doping requires a millisecond annealing technique. This fast annealing reduces the diffusion of impurity atoms. To resolve this problem, the junctionless transistors are a better choice. In JLTs, there is absence of junction between source channel and channel drain. Since junctions are the primary source of leakage and other short channel effects, this device reflects much improved performance than its junction-based counterparts [6–7]. The JLTs work on the principle of work function difference between gate and channel.

Along with simpler fabrication, this device has following other advantages such as reduced SCEs, high I_{ON}/I_{OFF}, nearly ideal subthreshold swing (~ 60 mV/dec), and low series resistance [8]. Double gate

structure provides better control of channel from both sides of the channel (top & bottom), resulting in reduced leakage current. Multi-gate devices offer improved mobility, better scalability, higher driving current and better transconductance. Due to the bulk conduction mechanism, JLTs have less effect of surface roughness and defects. This results in much lesser noise and improved reliability [9–10].

To assess the utility and performance of this device in analog circuit applications, three different circuits' common source amplifier, source follower amplifier, and differential amplifier, are designed. Further, to investigate digital applications, the CMOS inverter is designed and analysed. The common source amplifier is one of the most widely used circuits of all the FET circuit configurations. It provides current and voltage gain along with satisfactory input and output impedance. Source follower amplifiers, also known as common drain amplifiers, are one of the three basic single-stage amplifier configurations. This amplifier circuit provides high input impedance, low output impedance, unity voltage gain, and high bandwidth. The source follower is mainly used for impedance matching in both analog and digital circuits. The differential amplifier is the widely used amplifier circuit where the difference signal is amplified. This amplifier is used in analog circuits for better noise immunity and reduced harmonic. Various performance parameters of amplifier circuits as drain current, transconductance, and voltage gain, are presented in the paper.

Section II contains the device structure and simulation details. The analog circuit applications as common source, source follower and differential amplifier are presented in Section III. Further CMOS inverter using DGJLT is designed and analysed in Section IV, followed by a detailed conclusion in Section V.

2. Device Structure

The two-dimensional (2D) representation of junctionless-double-gate (JL-DG) MOSFET is presented in Fig. 1. The physical channel length and channel thickness are 20nm and 5nm, respectively. The source, drain, and channel regions are uniformly doped with an n-type impurity having a doping concentration of $1x10^{19}$atoms cm^{-3}. The gate material is isolated from silicon substrate with a 1nm spaced silicon dioxide (SiO_2) dielectric material. The work function of the gate material is adjusted to 5.25 eV with a heavily doped p+ poly layer. Both the gates of the double gate structure are internally connected to increase the capacitive coupling of the channel region and thereby reducing the SCEs. Table-I presents the physical device parameters of the proposed JL-DG MOSFET. In-order to simulate the low power analog and digital circuits using proposed JL-DG MOSFET, field-dependent saturation model, concentration-dependent mobility model, constant-voltage-temperature (CVT) model, Lombardi mobility model, and Shockley-Read-Hall recombination model have been used. [11-12].

Table- I

The physical device parameters of JL-DG MOSFET

Symbol	Parameter	Value
L_{ch}	Channel Length	20nm
t_{si}	Channel Thickness	5nm
t_{ox}	Oxide Thickness	1nm
N_D	Doping concentration	$1\times10^{19}cm^{-3}$
n_i	Intrinsic carrier concentration	$1.45\times10^{10}lcm^{-3}$
Φ_M	Gate Metal-work function	5.25eV

3. Analog Circuit Application

Handheld devices, digital cameras, mobile phones, and laptop computers are all equipped with various types of amplifiers nowadays. Amplifiers are the backbone of integrated circuits. Most analog and digital signals need amplification to drive a load or to distinguish the noise of a subsequent stage, or to provide a significant logic level to a digital circuit. In this section, we will discuss various amplifiers such as common source, source follower, and differential amplifiers.

3.1 Common Source Amplifier:

A MOSFET convert variations in the applied gate to source voltage V_{GS} to a small signal drain current under its transconductance. This current will drive a load and generate an equivalent output voltage [13]. The common source amplifier is shown in Fig. 2. The operation of this circuit is explain as follows. In this circuit, the input signal is applied to the proposed JL-DG MOS transistor (T_1). The drain and the gate terminal of the transistor (T_2) is shorted, and it will act as a diode-connected load resistance. In this configuration, the transistor T_2 is always ON in the saturation region which offers a high resistance. The transistor T_2 has been taken from the Silvaco Atlas model library such that it is having a threshold voltage of 0.5 V.

Figure 3 shows the variation of drain current (I_D) and transconductance (g_m) of common source amplifier with the variation of applied V_{GS}. It has been observed from the figure that as the gate voltage increases below its threshold voltage, the drain current increases. When the V_{GS} reaches to the threshold voltage of the MOS device, the drain current of amplifiers becomes constant. It is also observed from the figure that the transconductance, which is a function of drain current, initially increases with V_{GS}, attains a maximum value, and then starts diminishing.

Figure 4 shows the variation of output voltage and gain of common source amplifier with V_{GS}. When the drain current across the transistor (T_1) is low, the maximum current will be delivered to the load through

the transistor (T_2), and the output voltage will be high. Hence, the gain of the common source amplifier will be increased. As the gate voltage increases, the drain current across the transistor (T_1) will increase. Hence, the output voltage and gain will reduce. Table II presents the peak values of various performance parameters such as drain current, transconductance, output voltage, and voltage gain of the common source amplifier.

Table- II: Peak Values of performance parameters of commons source amplifier.

Symbol	Parameter	Value
I_D	Drain Current (A)	8.2815×10^{-5}
g_m	Transconductance (S)	1.03×10^{-3}
V_{out}	Output Voltage (V)	0.7275
A_V	Voltage Gain	36.3526

3.2 Source Follower Amplifier:

The source follower or common drain amplifier can be used as a buffer for impedance matching. The main advantages of the source follower amplifier are high input impedance, low output impedance, unity voltage gain, and high bandwidth. Figure 5 shows the circuit diagram of the source follower amplifier. The external bias voltage applied at the gate of the transistor (T_1) makes sure that it operates in the saturation region. Whereas, the input signal is applied to the proposed JL-DG MOS transistor (T_1). To gain a better understanding of the source follower amplifier, small-signal intrinsic gain (A_v) has been given as;

$$A_v = \frac{g_m}{g_m + g_{mb}} \qquad (1)$$

Where g_m is the transconductance of the JL-DG MOSFET and g_{mb} is the transconductance due to the back gate bias effect.

The variation of drain current and transconductance with applied V_{GS} for a source follower amplifier is shown in Fig. 6. The results reveal that the drain current of the source follower amplifier increases with an increase in the applied V_{GS}. It is also observed from the figure that the transconductance initially increases with V_{GS}, attains a maximum value, and then starts diminishing. The output voltage and gain of the source follower amplifier are shown in Fig. 7.

As the gate voltage increases, the drain current across the transistor (T_2) increases, and the output voltage will increase. Hence, the voltage gain of the source follower amplifier will increase. The maximum gain that can be achieved with a source follower amplifier is unity. The peak values of various

performance parameters such as drain current, transconductance, output voltage, and voltage gain of the source follower amplifier are tabulated in Table III.

Table- III

Peak Values of performance parameters of source follower amplifier.

Symbol	Parameter	Value
I_D	Drain Current (A)	8.287×10^{-5}
g_m	Transconductance (S)	1.4194×10^{-4}
V_{out}	Output Voltage (V)	0.8276
A_V	Voltage Gain	0.8276

3.3 Differential Amplifier:

The differential amplifier has become the preferred choice in modern high-performance analog and mixed-signal circuits. The differential operation offers higher immunity to the environmental noise than the single-stage operation [14]. Operational amplifiers, high-speed comparators, video amplifiers, and various other analog circuits employ differential amplifiers as input stages. Fully differential amplifiers are popular in integrated circuit design because they offer a higher power supply rejection ratio (PSRR) than single-ended competitors [15]. Furthermore, even-order nonlinearity does not exist in the differential inputs and outputs of well-matched, balanced MOS circuits.

Figure 8 shows a resistive load differential amplifier using the proposed JL-DG MOSFET. An external bias is applied to the gate of the transistor (T3) such that it will provide a bias current to the differential pair. The input voltage is applied to transistors T_1 and T_2, respectively. The output voltage is computed between two nodes having equal and opposite signal outrage around a fixed voltage. Hence, its output is a differential signal. The mid-point voltage in differential output is termed as common-mode (CM) level. It can be used to identify the CM level as the bias voltage, i.e., the value of output voltage in the absence of signal. The input-output characteristic of the differential amplifier is shown in Fig. 9.

The simulation results reveal that the output voltage swing will be high for a differential amplifier using the proposed JL-DG MOSFET. The gain of the differential amplifier with respect to input differential voltage is shown in Fig. 10. The results reveal that the common mode gains of differential amplifier will be maximum at CM level. Table IV shows the CM level and maximum gain of the differential amplifier stage using the proposed JL-DG MOSFET. It has been observed that the proposed differential amplifier provides a higher gain. Hence, it can be used in high-performance analog circuits.

Table- IV

Peak Values of performance parameters of the differential amplifier.

Symbol	Parameter	Value
$V_{out,CM}$	Output Common mode level (V)	0.60326
A_V	Voltage Gain	4.7468

4. Digital Circuit Application:

The inverter, the fundamental building block of any digital circuit is used to perform a boolean operation on a single input variable. The complementary MOS (CMOS) inverter consists of an NMOS driver transistor and a PMOS load transistor. The CMOS inverters are widely used for low power digital circuits. The advantage of the CMOS inverter circuits is low power dissipation, high speed, high noise margin, and high output voltage swing. [16–17]

The proposed JL-DG NMOS is employed as a pull-down driver transistor in a CMOS inverter as shown in Fig. 11. The symmetrical JL-DG PMOS is used as a pull-up load. The output load capacitance determines the delay in a CMOS inverter. The output load capacitance is the combination of external capacitance and parasitic capacitance. By summing the overall parasitic capacitances between the output node and the ground, the accurate value of the output load capacitance may be computed. C_{gs}, C_{gd}, C_{sb}, and C_{db} are the basic parasitic capacitances in nano-scale MOSFETs. Furthermore, potential difference between the source and substrate is kept zero for both a PMOS and an NMOS transistors. As a result, the source to bulk capacitance (C_{sb}) has a minor effect on the transient characteristics of the CMOS inverters. The gate to source capacitance (C_{gs}), the gate to drain parasitic capacitance (C_{gd}), and drain to bulk parasitic capacitance (C_{db}) are included in the calculations [18].

The voltage transfer characteristics (VTC) or DC transfer characteristics of the CMOS inverter is shown in Fig. 12. The transient and DC analyses of the proposed individual inverter stage are simulated by using numerical simulator ATLAS Silvaco [19]. The DC transfer characteristics provides the information of the switching threshold and the noise margin of the CMOS inverter. The plot also shows that the inverter's properties are practically centered about $V_{dd}/2$, which is essential in implementing the suggested high-density inverter. Figure 13 shows the transient analysis of the CMOS inverter. The transient analysis of the inverter provides the variation of output voltage with respect to the input voltage. This is helpful to compute the delay of the output transition.

Table V: CMOS inverter performance parameters

Symbol	Parameter	Value
V_{sp}	Switching Threshold (V)	0.430
NM	Noise Margin (V)	0.265
t_{pd}	Delay (psec)	19.180

Table V shows the performance parameters such as switching threshold, noise margin, and logical delay of CMOS inverter. The noise margin (NM) is the maximum amount of noise that a circuit can tolerate so that the logic of the inverter does not change. For the noise beyond this limit, the circuit performance and reliability degrade significantly. So, noise margin of the circuit must be kept as high as possible. Very High NMs, on the other hand, cause enormous voltage excursions, resulting in longer delays and increased power dissipation. Thus, for satisfactory operation, there is a trade-off between NMs, latency, and power. That means for high noise margin the speed of the circuit is affected.

Propagation delay is the time it takes for a circuit to produce an output as soon as the input is applied. Propagation delay in the inverter is calculated by taking the average of propagation delays (Low to high and high to low) encountered in the proposed circuit. These delays mainly depend on the device capacitance and mobility of carriers. Mathematically it is defined as

$$T_p = \frac{T_{LH}+T_{HL}}{2} \qquad (2)$$

From the simulation, a switching voltage of 0.43 V, noise margin of 0.265 V, and a delay of 19.18 p sec have been achieved with the CMOS inverter using JLDG MOSFET at 20 nm technology node.

5. Conclusion

In this research paper, we investigate the analog circuit applications of JL-DG MOSFET. The single-stage amplifiers such as common source amplifier, source follower, and differential amplifiers has been designed. The performance parameters such as drain current, transconductance, output voltage, and gain of these analog circuits have been studied using ATLAS 2D device simulator. The results reveal that the proposed common source amplifier using JL-DG MOSFET has a higher drain current, output voltage, and voltage gain. The common drain amplifier is having approximately unity gain and low output impedance. The results also reveal that the proposed differential amplifier using JL-DG MOSFET provides higher output voltage swing and high voltage gain. Further, the CMOS inverter has been designed by using the proposed JL-DG MOSFET and investigated to identify the digital circuit applications. A switching voltage

of 0.43 V, noise margin of 0.265 V, and a delay of 19.18 p sec have been achieved with the CMOS inverter using JL-DG MOSFET at 20 nm technology node. Hence, The JL-DG MOSFET has been used in high-performance, low power analog, and digital circuit applications.

Declarations

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Conflict of Interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

Author Contribution

All authors have made substantial contributions to the conception and design, or acquisition of data, or analysis and interpretation of data; have been involved in drafting the manuscript or revising it critically for important intellectual content, and have given final approval of the version to be published. Each author has participated sufficiently in work to take public responsibility for appropriate portions of the content. All authors read and approved the final manuscript.

Availability of data and material

The data and material are available within the manuscript.

Compliance with ethical standards

The authors declare that all procedures followed were in accordance with the ethical standards.

Consent to participate

All the authors declare their consent to participate in this research article.

Consent for Publication

All the authors declare their consent for publication of the article on acceptance.

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Figures

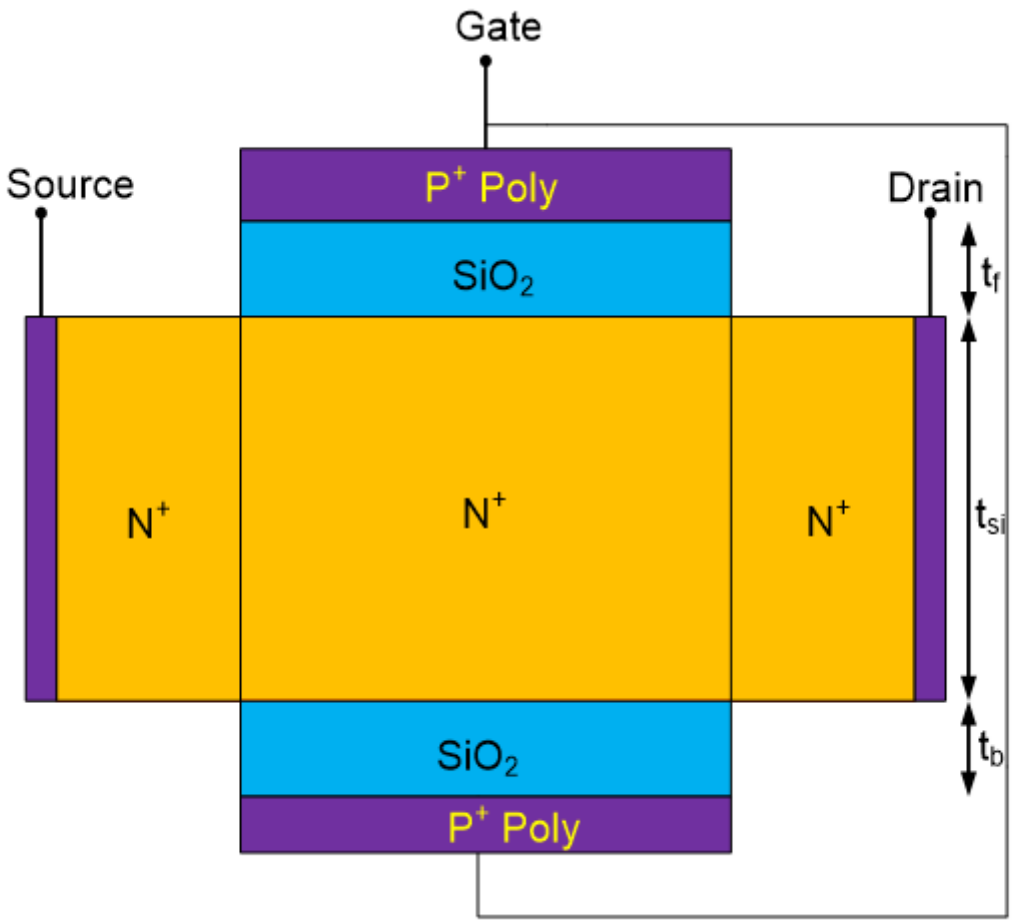

Figure 1

2D representation of JL-DG MOSFET.

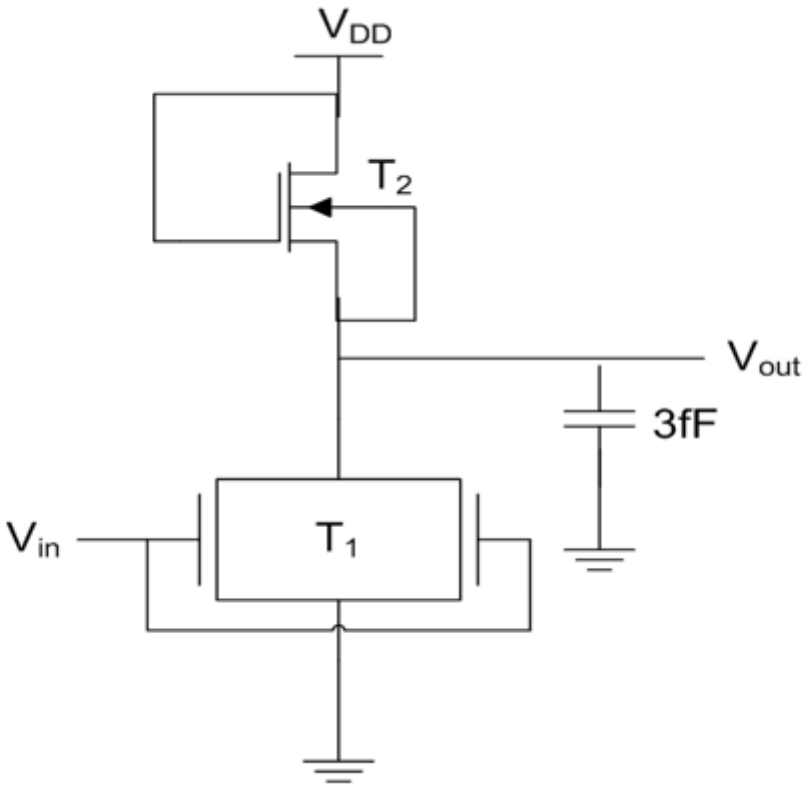

Figure 2

The common source amplifier with diode-connected load using JL-DG MOSFET.

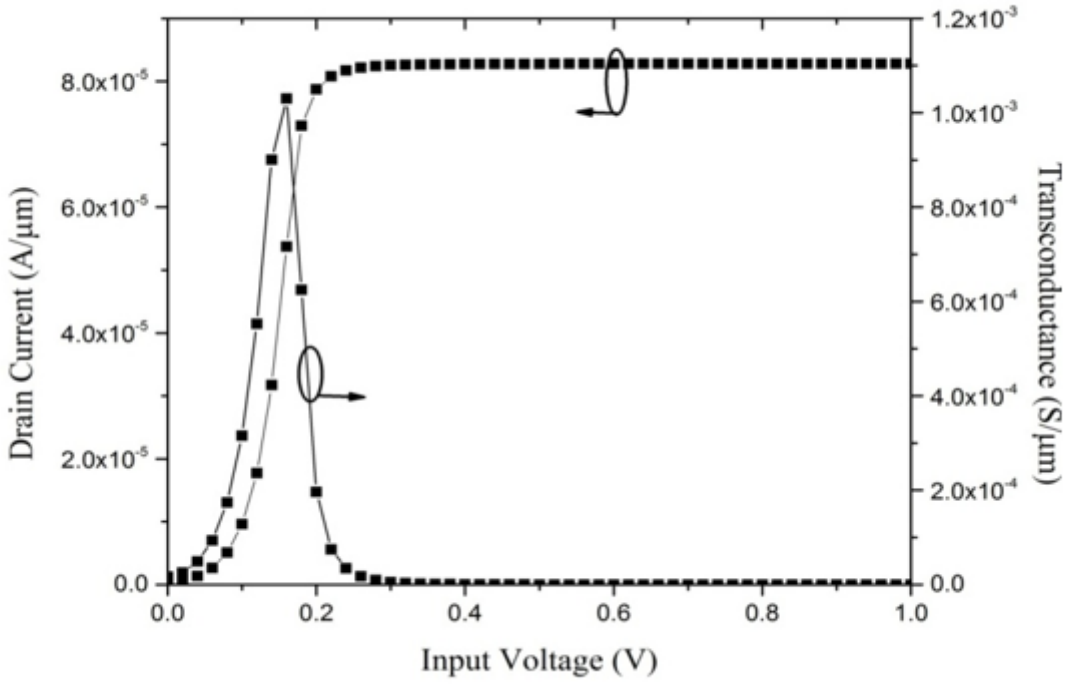

Figure 3

The variation of ID and gm with input voltage.

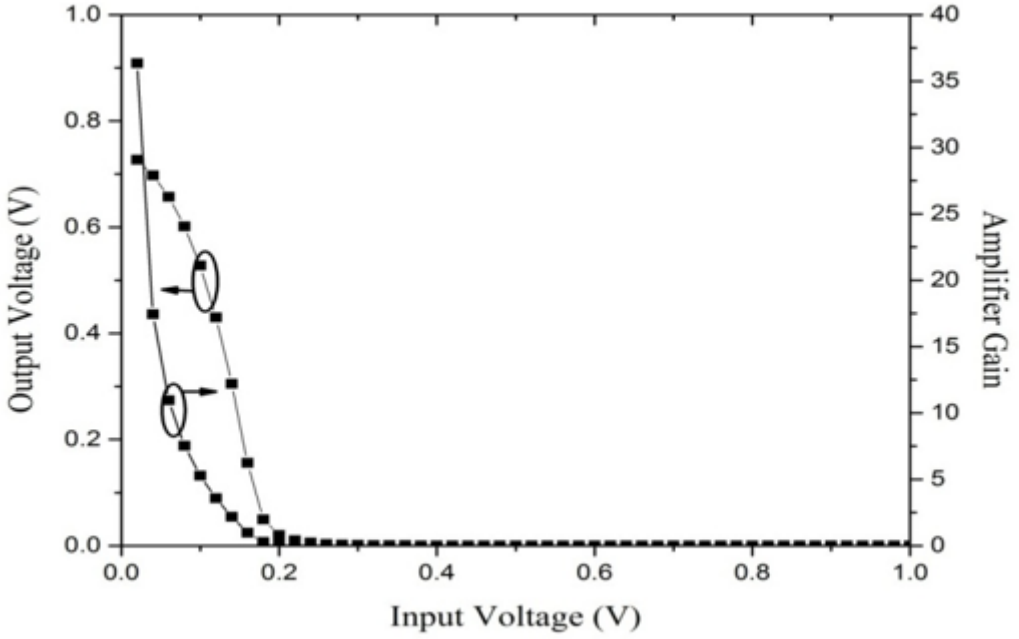

Figure 4

The variation of output voltage and gain of CS amplifier with input voltage.

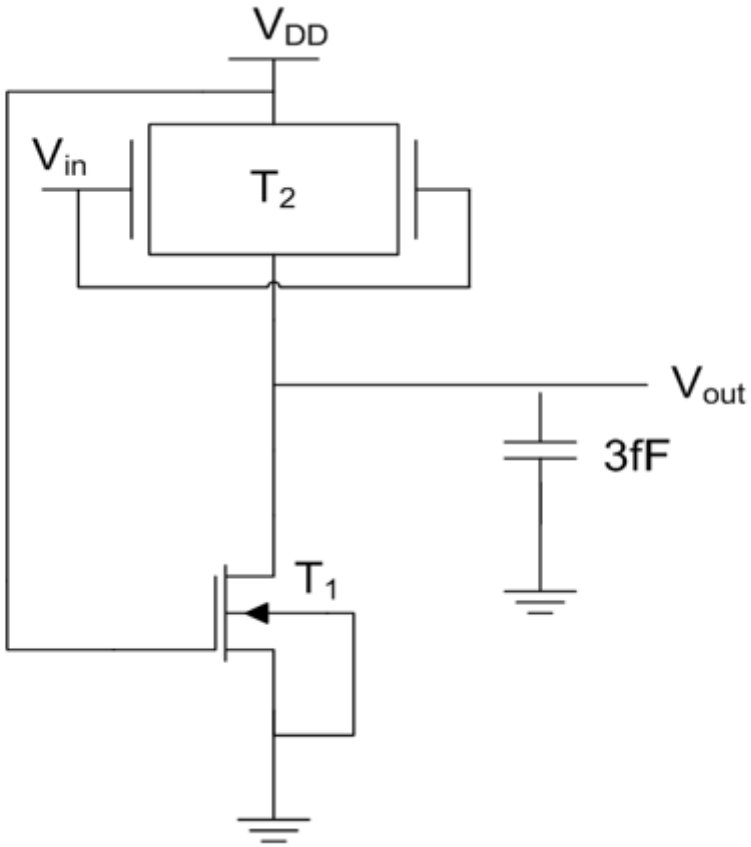

Figure 5

The source follower amplifier using JL-DG MOSFET.

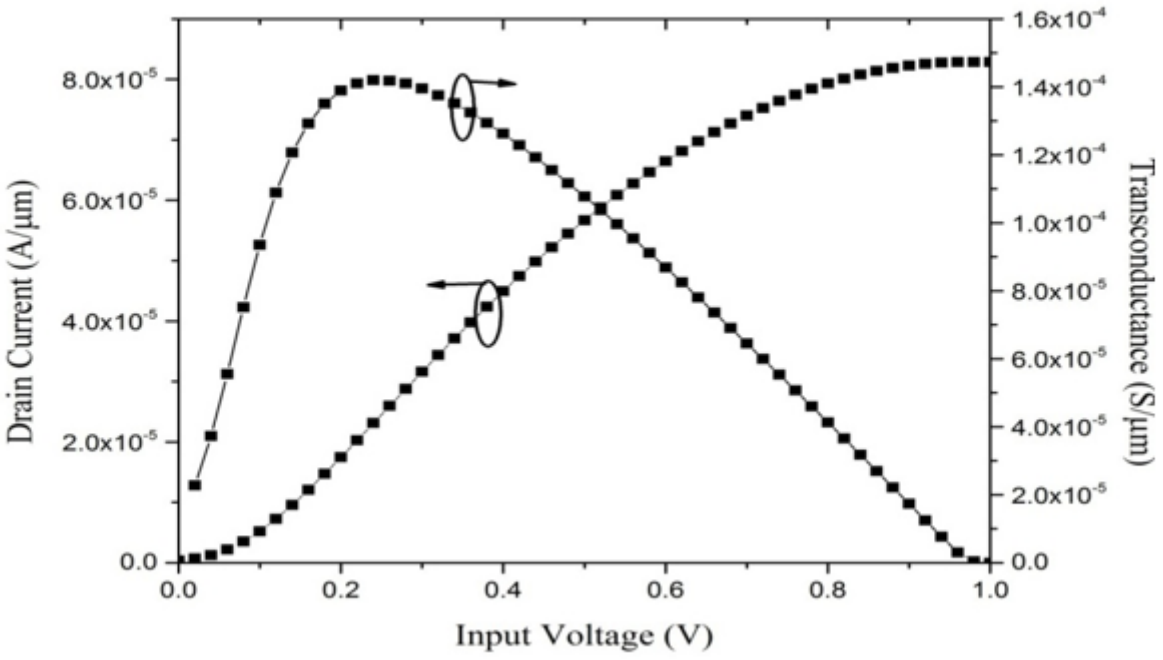

Figure 6

The variation of ID and gm of source follower stage with input voltage.

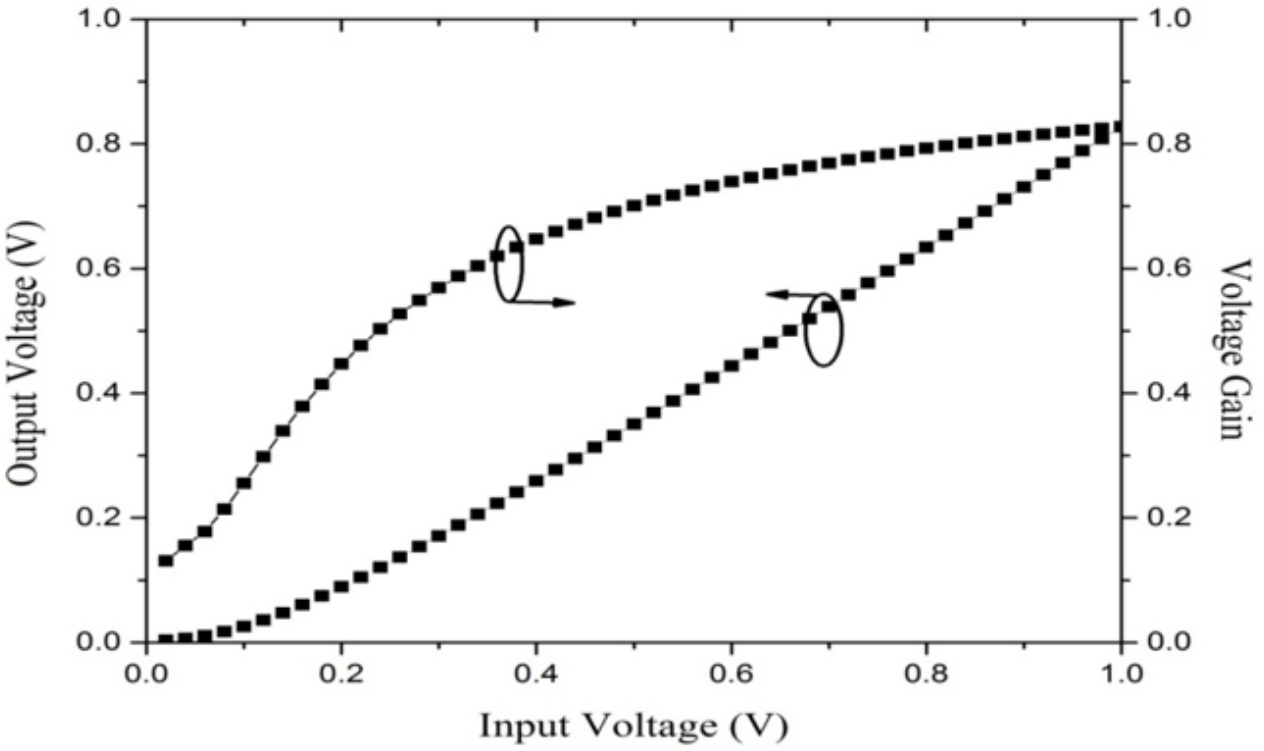

Figure 7

The variation of output voltage and gain of source follower stage with input voltage.

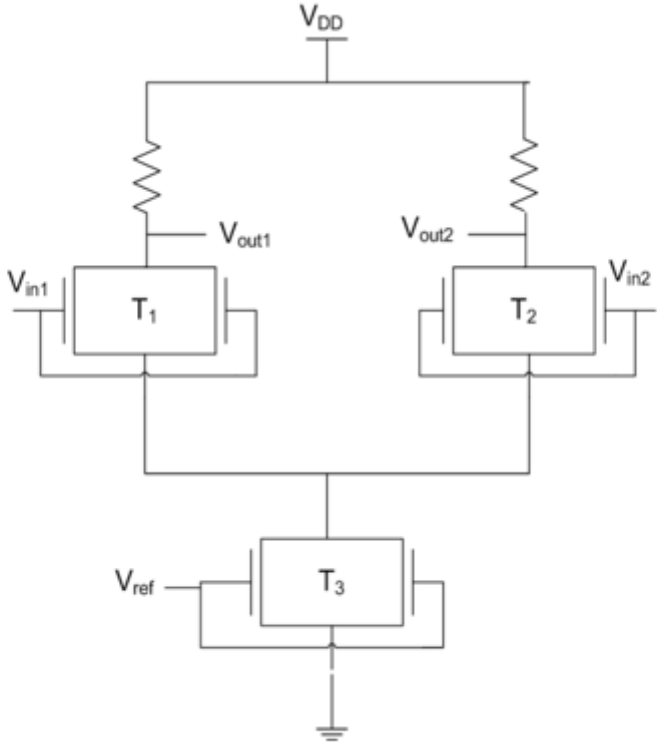

Figure 8

The resistive load differential amplifier using JLDG MOSFET.

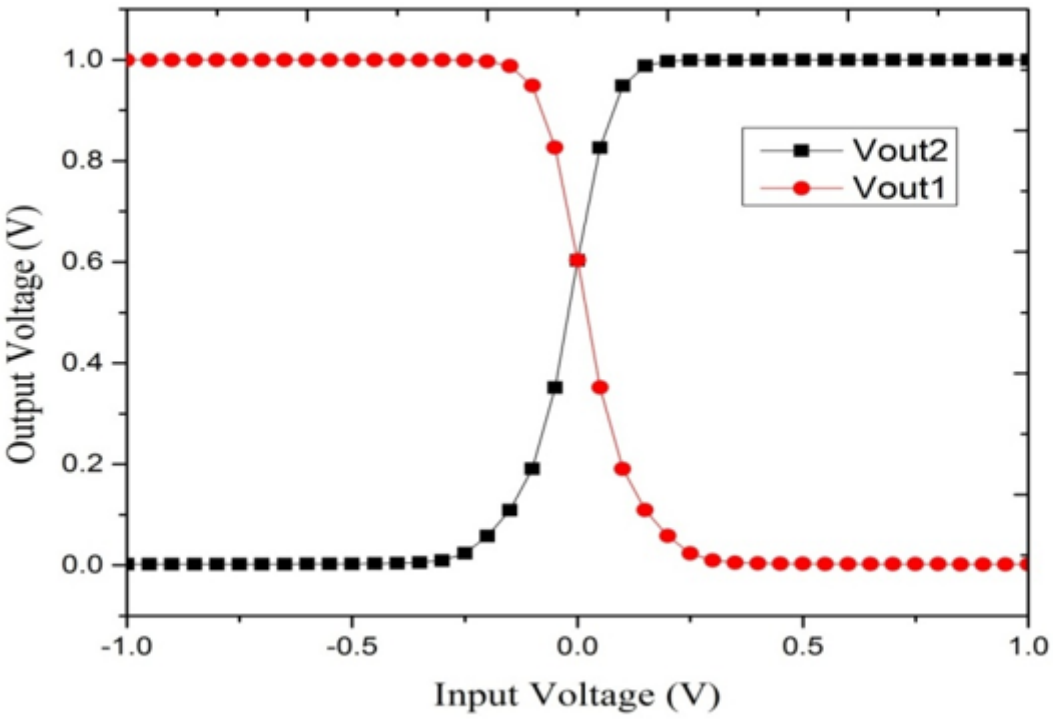

Figure 9

The input-output characteristics of the differential amplifier using JL-DG MOSFET.

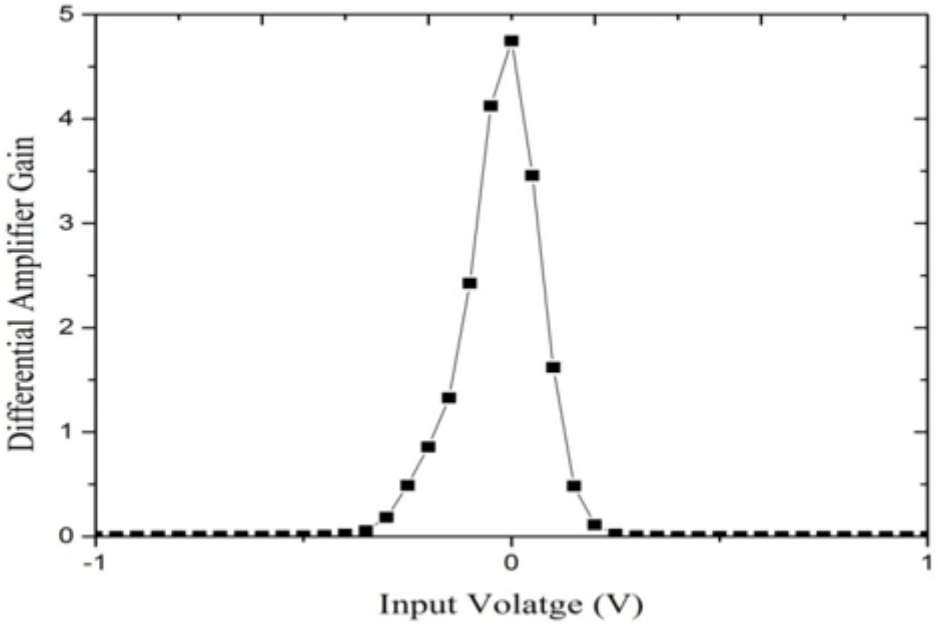

Figure 10

Variation of gain of differential amplifier with differential input voltage.

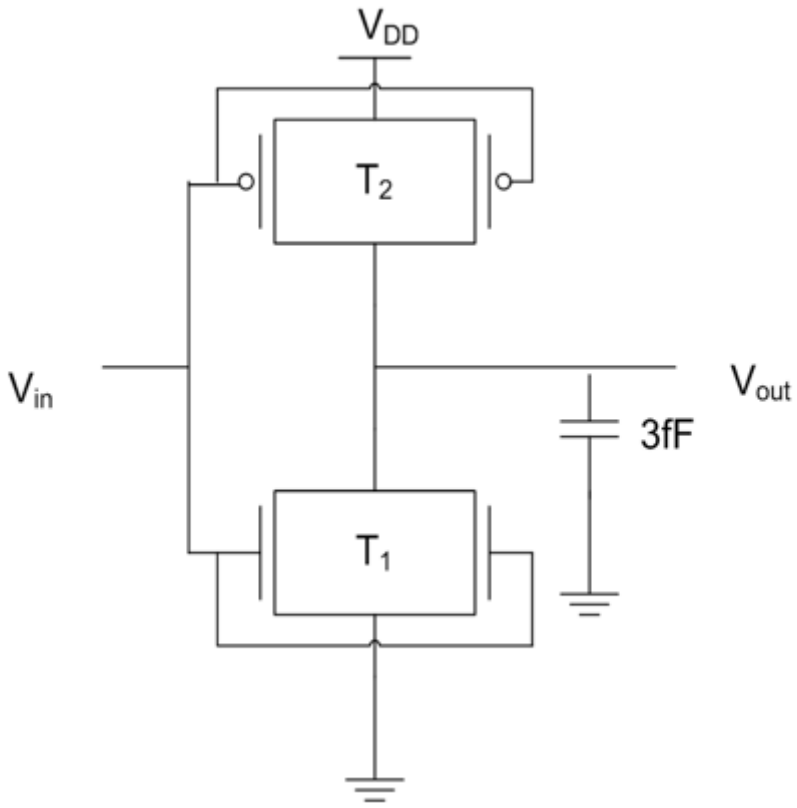

Figure 11

CMOS inverter using JLDG MOSFET.

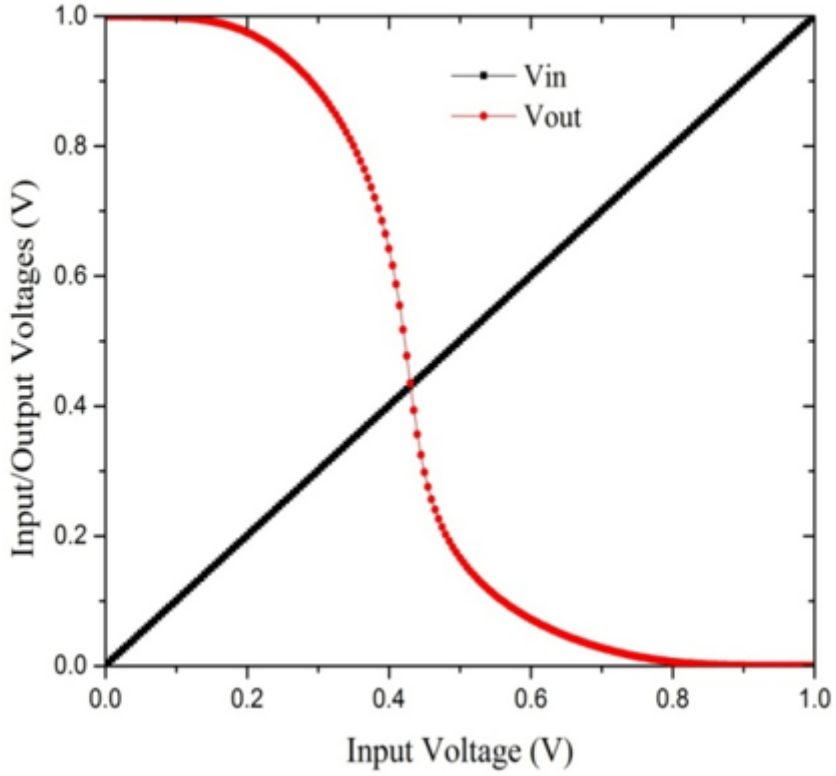

Figure 12

The voltage transfer characteristics of CMOS inverter.

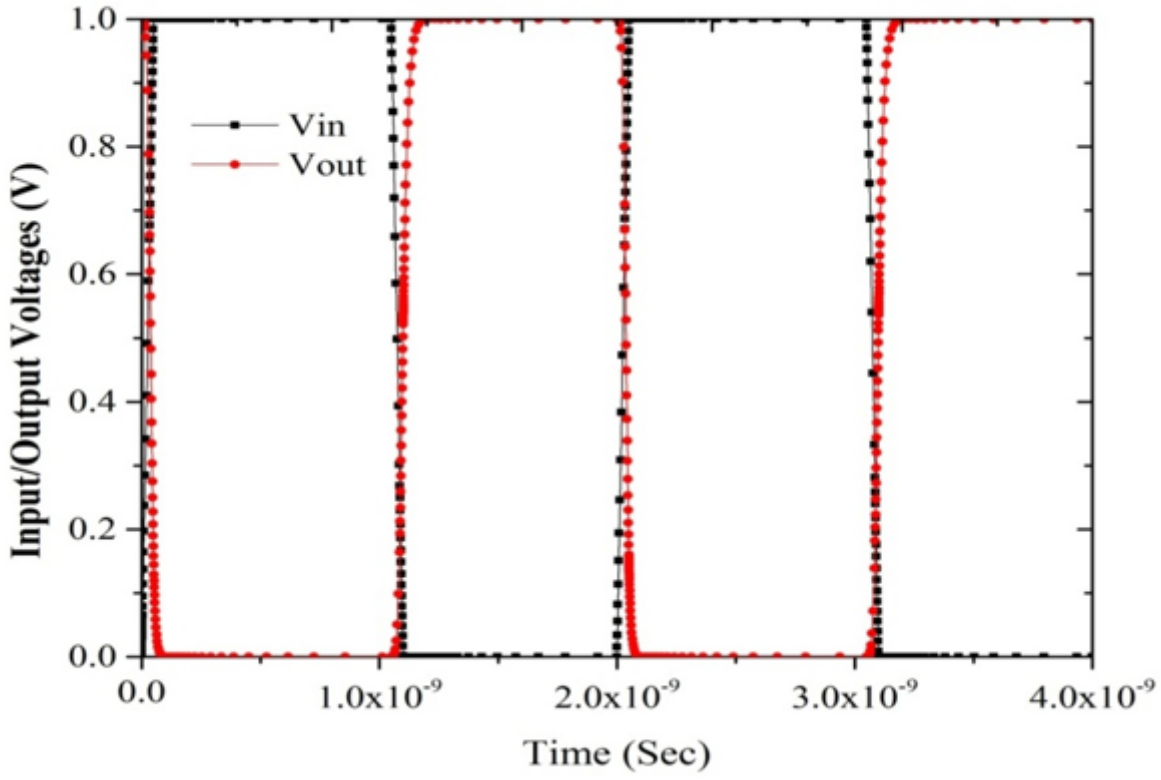

Figure 13

The transient analysis of CMOS inverter.