Junctionless Accumulation Mode Ferroelectric FET (JAM-FE-FET) for High Frequency Digital and Analog applications

Snehlata Yadav
Delhi Technological University
Sonam Rewari (rewarisonam@gmail.com)
Delhi Technological University https://orcid.org/0000-0001-8946-9849
Rajeshwari Pandey
Delhi Technological University

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Junctionless Accumulation Mode Ferroelectric FET (JAM-FE-FET) for high frequency Digital and Analog applications

Snehlata Yadav[1], Sonam Rewari[1], Rajeshwari Pandey[1]
snehlata_2k19phdec03@dtu.ac.in, rewarisonam@gmail.com, rajeshwaripandey@gmail.com
[1] Department of Electronics and Communication Engineering, Delhi Technological University, New Delhi-110042, India

Abstract:
In this paper, a Junctionless Accumulation Mode Ferroelectric Field Effect Transistor (JAM-FE-FET) has been proposed and assessed in terms of RF/analog specifications for varied channel lengths through simulations using TCAD Silvaco ATLAS simulator, using the Shockley-Read-Hall (SRH) recombination, ferro, Lombardi CVT, fermi and LK models. Major analog metrics like transconductance (g_m), intrinsic gain (A_V), output conductance (g_d), and early voltage (V_{EA}) are obtained for the JAM-FE-FET arrangement. The proposed structure shows an improvement in parameters like gm, I_{on}/I_{off}, A_v, TGF by 6.82%, 27.95%, 5.2%, 38.83% respectively. Further, frequency analysis of the proposed device is performed and several critical RF parameters like f_T, TFP, GFP, and GTFP have been observed to be enhanced by 6.89%, 11.38%, 13.65%, 12.01% respectively. Thus, the Junctionless accumulation mode ferroelectric FET (JAM-FE-FET) arrangement has been found to have superior analog and RF performance when compared to Junctionless ferroelectric FET(JL-FE-FET). As a result, the JAM-FE-FET device presented here can be contemplated a good contender for applications in high-frequency systems.

Keywords: Ferroelectric, Negative capacitance, Junctionless Accumulation mode (JAM), RF parameters, HZO

1. Introduction:

Various MOSFET structures have been realized over the last few decades, and their scaling has been quite successful down to the nano scale, resulting in a significant increase in performance [1],[2]. However, when the size of such transistors is reduced, junctions become closer, which is difficult due to the significant doping concentration gradients required. In order to combat this problem, J. E. Lilienfeld in the 1920s introduced the concept of Junctionless transistors [3]. It was successfully fabricated at the Tyndall Institute by Colinge et al [4]. The major characteristic feature of this device is the absence of p-n junction which avoids the requirement of gradients in doping concentration[5]. Various analytical study of surface potential for junctionless transistor has also been done[6],[7]. It has also been reported that cylindrical surrounding gate MOSFETs shows good switching performance and also can be used for microwave frequency applications[8],[9],[10]. However, the junctionless transistor poses various limitations such as degraded mobilities due to high doping concentrations.

Also, some of the significant obstacles in the device include the higher gate work function for completely depleted channel region in order to insure turning off the device. To address the aforementioned issues, a new modified structure known as the JAM FET was introduced [11], which has highly doped S/D regions and decreased doping in the channel, resulting in reduced mobility deterioration [12]. Another major issue that has arisen as a result of shrinking and the increased density of transistors on a chip is higher power consumption and heat dissipation, both of which slow down data processing rate [13],[14]. This can be enhanced by overcoming the lower working voltage restriction known as 'Boltzmann's Tyranny,' which allows the transistor operation voltage to be reduced, lowering power consumption. One such promising device is the ferroelectric field effect transistors (FE-FETs) [15]. Various investigations to understand the behavior of FE-FETs have been conducted in the past [16],[17],[18]. The majority of the research, however, concentrated on hysteretic behavior in memory applications [19],[20].

The discovery of ferroelectric properties in hafnium oxide (HfO_2) [21] in 2011 has gained a lot of attention [22],[23] because of its CMOS compatibility. Higher remnant polarization and large coercive field, at minimal thickness [24],[25], and superior performance characteristics have been demonstrated in ferroelectric HfO_2[26]. Due to its lower annealing temperature [27] and customizable ferroelectric properties, zirconium-doped HfO_2 (HZO) has popped up as a potential material [28],[29]. Apart from realizing memory, ferroelectric hafnium oxide is the sole material system that may be utilized to realize a new form of steep slope device called a Negative Capacitance Field Effect Transistor (NCFET) that was proposed in 2008 [30]. Negative capacitance FET has been studied both theoretically and practically for digital applications due to its ability to produce a subthreshold swing (SS) of 60 mV/decade [31],[32]. Although there are several demonstrations and investigations of digital and DC behavior of NCFET in the reported literature, the high frequency (RF) capabilities of NCFETs are yet to be fully explored. For RF applications of NCFET in future, research in this direction is crucial. Most of the previous research on NCFET have focused on Metal ferroelectric metal insulator semiconductor (MFMIS) configuration structure

[33],[34],[35],[36]. This structure simplifies modeling since the ferroelectric–insulator interface has a uniform potential, but the leakage currents would render the negative capacitance of ferroelectric FET unstable. Because of this instability, it is difficult to bias MFMIS devices and circuits, making the MFMIS structure unsuitable for RF applications. A metal–ferroelectric–insulator–semiconductor (MFIS) structure, on the other hand, mitigates these issues [37] and produces different overall device properties as a result of a spatially changing ferroelectric potential than MFMIS devices. Thus, the MFIS structure have always been preferred for integrating in advanced technologies. RF performance of MFIS NCFETs has also been investigated in few researches. Experiment in [38] revealed a modest improvement in f_T, while simulations by [39] revealed circuit-level figures of merit. However, no report has been published on the RF performance of JAM- FE-FET. Quantum confinement is also investigated in relation to ferroelectric thickness (t_{FE}) and channel thickness (t_{ch}). The quantum confinement effect reduces when the valus of t_{FE} and t_{ch} are greater than 7 nm and 15 nm respectively [40]. In our study, quantum mechanical effect has not been considered and therefore, the channel thickness and ferroelectric thickness are restricted to 20 nm and 10nm respectively. Thus, motivated by these coexisting research findings, a novel device structure, JAM-FE-FET is reported in this paper. This study takes the entire RF capabilities of NCFET with MFIS structure and incorporating the benefits of JAM FET.

Following the introduction, the next section delves into the device structure and simulation methods. The suggested device's performance parameters are examined in Section 3. Conclusions are drawn in the final section.

2. Proposed Structure & Simulation Parameters:

The schematic illustration of a JAM-FE-FET is shown in Fig. 1(a). All simulations are run on the TCAD Silvaco ATLAS simulator, with the Shockley-Read-Hall (SRH) recombination, ferro model, Lombardi CVT model, fermi and Landau-Khalatnikov (LK) models [41] being used. According to previous research, the negative capacitance is caused by a unique relationship between the electric field (E_{FE}) and polarization (P) of the ferroelectric layer which is given by the following equation:

$$E_{FE} = \alpha P + \beta P^3 + \gamma P^5 + \rho \frac{dP}{dt} \quad (1)$$

where α, β, and γ are the ferroelectric material parameters and ρ is the kinetic coefficient linked to the time constant associated with change in ferroelectric polarization. The parameters for the compared devices are enlisted in Table 1. The proposed structure comprising a gate-stack of TiN/HZO/SiO_2 is employed in the simulations. The channel length (L) is varied from 90 nm to 32 nm and channel thickness (t_{ch}) is taken 20 nm. A ferroelectric layer with a thickness (T_{FE}) of 10 nm and an insulator layer thickness (t_{IL}) of 0.9 nm in the gate stack. In JAM-FE-FET, the doping in the silicon channel is 1e17 cm^{-3} with n-type dopants, whereas the source and drain regions are doped strongly with 1e19 cm^{-3} n-type dopants. The doping level for the entire simulation is considered to be uniform. Titanium Nitride (TiN) having work function (ϕ_m) 4.65eV is used as gate material. Thereafter, numerical approaches such as Gummel and Newton, have been contemplated to improve convergence. In addition to these, the specific properties of the ferroelectric material (HZO) are listed in Table 2, that induces the negative capacitance effect. The drain to source voltage (V_{ds}) was set to 50 mV and the gate to source voltage (V_{gs}) was varied from 0 to 1 V to obtain the transfer characteristics. Fig. 1(b) shows the drain current with and without quantum model. As seen in Fig. 1(b), quantum effects have no influence on the transfer characteristics and have thus been ignored in this study.

3. Device fabrication and calibration:

The fabrication of ferroelectric negative capacitance field effect transistor has been explained by D. Kwon et al. in 2019 [42]. The transistor can be fabricated by taking a silicon substrate followed by the active region formation using photolithography.

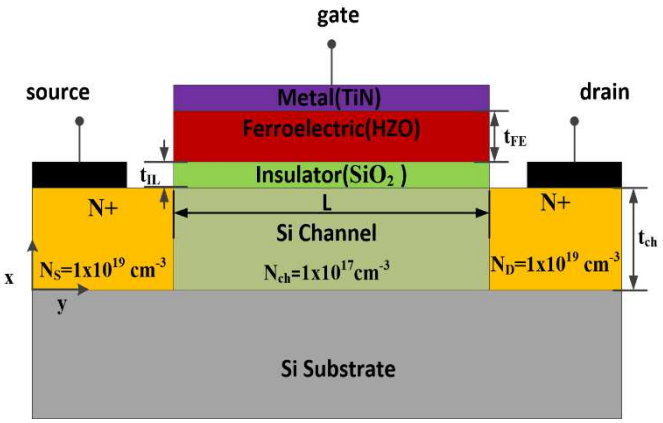


Fig. 1(a). A schematic representation of JAM-FE-FET

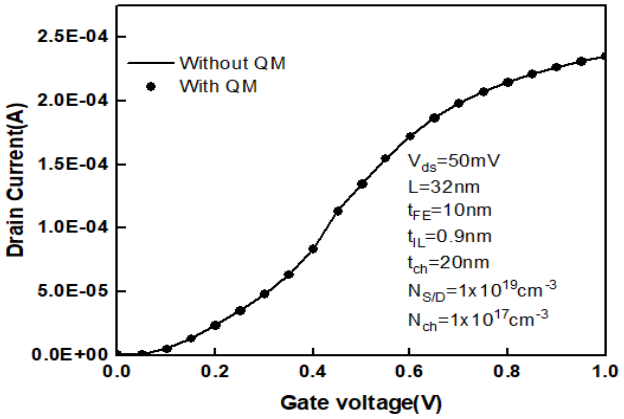


Fig. 1(b). The effect of the Quantum Model (QM) on the drain current

Table 1. Various parameters employed for the device simulation

Parameter	Symbol	JL-FE-FET	JAM-FE-FET
Channel length	L	90,45,32 nm	90,45,32 nm
Channel thickness	t_{ch}	20 nm	20 nm
Ferroelectric thickness	t_{FE}	10 nm	10 nm

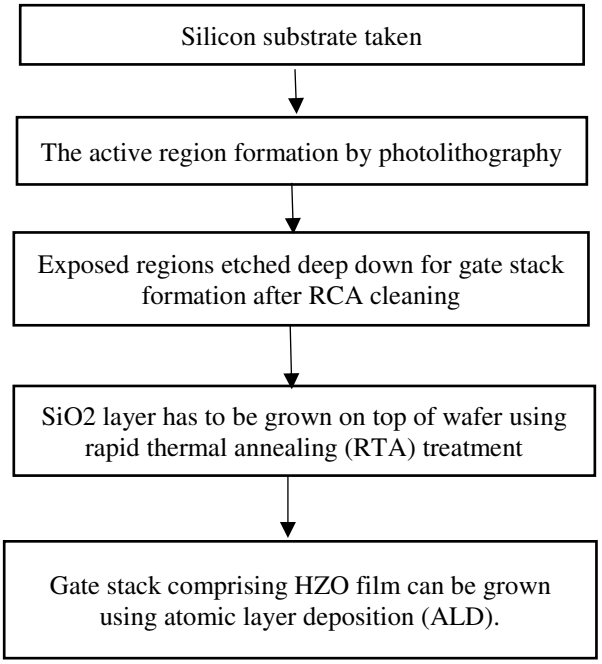
Insulator thickness	t_{IL}	0.9 nm	0.9 nm
Source/Drain doping	$N_{S/D}$	$1x10^{19}$ cm^{-3}	$1x10^{19}$ cm^{-3}
Channel doping	N_{ch}	$1x10^{19}cm^{-3}$ (n-type)	$1x10^{17}cm^{-3}$(n-type)
Metal work function	ϕ_m	4.65 eV	4.65 eV

Table 2. Properties of ferroelectric material (HZO)

Parameter	Symbol	Values
Spontaneous Polarization	Ps	10-40μC/cm^2
Remnant Polarization	Pr	1-40μC/cm^2
Coercive Field	Ec	1-2MV/cm
Dielectric constant	ε	30

Next, the exposed regions have to be etched deep down for the gate stack formation after RCA cleaning. On top of the wafer, rapid thermal annealing (RTA) treatment can be used to grow SiO2 layer. Further, the ferroelectric gate oxide, an HZO film deposition using atomic layer deposition (ALD) has to be performed. For short channel devices, electron beam lithography can be used to define the gate region. Ion implantation can then be performed on the exposed source/drain (S/D) areas. Next, the post metallization anneal in N_2 ambient can be performed for dopant activation and finally metal contacts of sputtered TiN gate electrode can be formed at the top. The steps of fabrication process is shown by a flowchart in Fig. 2(a).

The proper calibration of this research work is done with the experimental ferroelectric research under the same device dimensions [42]. The Shockley-Read-Hall (SRH) recombination, ferro model, Lombardi CVT model, fermi and Landau-Khalatnikov (LK) models are used for calibration. The transfer characteristic curves in Fig. 2(b), are in good agreement with one other.



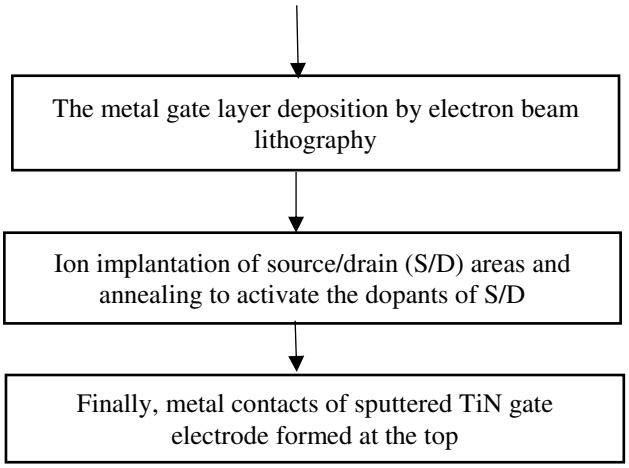


Fig. 2(a). Fabrication flowchart of proposed JAM-FE-FET

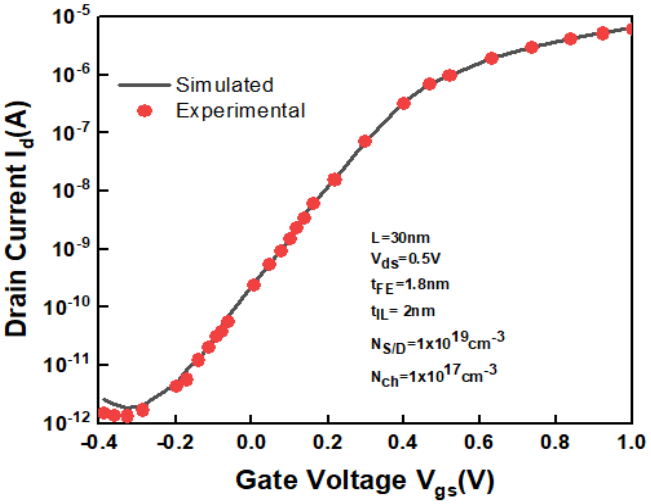


Fig. 2(b). Calibrated transfer characteristics of simulation data with experimental data[42]

4. Results & Discussions:

Fig. 3 demonstrates how the drain current of JAM-FE-FET and JL-FE-FET varies with gate voltage for various channel lengths. Fig. depicts that JAM-FE-FET have higher drain current over JL-FE-FET. The greater mobility of carriers in the channel is responsible for this improvement. The drain current (I_{on}) increases dramatically when the channel length L is scaled down from 90 nm to 32 nm, as shown in Fig. 3. The results for I_{on} increment in short channel can be intuitively explained through velocity saturation theory in which the inversion region current is in proportion to the device total oxide capacitance [43].

Table 3. I_{on}/I_{off} Ratio

Parameter	L=32nm		L=45nm		L=90nm	
	JAM-FE-FET	JL-FE-FET	JAM-FE-FET	JL-FE-FET	JAM-FE-FET	JL-FE-FET
I_{on}	2.35×10^{-4}	2.21×10^{-4}	2.09×10^{-4}	1.95×10^{-4}	1.54×10^{-4}	1.43×10^{-4}
I_{off}	6.58×10^{-10}	7.96×10^{-10}	6.68×10^{-10}	8.04×10^{-10}	6.9×10^{-10}	8.37×10^{-10}
I_{on}/I_{off}	35.7×10^{4}	27.7×10^{4}	31.2×10^{4}	24.2×10^{4}	22.3×10^{4}	17.08×10^{4}

In addition to suppressing I_{off} by increasing total oxide capacitance, drain coupling in NCFET at lower gate voltage causes a repression of channel potential and a rise in energy barrier that grows greater as capacitance matching improves, further suppressing I_{off}.

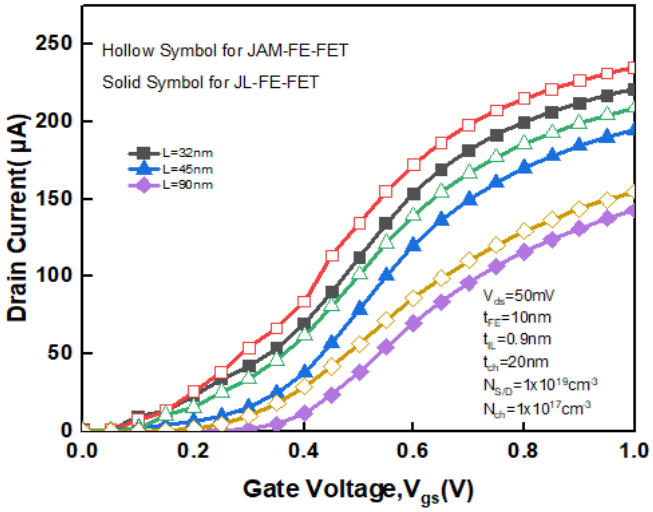


Fig. 3. Drain current variation with V_{gs}

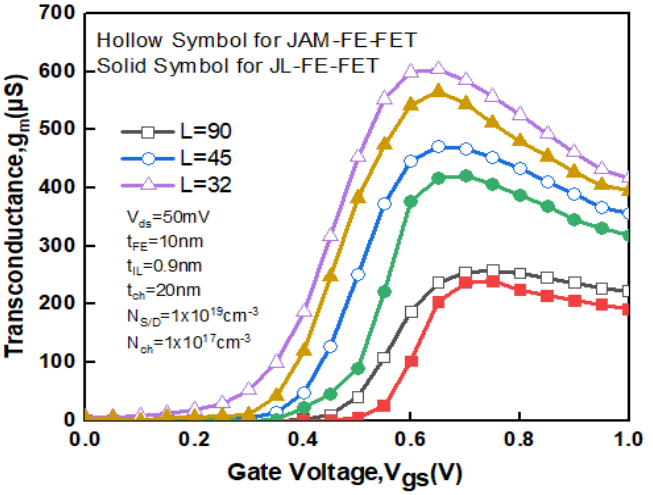


Fig. 4. Transconductance variation with V_{gs}

Transconductance is a measurement of the relationship between the deviation in drain current and the change in V_{gs} at constant V_{ds}. As illustrated in Fig. 4, gm is calculated using the I_d-V_{gs} curve derivative. Since the gate control over channel has been enhanced, and short channel effects have been decreased, the JAM-FE-FET has the highest transconductance value when compared to JL-FE-FET.

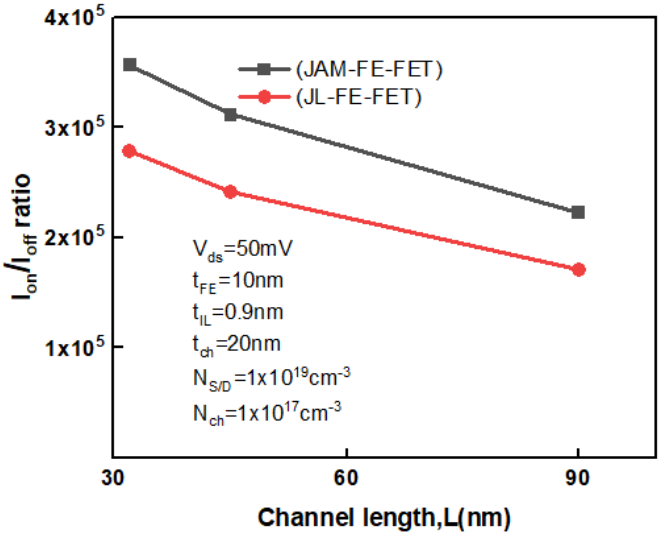


Fig. 5. I_{on}/I_{off} variation with channel length

Additionally, gate-stack construction improves average carrier velocity, which leads to higher electron mobility and, eventually, increased gm.

Fig. 5 shows the I_{on}/I_{off} ratio variation for JAM-FE-FET and JL-FE-FET for different channel length. I_{on} and I_{off} for these devices are obtained at V_{gs}= 1V and V_{gs}= 0V respectively for V_{ds}= 50mV. It is one of the most critical parameters for the digital applications. The I_{on}/I_{off} ratio for the compared devices are shown in Table 3.

It can be assessed that, I_{on}/I_{off} ratio for channel length L= 90 nm is low for digital devices. However, an improvement in I_{on}/I_{off} ratio of JAM-FE-FET over JL-FE-FET for channel length L= 32 nm has been obtained due to increased mobility in JAM configuration leading to increase in drain current with reduction in current leakage and consequently greater switching ratio.

The subthreshold swings for the compared devices are shown in Fig. 6. It has been discovered that both the devices have steep SS behavior (<60mV/dec). Subthreshold slope values fewer than 60 mv/dec have also been seen in previous research studies[44]. Hence the device can be switched quickly over a wide range of current. It can also be observed that as the gate length is reduced the subthreshold value increases.

SS can be expressed as:

$$SS = \frac{\partial V_{gs}}{\partial log_{10} I_d} \qquad (2)$$

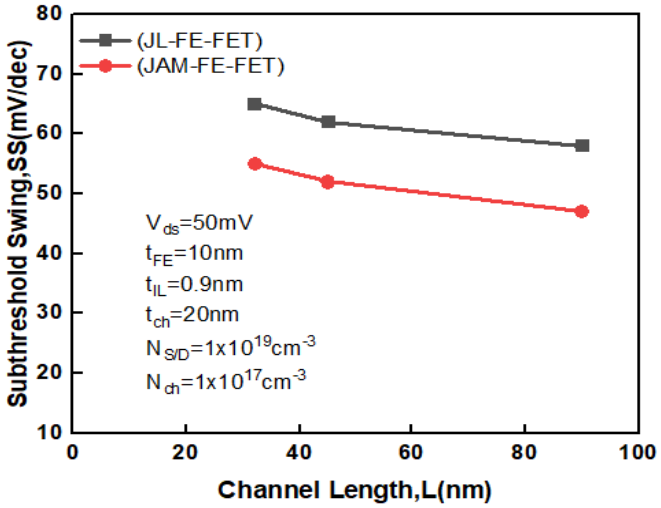


Fig. 6. SS variation with channel length

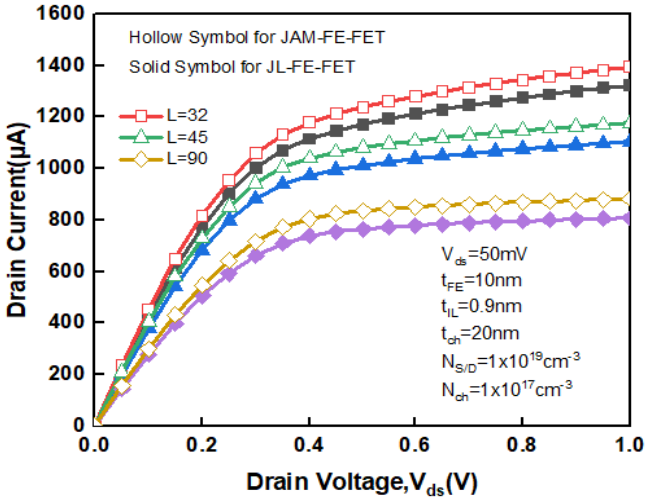


Fig. 7. Drain current variation with V_{ds}

For V_{gs}= 1V, Fig. 7 depicts the drain current variation with drain voltage. The figure clearly indicates that, similar to JL-FE-FET, in the linear region drain current is almost identical, but in the saturation region, device with shorter gate lengths display greater saturation currents.

Fig. 8 depicts the output conductance variation for the compared device structures. The output conductance can be calculated by varying the drain current with the drain to source voltage while maintaining the constant gate to source voltage. It can be expressed as [45]:

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \tag{3}$$

It can be inferred from the figure that g_d is higher in the linear region and keep up a constant value in the saturation region. Thus, the driving capability of the proposed device is greater than the compared one.

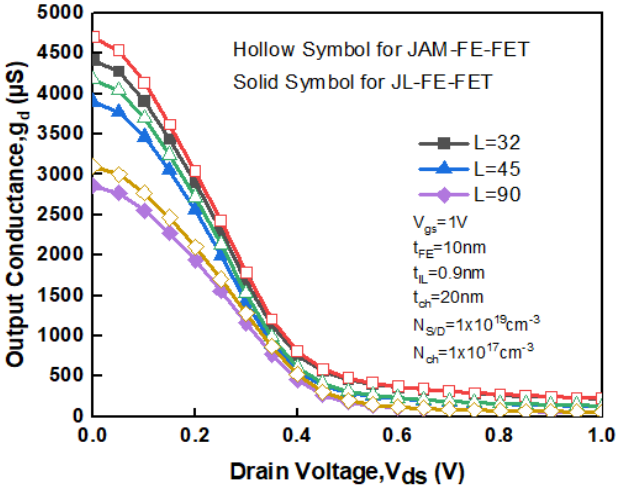


Fig. 8. Output conductance variation with V_{ds}

It can also be assessed from the graph that the output conductance increases when the scaling of channel length is done from 90 nm to 32 nm due to the suppressed short channel effects and the increased gate controllability.

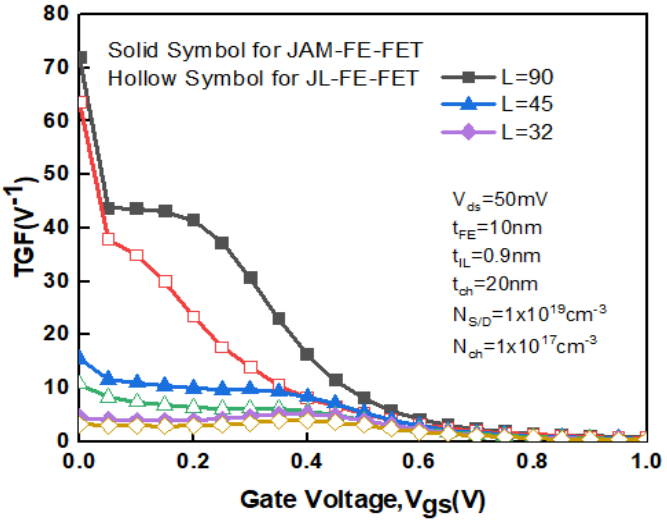


Fig. 9. TGF as a function of V_{gs}

Transconductance Generation factor (TGF) can be defined as the accessible gain per unit power loss. It can be expressed as

$$TGF = \frac{g_m}{I_d} \tag{4}$$

The device that operates at lower supply voltage performs better for higher TGF values. It is clearly evident from Fig.9 that the proposed device structure attains the maximum TGF value. Since the drain current is higher, it corresponds to high value of transconductance and eventually high TGF.

Immunity to the channel length modulation (CLM) is provided by Early Voltage (V_{EA}) [45]. Early Voltage is expressed as:

$$V_{EA} = \frac{I_d}{g_d} \tag{5}$$

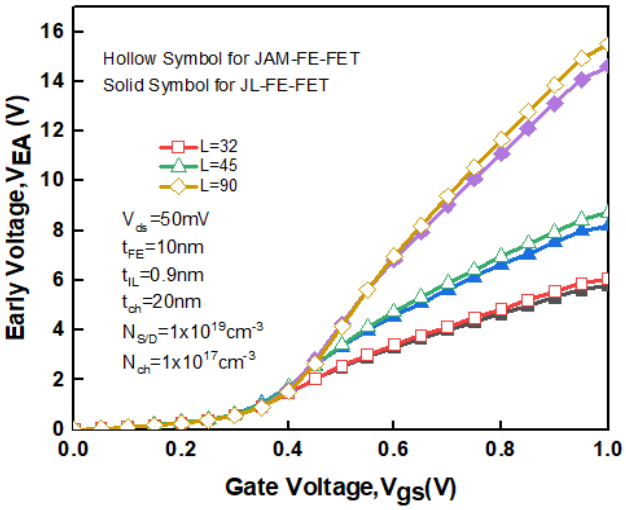


Fig. 10. Early Voltage variation with V_{gs}

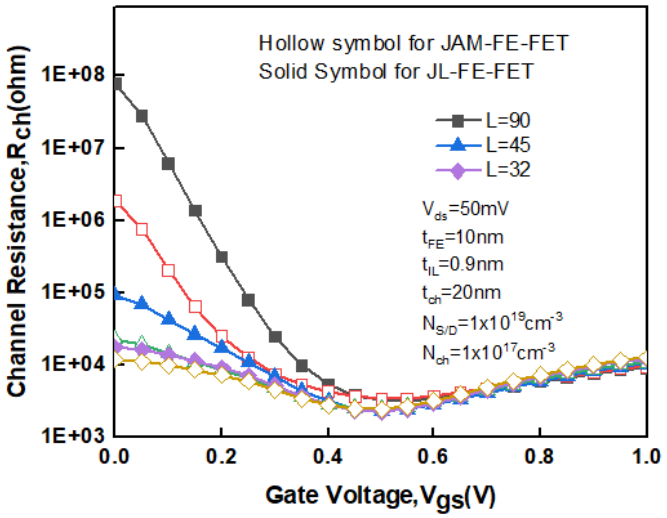


Fig. 11. Channel resistance variation with V_{gs}

The drain current rise, I_d in JAM-FE-FET is greater than the decrease in transconductance, resulting in a higher V_{EA} than in JL-FE-FET. For varied channel lengths, Fig. 10 depicts the early voltage shift as a function of gate bias. A greater V_{EA} indicates that the device will have higher gain and can be used in amplifiers [46]. Fig. 11 shows the channel resistance variation with the gate voltage. The channel resistance should be minimum for higher driving current. As can be observed from the figure that the JAM-FE-FET exhibits lower channel resistance owing to its increased carrier density and velocity in the channel region.

The next figure of merit is the intrinsic dc gain which can be defined as the transconductance (g_m) to output conductance (g_d) ratio, i.e., g_m/g_d [46]. Since g_d is extracted from static I_d–V_{ds} curve, so it is the low frequency or quasi-static result. It is a critical parameter for practical transconductance amplifiers. The change of g_m/g_d with gate voltage is shown in Fig. 12 for L= 32 nm, L= 45 nm and L= 90 nm for the compared devices. It can be observed from Fig. 12 that the intrinsic gain is higher at channel length 90 nm because of low output conductance which is essential for analog applications.

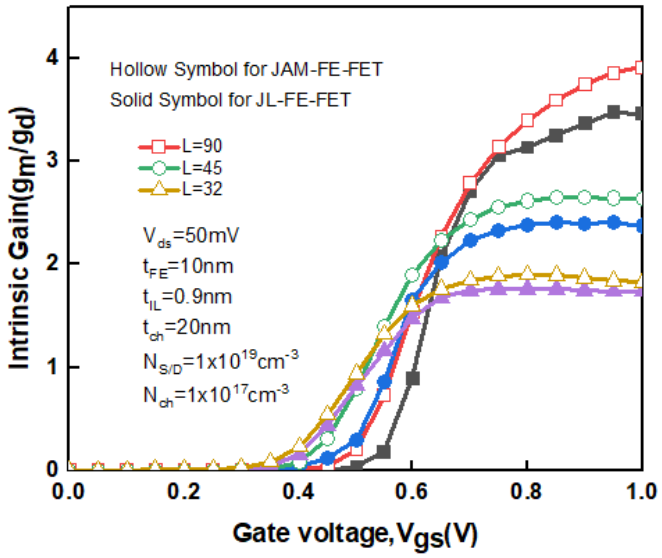


Fig. 12. Intrinsic gain variation with V_{gs}

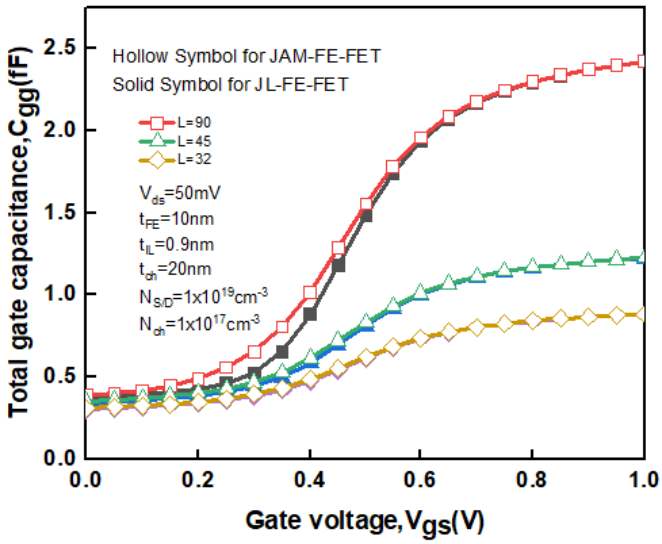


Fig. 13. C_{gg} variation with V_{gs}

The capacitive behavior of a device controls its high frequency functioning. Fig. 13 shows how a change in gate bias (V_{gs}) affects total gate capacitance (C_{gg}) in JAM-FE-FET and JL-FE-FET. It can be observed that JAM-FE-FET reveals profiles that are considerably closer to those of JL-FE-FET.

Cut off frequency denoted as f_T is an intrinsic property of the device and represents a figure of merit for high frequency operation. It can be expressed as:

$$f_T = g_m/2\pi C_{GG} \quad (6)$$

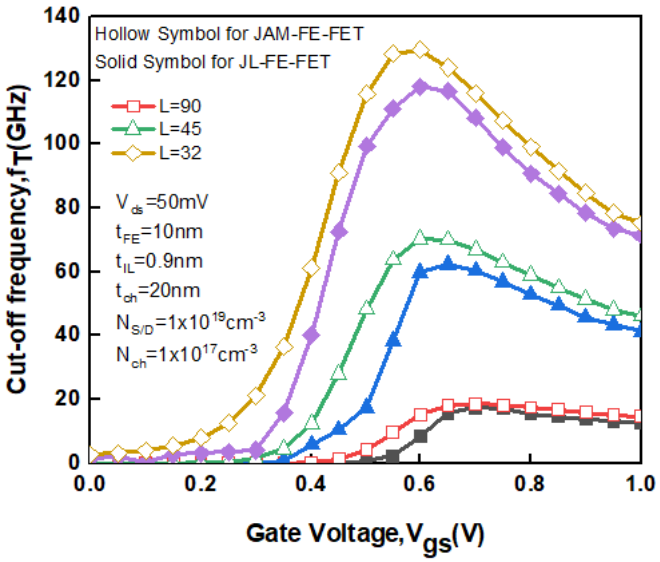


Fig. 14. f_T variation with V_{gs}

Cut-off frequency for different channel lengths with respect to gate voltage is shown in Fig. 14. The high value of cut-off frequency is observed because of high g_m value and comparable C_{gg}. However the cut off frequency further reduces for high gate voltages due to the increase in total gate capacitance.

The transducer power gain (G_T) can be defined as the P_{load} to the P_{source} ratio, where P_{load} is the average power given to the load, and P_{source} is the average power available from the source. It can be expressed as:

$$G_T = \frac{P_{load}}{P_{source}} \quad (7)$$

Maximum-Transducer-Power-Gain (MTPG) is described as a power gain that can be obtained when load is driven with the identical inputs.

The MTPGs for JL-FE-FET and JAM-FE-FET are shown in Fig. 15 for channel lengths varying from 30 nm to 90 nm. From the Fig. 15, it can be clearly interpreted that JAM-FE-FET has a higher gain owing to its architecture which overcomes the deterioration in mobility. It can also be inferred from the figure that as the channel length is scaled down from 90 nm to 45 nm the transducer gain increases drastically.

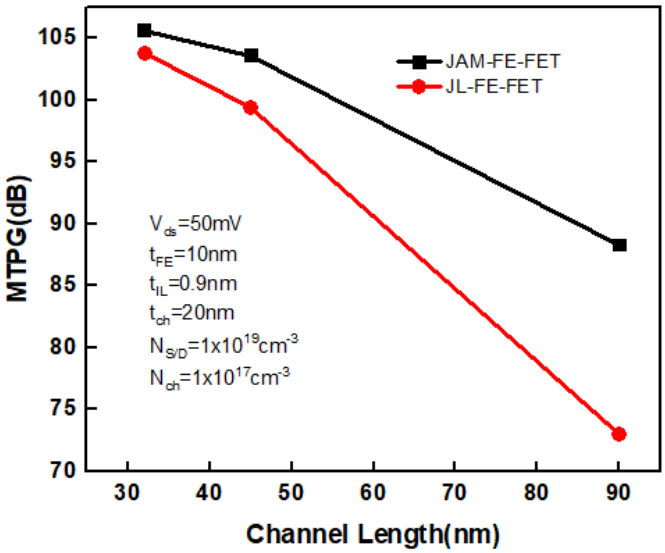


Fig. 15. MTPG variation with channel length

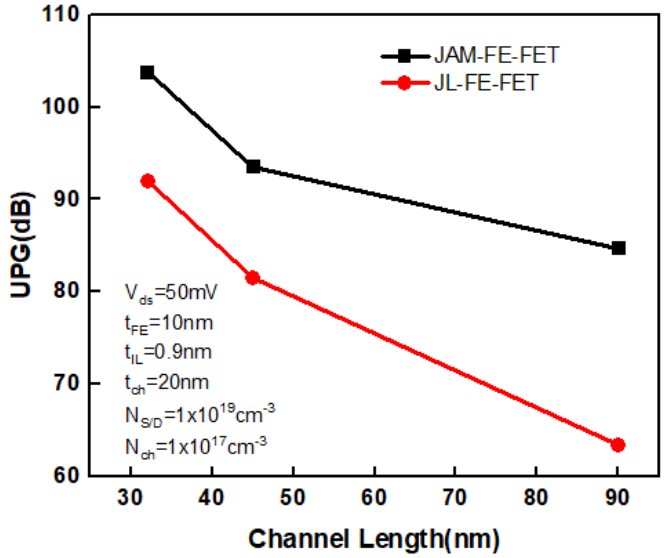


Fig. 16. UPG variation with channel length

Variation in Unilateral Power Gain (UPG) for JAM-FE- FET and JL-FE-FET with respect to V_{gs} is depicted in Fig. 16. When the gate bias is applied, the structure generates a larger electric field in addition to enhanced capacitance, resulting in increased electron velocity and therefore superior saturation velocity. As a result, it's reasonable to conclude that JAM-FE-FET has a greater UPG. It can also be inferred from the figure that as the channel length is increased from 45 nm to 90 nm there is a gradual decline in the unilateral power gain. Overall, the JAM-FE-FET possess high UPG.

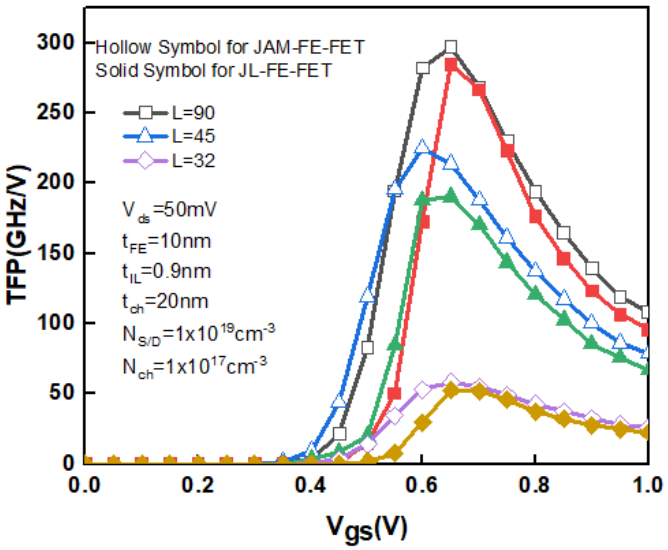


Fig. 17. TFP variation with V_{gs}

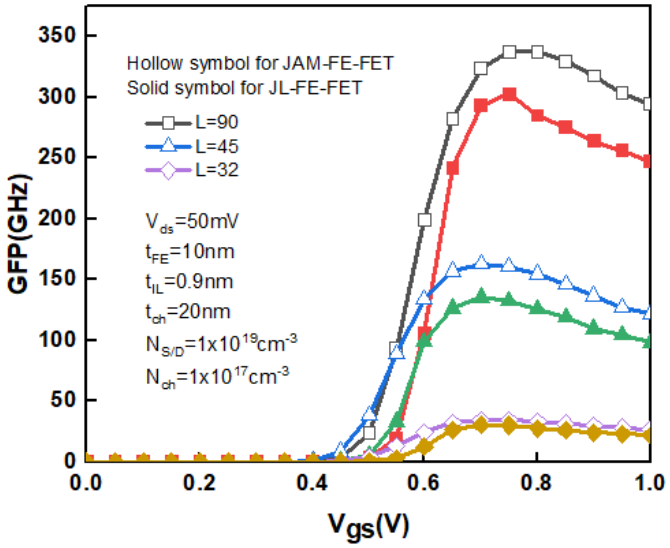


Fig. 18. GFP variation with V_{gs}

The total oxide capacitance also explains these trends. A better capacitance matching in Negative Capacitance FET helps in achieving a high oxide capacitance through which a higher TFP can be obtained. The Gain Frequency Product (GFP) is another performance parameter for high frequency operational amplifier applications. TFP and GFP are expressed as follows:

$$TFP = \frac{g_m f_T}{I_D} \quad (8)$$

$$GFP = \frac{g_m}{g_d} \times f_T \quad (9)$$

GFP increases with V_{gs} due to increment in f_T and intrinsic gain. The curves begin to decline owing to the charge carriers' saturation mobility, which is what causes parasitic capacitances to exist.

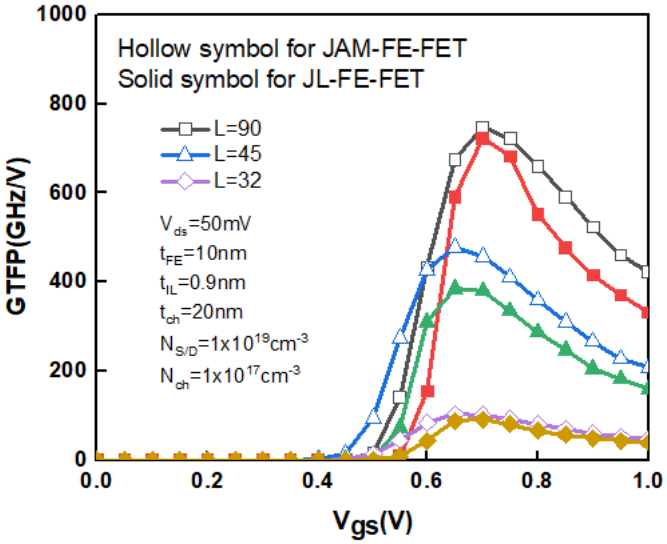


Fig. 19. GTFP variation with V_{gs}

Table 4. Performance parameters at channel length L = 32 nm

Parameter	JAM-FE-FET	JL-FE-FET	%Improvement
I_d(μA)	235.21	221.11	6.3
g_m(μS)	603.52	564.98	6.82
g_d(μS)	4700	4420	6.33
I_{on}/I_{off}(×10^6)	0.357	0.279	27.95
SS (mV/dec)	54	65	20.37
TGF(V^{-1})	4.54	3.27	38.83
V_{EA}(V)	6.07	5.80	4.65
Av (dB)	1.82	1.73	5.20
C_{gg}(fF)	0.83	0.82	1.21
f_T (GHz)	124	116	6.89
MTPG (dB)	105.63	103.78	1.78
UPG (dB)	103.79	91.97	12.85
TFP(GHz/V)	58.50	52.52	11.38
GFP(GHz)	34.45	30.31	13.65
GTFP(GHz/V)	101.8	90.88	12.01

Fig.17 and Fig.18 shows the comparison of TFP and GFP of both the device configuration. It can be observed that JAM-FE-FET possess higher values for both parameters. The RF parameter which determines the entire performance of the device is Gain Transconductance Frequency Product (GTFP). It is expressed as

$$GTFP = \frac{g_m}{g_d} \times \frac{g_m}{I_D} \times f_T \quad (10)$$

Higher the GTFP value, better is the device performance. So, from the Fig.19 it is clear that the proposed device achieves the high GTFP value which indicates better performance. This enhancement is due to the electric field reduction in JAM-FE-FET owing to its gate stack architecture resulting in an improvement of the parameters. Table 4. Gives the Performance parameters at channel length L = 32 nm

5. Conclusion

In this research article, a simulation-based comparative analysis is done for proposed JAM-FE-FET with JL-FE-FET. The SILVACO ATLAS 3D simulator was used to test the

performance of proposed device in terms of analog and RF characteristics. In terms of switching ratio, the suggested JAM-FE-FET device achieves the best results. In comparison to JL-FE-FET, the subthreshold swing is also lowered by 20.37%. The proposed device's SS improves as a result of the negative capacitance effect in the MFIS structure. The proposed device also shows an improvement in terms of transconductance and TGF by 6.82% and 38.83% respectively. The I_{on}/I_{off} ratio also shows a significant improvement of 27.95% owing to the device architecture which overcomes the mobility degradation in the channel region. Also, the capacitive behavior of the proposed device is in close agreement with the JL-FE-FET. However, the enhanced behavior of transconductance results in high cut-off frequency which is a critical parameter in RF applications. Various RF parameters like f_T, TFP, GFP and GTFP are enhanced by 6.89%, 11.38%, 13.65%, and 12.01% respectively. Therefore, from the above obtained results the proposed JAM-FE-FET can be viewed as a promising device for applications in high frequency systems.

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Not Applicable

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There are no conflicts of interest amongst the authors

9. AUTHOR CONTRIBUTIONS

The authors have contributed mutually regarding this paper.

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Not Applicable

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Not Applicable

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All the authors have complete consent to participate.

13. CONSENT FOR PUBLICATION

All the authors have complete consent for publication.

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All the ethics have been followed

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All the authors have Informed consent

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